SC18IS604

SPI to I²C-bus bridge

Rev. 1.0 — 22 September 2021 Product data sheet

1 General description

SC18IS604 is designed to serve as an interface between the standard SPI of a host (microcontroller, microprocessor, chip set, etc.) and the serial I²C-bus. This allows the host to communicate directly with other I²C-bus devices. SC18IS604 can operate as an I²C-bus controller-transmitter or controller-receiver. SC18IS604 controls all the I²C-bus specific sequences, protocol, arbitration and timing.

SC18IS604 is a functional replacement for SC18IS600 with exception of:

- New pinout
- Transmit and receive buffer of 255 bytes vs 96 bytes
- Five instead of six GPIOs; no quasi bidirectional mode
- Lower operating supply voltage level (1.71 V vs 2.4 V)
- Temperature range of -40 to +105 °C vs -40 to +85 °C
- Device is rotated 180 degrees in the tape pocket; pin 1 is now in Quadrant 1

2 Features and benefits

- SPI slave interface
- SPI Mode 3
- Single primary I²C-bus controller
- Five General Purpose Input/Output (GPIO) pins
- 5 V tolerant I/O pins
- High-speed SPI: Up to 1.2 MHz
- Fast-mode I²C-bus: 375 kHz
- 255-byte transmit buffer
- 255-byte receive buffer
- 1.71 V to 3.6 V operation
- Deep Power-down mode with SPI $\overline{CS}$ wake up
- Internal oscillator
- Active LOW interrupt output
- ESD protection exceeds 2000 V HBM per JESD22-A114
- Latch-up testing is done to JEDEC Standard JESD78 that exceeds 100 mA
- Available in TSSOP16 package

3 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
SC18IS604PW	18IS604	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SC18IS604PW	SC18IS604PWJ	TSSOP16	REEL 13" Q1 *STANDARD MARK SMD [1]	2500	T_{amb} = -40 °C to +105 °C

[1] Find packing information at www.nxp.com/docs/en/packing/SOT403-1_118.pdf

4 Block diagram

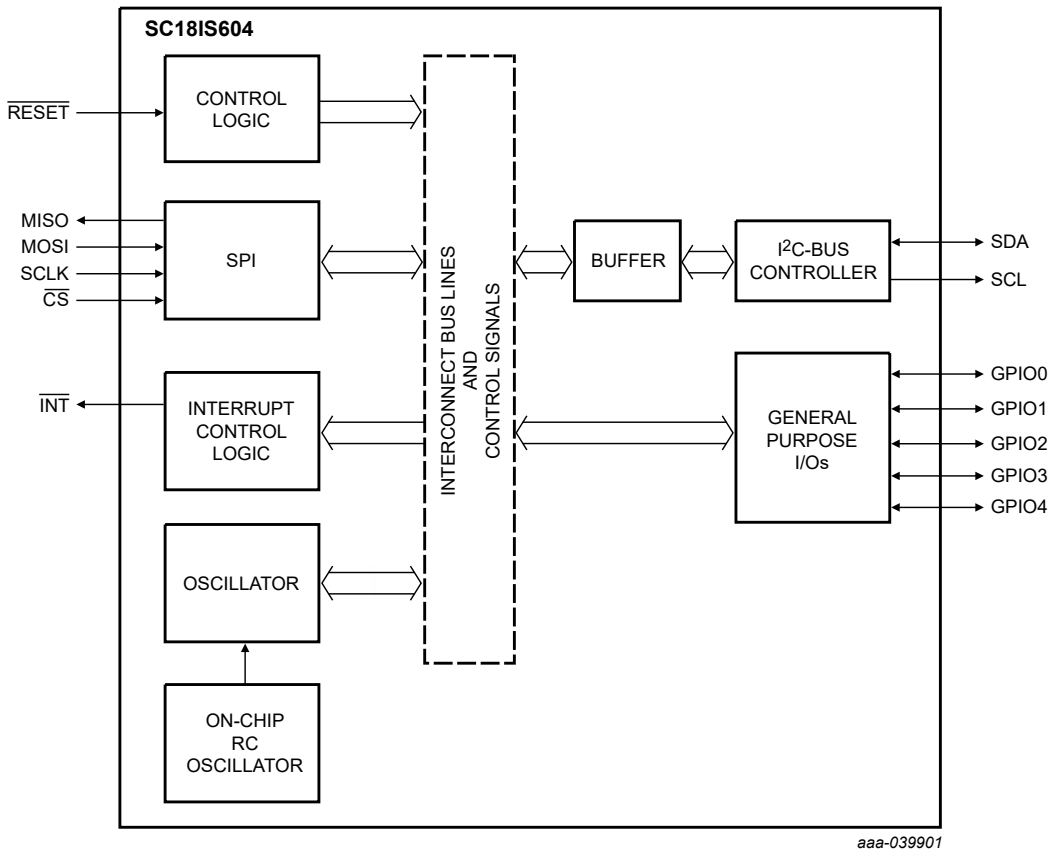


Figure 1. Block diagram of SC18IS604

5 Pinning information

5.1 Pinning

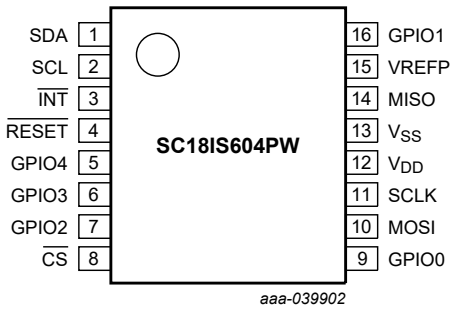


Figure 2. SC18IS604 pin configuration for TSSOP16

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
GPIO0	9	I/O	programmable I/O pin
$\overline{CS}$	8	I	Chip select. When $\overline{CS}$ is LOW, SC18IS604 is selected. $\overline{CS}$ is used to wake SC18IS604 from Deep Power-down mode. See Section 6.5.9 "Deep Power-down mode".
$\overline{RESET}$	4	I	Controller Reset. When active (LOW), $\overline{RESET}$ sets internal registers to the default values, and resets the I²C-bus and SPI hardware. See Table 4.
V_{SS}	13	I	ground supply voltage
MISO	14	O	SPI slave data output
MOSI	10	I	SPI slave data input
SDA	1	I/O	I²C-bus serial data input/output
SCL	2	O	I²C-bus serial clock output
GPIO1	16	I/O	programmable I/O pin
GPIO2	7	I/O	programmable I/O pin
SCLK	11	I	SPI clock input
V_{DD}	12	I	supply voltage
GPIO3	6	I/O	programmable I/O pin
$\overline{INT}$	3	O	Interrupt. When active (LOW), $\overline{INT}$ informs the CPU that SC18IS604 has an interrupt to be serviced. $\overline{INT}$ is reset (deactivated) either when the I2CStat register is read or as a result of a controller reset ($\overline{RESET}$). This pin is an open-drain pin which must be pulled HIGH with resistor and must not be held LOW at power on or reset.
GPIO4	5	I	input pin
VREFP	15	I	connect to V_{DD}

6 Functional description

SC18IS604 acts as a bridge between a SPI interface and an I²C-bus. It allows an SPI master device to communicate with I²C-bus target devices. The SPI interface supports Mode 3 of the SPI specification and can operate up to 1.2 Mbit/s.

6.1 Internal registers

SC18IS604 provides internal registers for monitoring and control. These registers are shown in Table 4. Register functions are more fully described in the following paragraphs.

Table 4. Internal registers summary

Register address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Default value
0x00	IOConfig	IO3.1	IO3.0	IO2.1	IO2.0	IO1.1	IO1.0	IO0.1	IO0.0	R/W	0x00
0x01	IOState	0	0	0	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	R/W	0xXX
0x02	I2CClock	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0	R/W	0x19
0x03	I2CTO	TO6	TO5	TO4	TO3	TO2	TO1	TO0	TE	R/W	0x00
0x04	I2CStat	1	1	1	1	I2CSTAT3	I2CSTAT2	I2CSTAT1	I2CSTAT0	R	0x00
0x05	I2CAdr	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	X	R/W	0x00

6.2 Register descriptions

6.2.1 Programmable IO port configuration register (IOConfig)

Pins GPIO0 to GPIO3 may be configured by software to one of three types. These are: push-pull, open-drain, and input-only. Two configuration bits per pin, located in the IOConfig register, select the IO type for each pin. Each pin has Schmitt-triggered input that also has a glitch suppression circuit. IO4 is input and is not user-configurable.

Table 5 shows the configurations for the programmable I/O pins. IOx.1 and IOx.0 correspond to GPIOx.

Table 5. Pin configurations

IOx.1	IOx.0	Pin configuration
0	0	input-only configuration
0	1	input-only configuration
1	0	push-pull output configuration
1	1	open-drain output configuration

6.2.1.1 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the pin when the pin latch contains a logic 0. To be used as a logic output, a pin configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

The open-drain pin configuration is shown in Figure 3.

An open-drain pin has a Schmitt-triggered input that also has a glitch suppression circuit.

Device uses a pseudo open-drain mode. The pin cannot be pulled up above V_{DD}. The pins are not 5 V tolerant when V_{DD} is grounded.

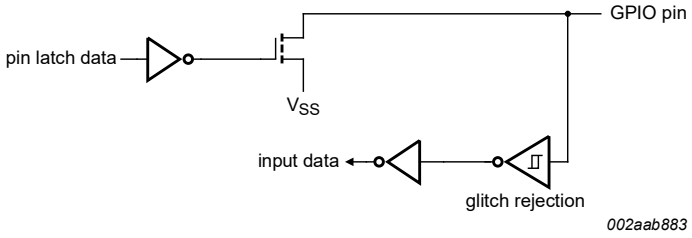


Figure 3. Open-drain output configuration

6.2.1.2 Input-only configuration

The input-only pin configuration is shown in Figure 4. It is a Schmitt-triggered input that also has a glitch suppression circuit.

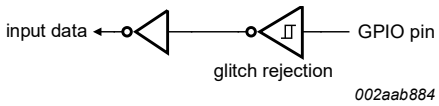


Figure 4. Input-only configuration

6.2.1.3 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as the open-drain output mode, but provides a continuous strong pull-up when the pin latch contains a logic 1. The push-pull mode may be used when more source current is needed from a pin output.

The push-pull pin configuration is shown in Figure 5.

A push-pull pin has a Schmitt-triggered input that also has a glitch suppression circuit.

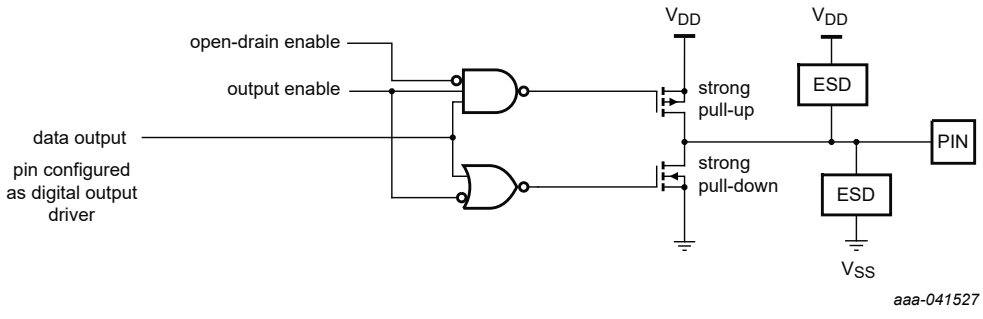


Figure 5. Push-pull output configuration

6.2.2 I/O pins state register (IOState)

When read, this register returns the actual state of all programmable I/O pins. When written, each register bit will be transferred to the corresponding I/O pin programmed as output.

Table 6. IOState - I/O pins state register (address 0x01) bit description

Bit	Symbol	Description
7:6	-	reserved
5	-	Set the logic level on the output pins. Write to this register: logic 0 = set output pin to zero logic 1 = set output pin to one A read from this register returns states of all pins.
4	GPIO4 [1]	
3	GPIO3	
2	GPIO2	
1	GPIO1	
0	GPIO0	

[1] GPIO4 is input only, write to it has no effect.

6.2.3 I²C-bus address register (I2CAdr)

The contents of the register represents the device's own I²C-bus address. The most significant bit corresponds to the first bit received from the I²C-bus after a START condition. The least significant bit is not used, but should be programmed with a '0'.

I2CAdr is not needed for device operation, but should be configured so that its address does not conflict with an I²C-bus device address used by the bus controller.

6.2.4 I²C-bus clock rates register (I2CClk)

This register determines the I²C-bus clock frequency. Various clock rates are shown in Table 7 for SC18IS604. The frequency can be determined using Equation 1:

$$I2C\text{-}busclock\,frequency = \frac{15000000}{8 \times I2CClk} \quad (1)$$

Table 7. I²C-bus clock frequency

I2CClk (decimal)	I²C-bus clock frequency
5 (minimum)	375 kHz
7	268 kHz
9	208 kHz
19	99 kHz
255 (maximum)	7.4 kHz

6.2.5 I²C-bus timeout register (I2CTO)

The timeout register is used to determine the maximum time that the I²C-bus controller is allowed to complete a transfer before setting an I²C-bus timeout interrupt.

Table 8. I2CTO - I²C-bus timeout register (address 0x04) bit description

Bit	Symbol	Description
7:1	TO[7:1]	timeout value

Table 8. I2CTO - I²C-bus timeout register (address 0x04) bit description...*continued*

Bit	Symbol	Description
0	TE	Enable/disable timeout function logic 0 = disable logic 1 = enable

The least significant bit of I2CTO (TE bit) is used as a timeout enable/disable. A logic 1 will enable the timeout function.

The timeout can be computed by the following equation:

$$timeout = \frac{(I2CClock+1)}{15000000} \times \left((1 + I2CTO[7:1]) \times 512 \right)$$

Decimal value for I2CClock is from Section 6.2.4 "I2C-bus clock rates register (I2CClk)"

The timeout value is an approximate value.

In the case of arbitration loss, SC18IS604 transmits a START condition when the bus becomes free unless the timeout condition is reached. If the timeout condition is reached, an interrupt is generated on the $\overline{INT}$ pin. The 'I²C-bus timeout' status can be read in I2CStat.

6.2.6 I²C-bus status register (I2CStat)

This register reports the results of I²C-bus transmit and receive transaction between SC18IS604 and an I²C-bus target device.

Table 9. I²C-bus status

Register value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I²C-bus status description
0xF0	1	1	1	1	0	0	0	0	Transmission successful. SC18IS604 has successfully completed an I²C-bus read or write transaction. An interrupt is generated on $\overline{INT}$. This is also the default status after reset. No interrupt is generated after reset.
0xF1	1	1	1	1	0	0	0	1	I²C-bus device address not acknowledged. No I²C-bus target device has acknowledged the target address that has been sent out in an I²C-bus read or write transaction. An interrupt is generated on $\overline{INT}$.
0xF2	1	1	1	1	0	0	1	0	I²C-bus device address not acknowledged. An I²C-bus target has not acknowledged the byte that has just been transmitted by SC18IS604. An interrupt is generated on $\overline{INT}$.
0xF3	1	1	1	1	0	0	1	1	I²C-bus busy. SC18IS604 is busy performing an I²C-bus transaction, no new transaction should be initiated by the host. No interrupt is generated.

Table 9. I²C-bus status...*continued*

Register value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	I²C-bus status description
0xF8	1	1	1	1	1	0	0	0	I²C-bus timeout (see Section 6.2.5 "I2C-bus timeout register (I2CTO)"). SC18IS604 has started an I²C-bus transaction that has taken longer than the time programmed in I2CTO register. This could happen after a period of unsuccessful arbitration or when an I²C-bus target is (continuously) pulling the SCL clock LOW. An interrupt is generated on $\overline{INT}$.)
0xF9	1	1	1	1	1	0	0	1	I²C-bus invalid data count. The number of bytes specified in a read or write command to SC18IS604. An interrupt is generated on $\overline{INT}$.

6.3 I²C-bus serial interface

I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between controllers and targets
- Multi-controller bus (no central controller)
- Arbitration between simultaneously transmitting controllers without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 6. SC18IS604 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz. (Refer to *UM10204, "I²C-bus specification and user manual"*.)

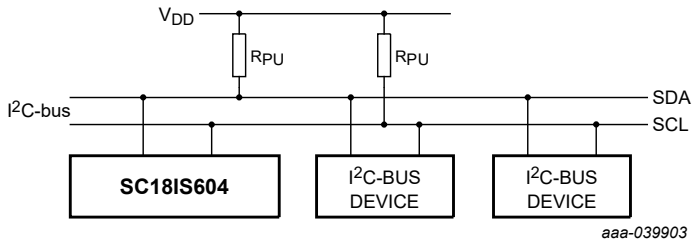


Figure 6. I²C-bus configuration

6.4 Serial Peripheral Interface (SPI)

The host communicates with SC18IS604 via the SPI interface. SC18IS604 operates in Slave mode up to 1.2 MHz.

The SPI interface has four pins: SCLK, MOSI, MISO, and $\overline{CS}$.

- **SCLK**, **MOSI** and **MISO** are typically tied together between two or more SPI devices. Data flows from the master to SC18IS604 on the MOSI (Master Out Slave In) pin and

flows from SC18IS604 to the master on the MISO (Master In Slave Out) pin. The SCLK signal is an input to SC18IS604.

- **$\overline{CS}$** is the slave select pin. In a typical configuration, an SPI master selects one SPI device as the current slave. An SPI slave device uses its $\overline{CS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 7.

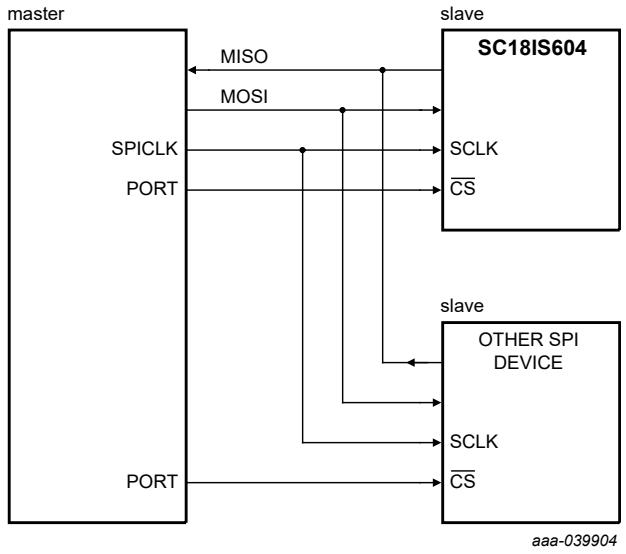


Figure 7. SPI single master multiple slaves configuration

6.5 SPI message format

6.5.1 Write N bytes to I²C-bus target device

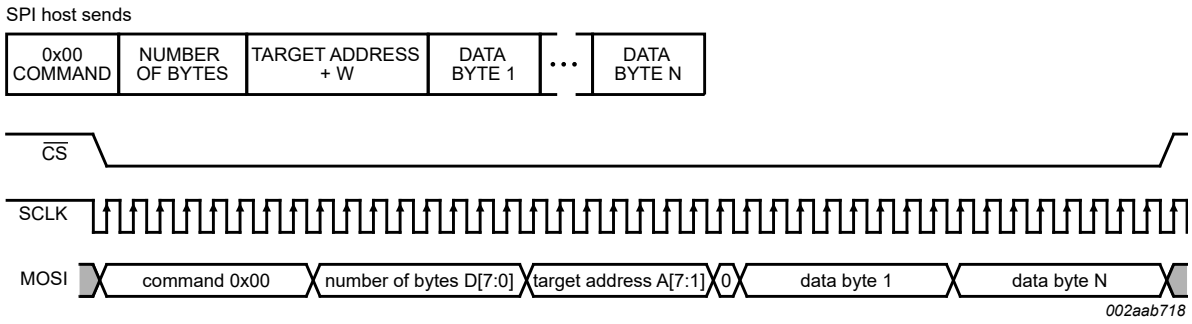


Figure 8. Write N bytes to I²C-bus target device

The SPI host issues the write command by sending a 0x00 command followed by the total number of bytes (maximum 255 bytes excluding the address) to send and an I²C-bus target device address followed by I²C-bus data bytes, beginning with the first byte (data byte 1) and ending with the last byte (data byte N). Once the SPI host issues this command, SC18IS604 will access the I²C-bus target device and start sending the I²C-bus data bytes.

When the I²C-bus write transaction has successfully finished, and interrupt is generated on the $\overline{INT}$ pin, and the 'transaction completed' status can be read in I2CStat.

Note that the third byte sent by the host is the device I²C-bus target address. SC18IS604 will ignore the least significant bit so a write will always be performed even if the least significant bit is a '1'.

6.5.2 Read N bytes from I²C-bus target device

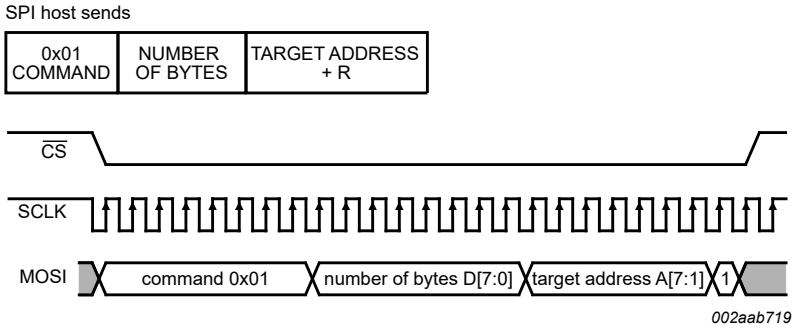


Figure 9. Read N bytes from I²C-bus target device

Once the host issues this command, SC18IS604 will start an I²C-bus read transaction on the I²C-bus to the specified target address. Once the data is received, SC18IS604 will place this data in the receiver buffer, and will generate an interrupt on the $\overline{INT}$ pin. The 'transaction completed' status can be read in the I2CStat. Note that the data is not returned until a Read Buffer command is performed (see Section 6.5.4).

Note that the third byte sent by the host is the device target address. SC18IS604 will ignore the least significant bit so a read will always be performed even if the least significant bit is a '0'. The maximum number of bytes to be read is 255.

6.5.3 I²C-bus read after write

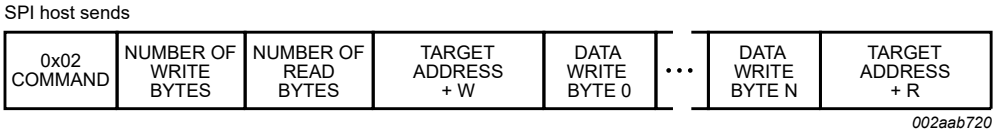


Figure 10. I²C-bus read after write

Once the host issues this command, SC18IS604 will start a write transaction on the I²C-bus to the specified target address. Once the data is written, SC18IS604 will read data from the specified target, place the data in the Receiver Buffer and generate an interrupt on the $\overline{INT}$ pin. The 'transaction completed' status can be read in I2CStat. Note that the data is not returned until a 'Read Buffer' command is performed.

6.5.4 Read buffer

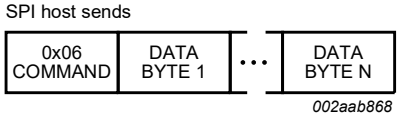


Figure 11. Read buffer

When the host issues a Read Buffer command, SC18IS604 will return the data in the Read Buffer on the MISO pin. Note that the Read Buffer will be overwritten if an additional 'Read N bytes' or a 'Read after write' command is executed before the Read Buffer command.

6.5.5 I²C-bus write after write

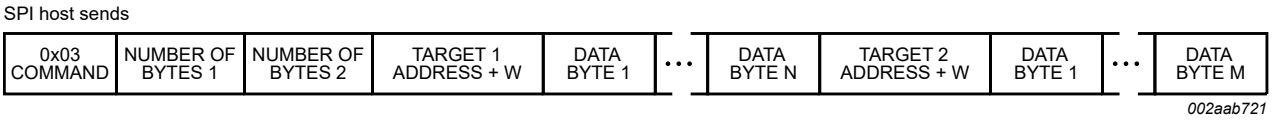


Figure 12. Write after write

When the host issues this command, SC18IS604 will first write N data bytes to the I²C-bus target 1 device followed by a write of M data bytes to the I²C-bus target 2 device.

6.5.6 SPI configuration

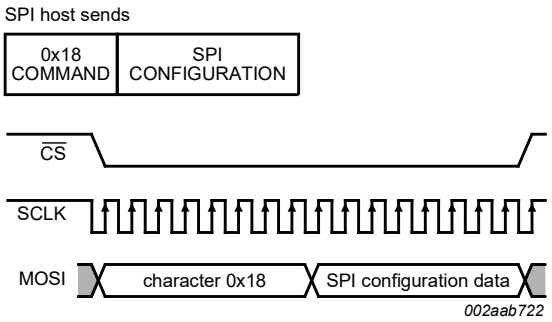


Figure 13. SPI configuration

Table 10. SPI configuration

SPI configuration	Data order
0x81	LSB first
0x42	MSB first (default)

The SPI configuration command can be used to change the order in which the bits of SPI data byte are sent on the SPI bus. In the LSB first configuration (SPI configuration data is 0x81), bit 0 is the first bit sent of any SPI byte. In MSB first (SPI configuration data is 0x42), bit 7 is the first bit sent. Table 10 shows the two possible configurations that can be programmed.

6.5.7 Write to SC18IS604 internal registers

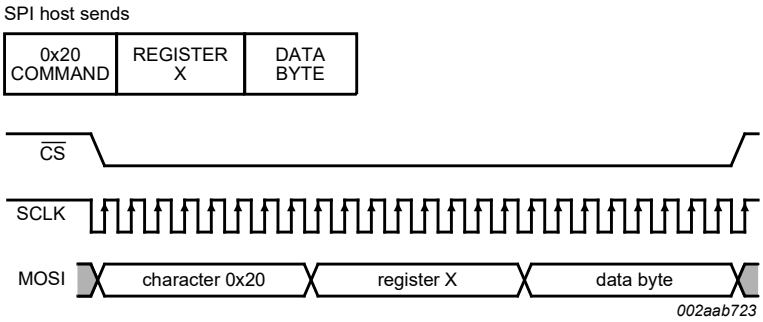


Figure 14. Write to SC18IS604 internal registers

A Write Register function is initiated by sending a 0x20 command followed by an internal register address to be written (see Section 6.1). The register data byte follows the register address. Only one register can be accessed in a single transaction. There is no auto-incrementing of the register address.

6.5.8 Read from SC18IS604 internal register

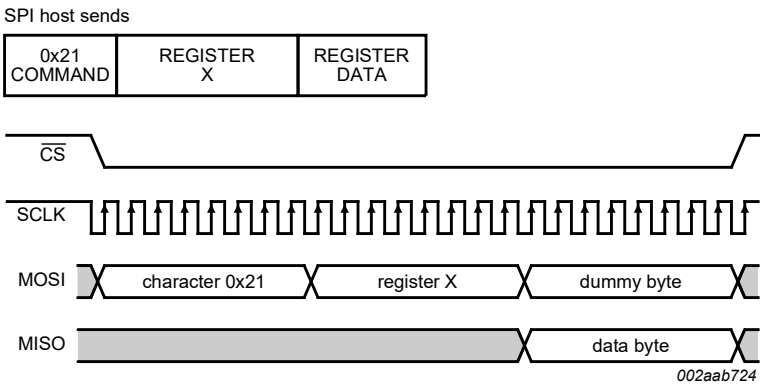


Figure 15. Read from SC18IS604 internal register

A Read Register function is initiated by sending a 0x21 command followed by an internal register address to be read (see Section 6.1) and a dummy byte. The data byte of the read register is returned by SC18IS604 on the MISO pin. Only one register can be accessed in a single transaction. There is no auto-incrementing of the register address.

Note that write and read from internal registers are processed immediately as soon as SC18IS604 determines the intended register.

6.5.9 Deep Power-down mode

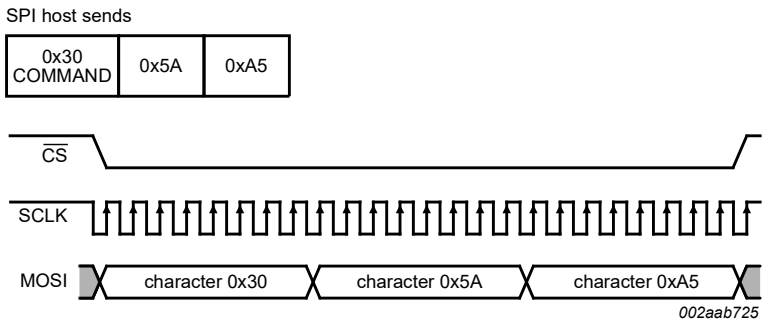


Figure 16. Deep Power-down mode

SC18IS604 can be placed in a low-power mode where the internal oscillator is stopped and it will no longer respond to SPI messages. Enter the Power-down mode by sending the power-down command (0x30) followed by the two defined bytes, which are 0x5A followed by 0xA5. If the exact message is not received, the device will not enter the power-down state.

$\overline{CS}$ should be placed in a HIGH state after sending the Deep Power-down mode sequence. To exit the power-down state, $\overline{CS}$ should be brought LOW. After leaving the power-down state, $\overline{CS}$ can once again be used as the chip selection function.

6.5.10 Read version function ID

A new command 0xFE was included with SC18IS604 as a diagnostic tool when bringing up the bridge to verify SPI parameters are correct. This command places a version string in the SPI read buffer. The string contains the part number and a version string. The interrupt pin is set and the version string can be read with command 0x06. The string is in the form “SC18IS604 1.0.0”

The total length is 16 bytes and includes a 00h null terminator. Values in the read buffer past the null terminator remain from the previous operation. The example above yields these hex values in the first 16 locations in the read buffer: 0x53 0x43 0x31 0x38 0x49 0x53 0x36 0x30 0x34 0x20 0x31 0x2e 0x30 0x2e 0x30 0x00

7 Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1] [2]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.5	+4.6	V
$T_{amb(bias)}$	bias ambient temperature	operating		-55	+150	°C
T_{stg}	storage temperature			-65	+150	°C
V_I	input voltage	5 V tolerant I/O pins; $V_{DD} \geq 1.71$ V	[3] [4]	-0.5	+5.4	V
		3 V tolerant I/O - all pins	[5]	-0.5	+3.6	V
$I_{OH(I/O)}$	HIGH-level output current per input/output pin			-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin			-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current			-	120	mA
P_{tot}/pack	total power dissipation per package		[6]	-	1.5	W

[1] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
[2] Parameters are valid over the operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
[3] Applies to all 5 V tolerant I/O pins except the 3 V tolerant pin MISO
[4] Including the voltage on outputs in 3-state mode.
[5] V_{DD} present or not present.
[6] Based on package heat transfer, not device power consumption.

8 Static characteristics

Table 12. Static characteristics

V_{DD} = 1.71 V to 3.6 V; T_{amb} = -40 °C to +105 °C, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
VDD	supply voltage			1.71		3.6	V
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.3 V		-	2.1	4.0	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.3 V		-	1.3	3.4	mA
$I_{DD(tpd)}$	total Power-down mode supply current	V_{DD} = 3.3 V		-	6	75	µA
$V_{th(HL)}$	HIGH-LOW threshold voltage	Schmitt trigger input		$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	Schmitt trigger input		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 2.5 V ≤ V_{DD} ≤ 3.6 V		-		0.5	V
		I_{OL} = 3 mA; 1.71 V ≤ V_{DD} ≤ 2.5 V		-		0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V ≤ V_{DD} ≤ 3.6 V		V_{DD} - 0.4	-	-	V
		I_{OH} = 3 mA; 1.71 V ≤ V_{DD} ≤ 2.5 V		V_{DD} - 0.5		-	V

Table 12. Static characteristics...*continued*

V_{DD} = 1.71 V to 3.6 V; T_{amb} = -40 °C to +105 °C, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
C_{ig}	input capacitance at gate		[2]	-	-	15	pF
I_{IL}	LOW-level input current	logical 0; V_I = 0.4 V		-	-	-80	µA
I_{LI}	input leakage current	all ports; $V_I = V_{IL}$ or V_{IH}	[3]	-	-	±10	µA
I_{THL}	HIGH-LOW transition current	all ports; logical 1-to-0; V_I = 2.0 V at V_{DD} = 3.6 V		-30	-	-450	µA
I_{pu}	pull-up current	V_I = 0 V;	[4]				µA
		2.0 V ≤ V_{DD} ≤ 3.6 V		10	50	90	µA
		1.71 V ≤ V_{DD} ≤ 2.0 V		7	50	85	µA
		$V_{DD} < V_I < 5$ V		0	0	0	µA

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.
[2] Pin capacitance is characterized but not tested.
[3] Measured with pins in high-impedance mode.
[4] Pull-up current measured across the weak pull-up resistor

9 Dynamic characteristics

Table 13. Dynamic characteristics

V_{DD} = 1.71 V to 3.6 V; T_{amb} = -40 °C to +105 °C, unless otherwise specified [1]

Symbol	Parameter	Conditions		Min	Max	Unit
Glitch filter						
t_{gr}	glitch rejection time	$\overline{\text{RESET}}$ pin	[2]	-	20	ns
t_{sa}	signal acceptance time	$\overline{\text{RESET}}$ pin		125	-	ns
		any pin except $\overline{\text{RESET}}$		50	-	ns
SPI slave interface						
t_{DS}	data set-up time	1.71 V ≤ V_{DD} ≤ 3.6 V		10	-	ns
t_{DH}	data hold time	1.71 V ≤ V_{DD} ≤ 3.6 V		7	-	ns
$t_{v(Q)}$	data output vallid time	3.0 V ≤ V_{DD} ≤ 3.6 V		0	28	ns
		1.71 V ≤ V_{DD} ≤ 3.0 V		0	32	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 1.2 MHz, but are guaranteed to operate down to 0 Hz.
[2] SCL and SDA do not have glitch suppression circuits.

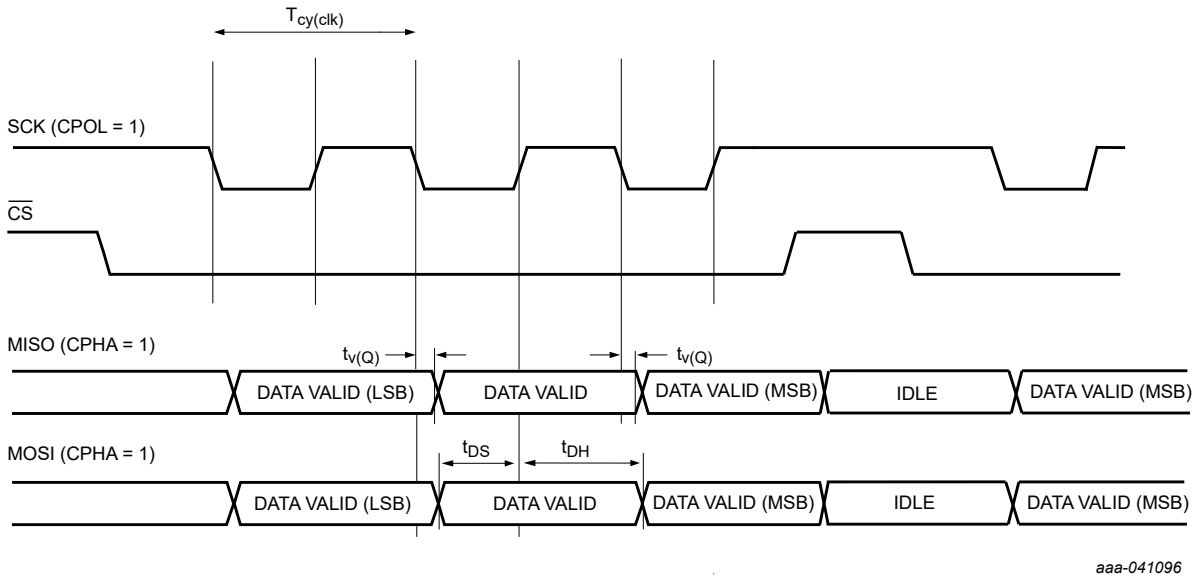


Figure 17. SPI slave timing (Mode 3)

Table 14. Additional SPI AC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{SPICLKW}$	SPICLK HIGH time	between two SPI bytes		8	-	-	µs
t_{CSW}	$\overline{CS}$ HIGH time	between two SPI transactions		0.4	-	-	µs
$t_{SPILAG1}$	SPI enable lag time 1	in a SPI to I²C-bus transaction		0.4	-	-	µs
t_d	delay time	from last SCLK pulse to SDA LOW in a SPI to I²C-bus transaction		35	-	-	µs

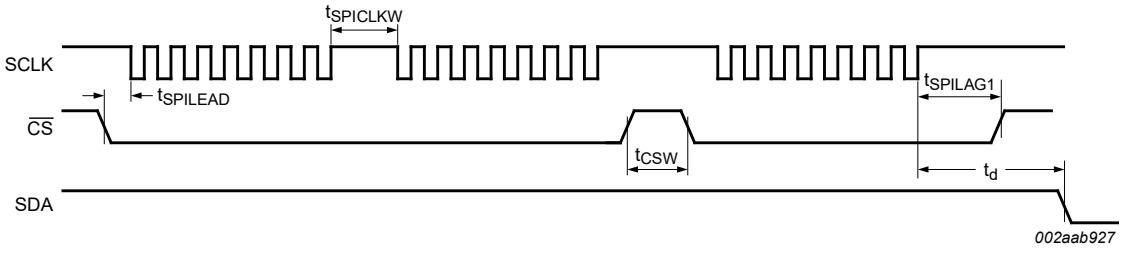


Figure 18. SPI to I²C-bus timing diagram

Table 15. I²C-bus timing characteristics

All the timing limits are valid within the operating supply voltage and ambient temperature range; V_{DD} = 1.71 V to 3.6 V; T_{amb} = -40 °C to +105 °C; and refer to V_{IL} and V_{IH} with an input voltage of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions		Standard mode I²C-bus		Fast mode I²C-bus		Unit
				Min	Max	Min	Max	
f_{SCL}	SCL clock frequency			0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition			4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition			4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition			4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time			0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time			-	0.6	-	0.6	µs
$t_{VD;DAT}$	data valid time	LOW-level		-	0.6	-	0.6	µs
		HIGH-level		-	0.6	-	0.6	µs
$t_{SU;DAT}$	data set-up time			250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock			4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock			4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals			-	0.3	-	0.3	µs
t_r	rise time of both SDA and SCL signals			-	1	-	0.3	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter			-	50	-	50	ns

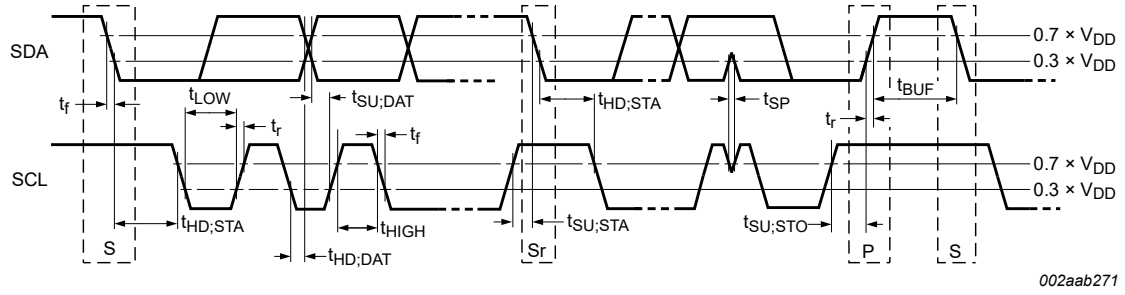
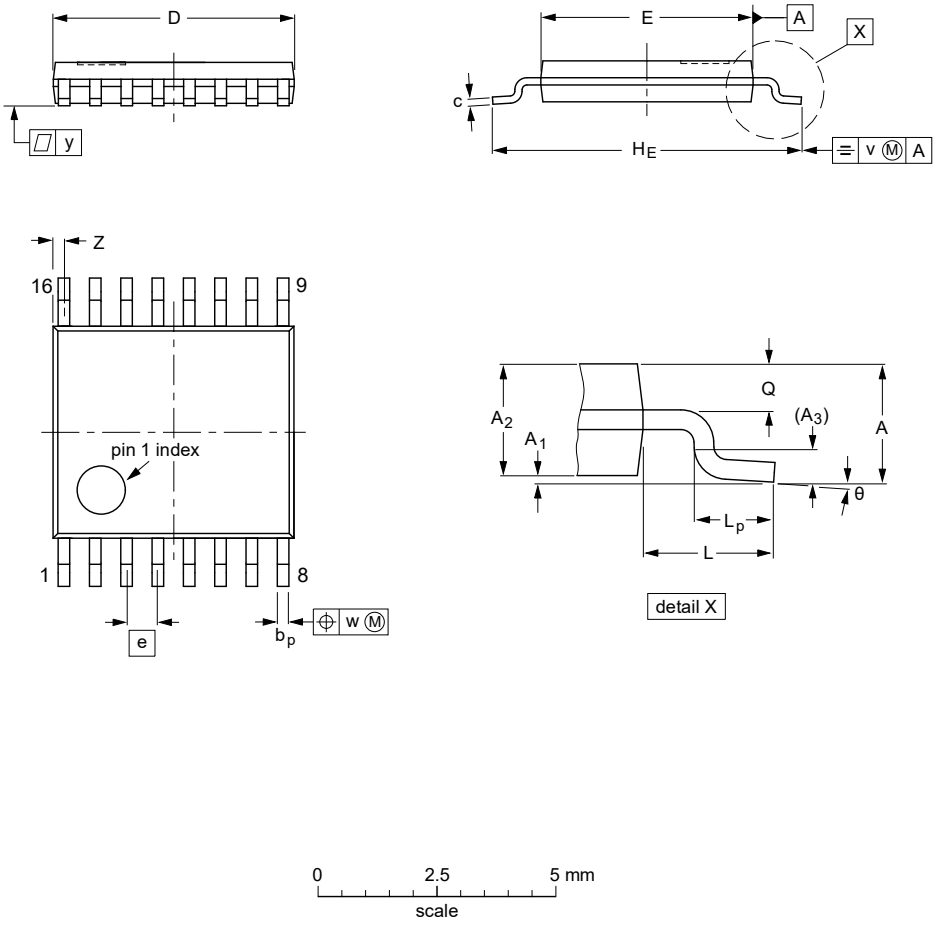


Figure 19. I²C-bus timing

10 Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

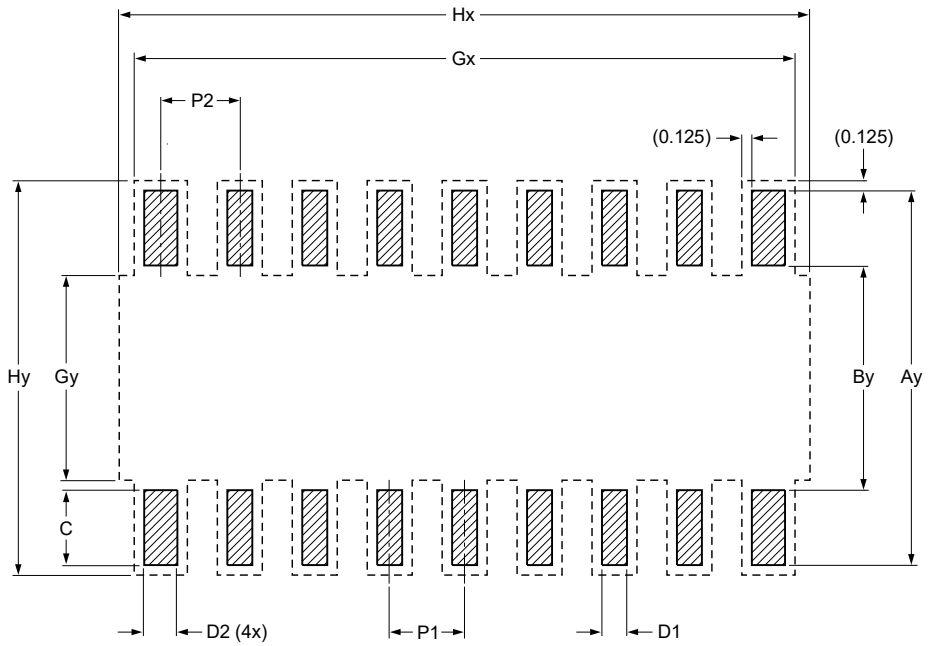
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Figure 20. Package outline SOT403-1 (TSSOP16)

11 PCB layout

Footprint information for reflow soldering of TSSOP16 package **SOT403-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Figure 21. SOT403-1 (TSSOP16) footprint information for reflow soldering

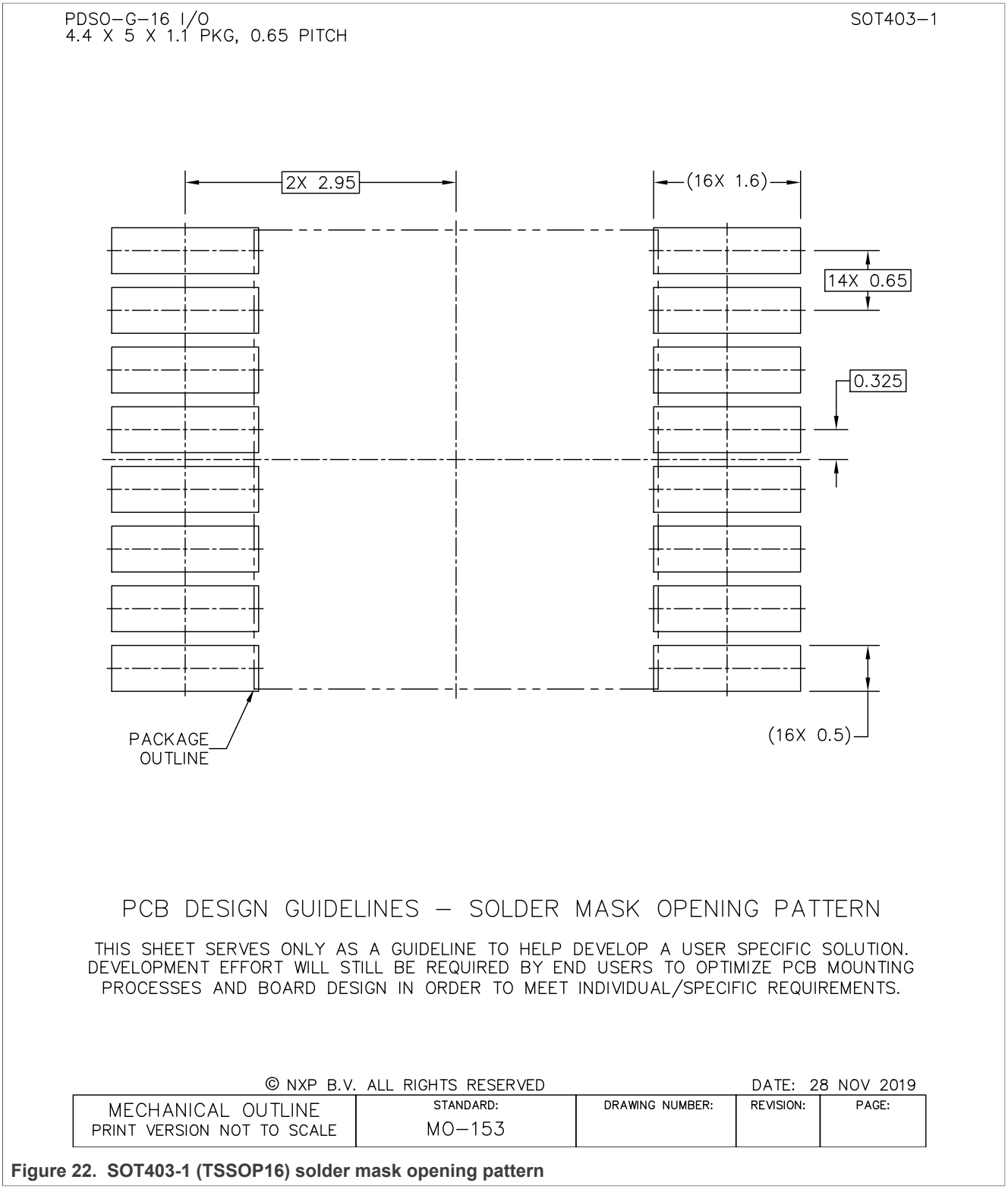


Figure 22. SOT403-1 (TSSOP16) solder mask opening pattern

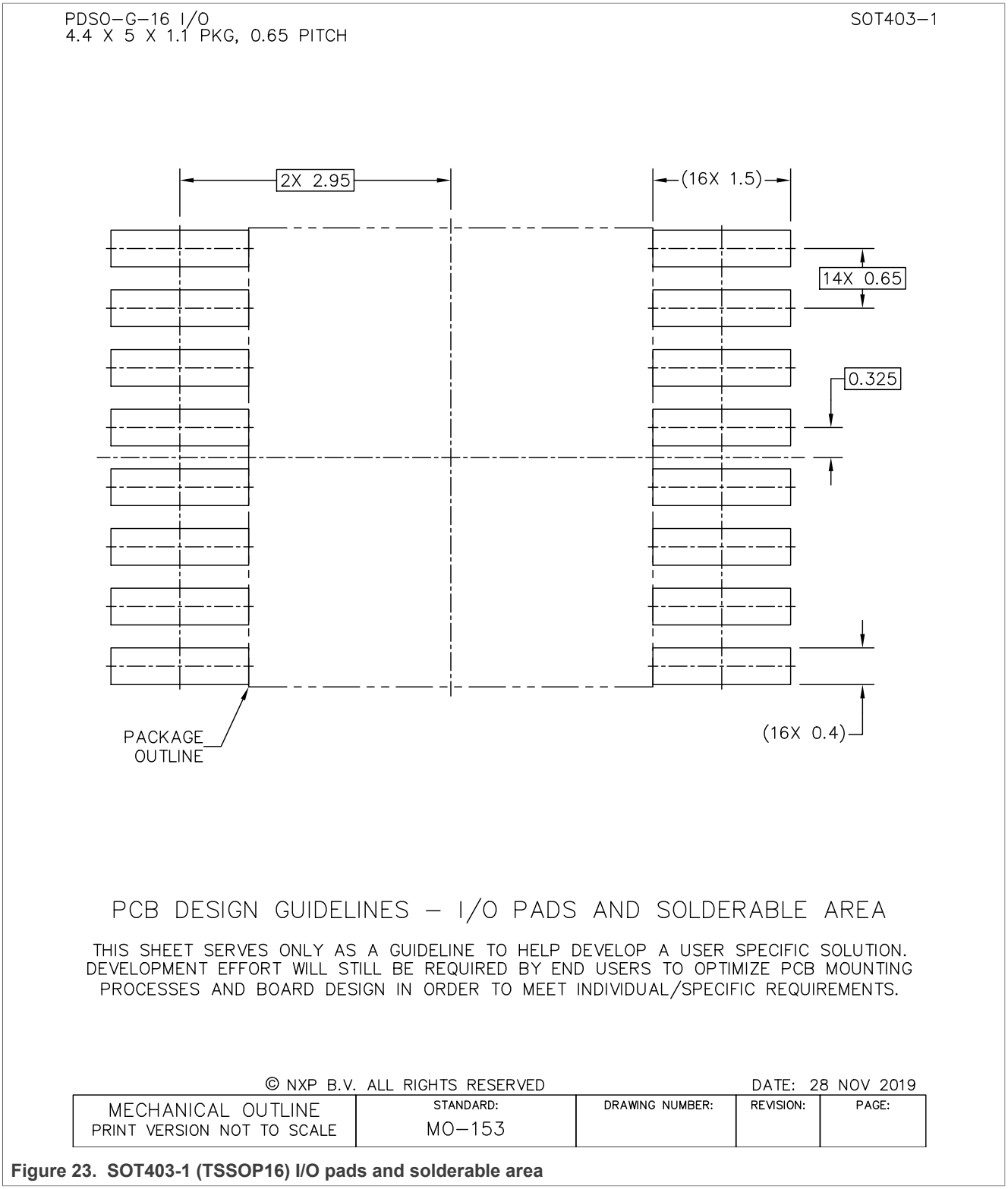


Figure 23. SOT403-1 (TSSOP16) I/O pads and solderable area

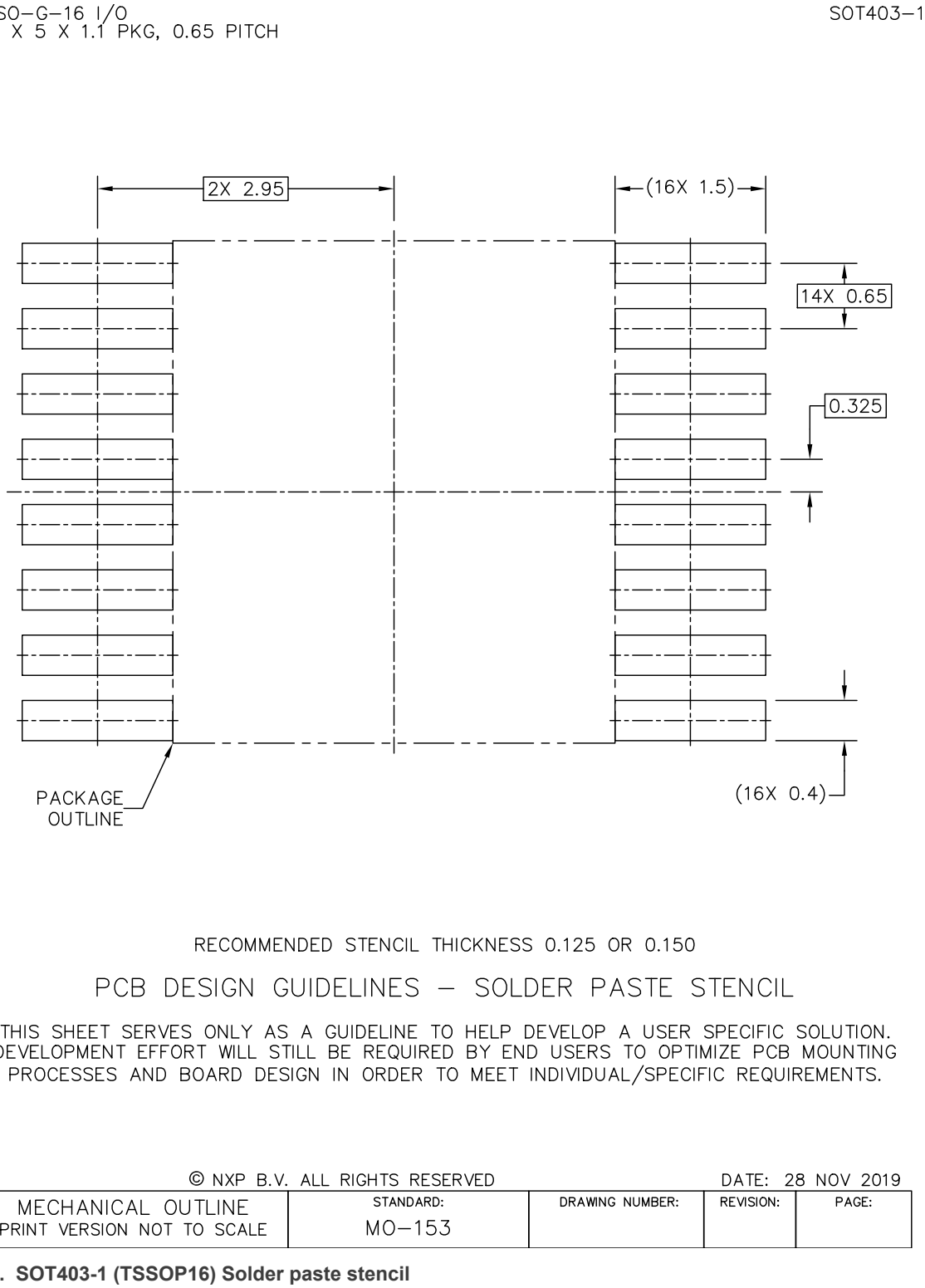


Figure 24. SOT403-1 (TSSOP16) Solder paste stencil

12 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and Table 17

Table 16. SnPb eutectic process (from J-STD-020D)

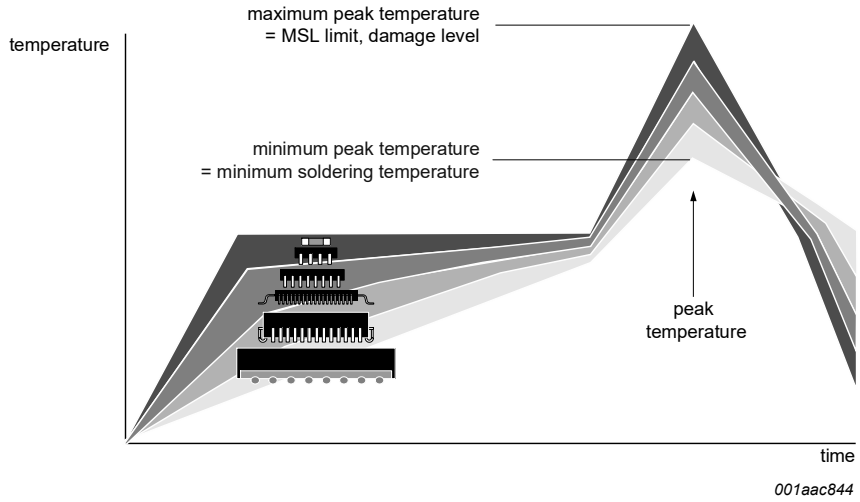
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.



MSL: Moisture Sensitivity Level

Figure 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13 Abbreviations

Table 18. Abbreviations

Acronym	Description
ASCII	American Standard Code for Information Interchange
CPU	Central Processing Unit
GPIO	General Purpose Input/Output
I/O	Input/Output
I^2C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

14 Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SC18IS604 v.1.0	20210922	Product data sheet	-	-

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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