

### POWER MANAGEMENT

#### Description

The SC2441 is a high-frequency triple output switching regulator controller. It consists of a dual out-of-phase synchronous step-down PWM controller with high-current output gate drives and a 1.7A integrated step-up switching regulator.

The dual-phase step-down controller of the SC2441 can be configured to provide two individually controlled and regulated outputs or a single output with shared current in each phase. The buck controller can operate from an input voltage of at least 4.72V or they can run off a supply generated locally with the integrated boost regulator. This makes the SC2441 ideally suited for applications where a low-voltage input (3.3V, 2.5V, or 1.8V) is to be stepped down for lower voltage logic yet the input is too low to drive power MOSFET's efficiently. The boost regulator can be used to provide a third auxiliary output while generating the bias for the buck controllers.

Both the step-down controllers and the step-up regulator employ fixed frequency peak current-mode control for fast transient response. The master oscillator frequency can be programmed by the user.

Individual soft-start and overload shutdown timer are employed in each step-down controller for hiccup overload protection. In single-output configuration, the channel 1 timer controls the soft-start and overload shutdown functions of both controllers.

#### Typical Application Circuit

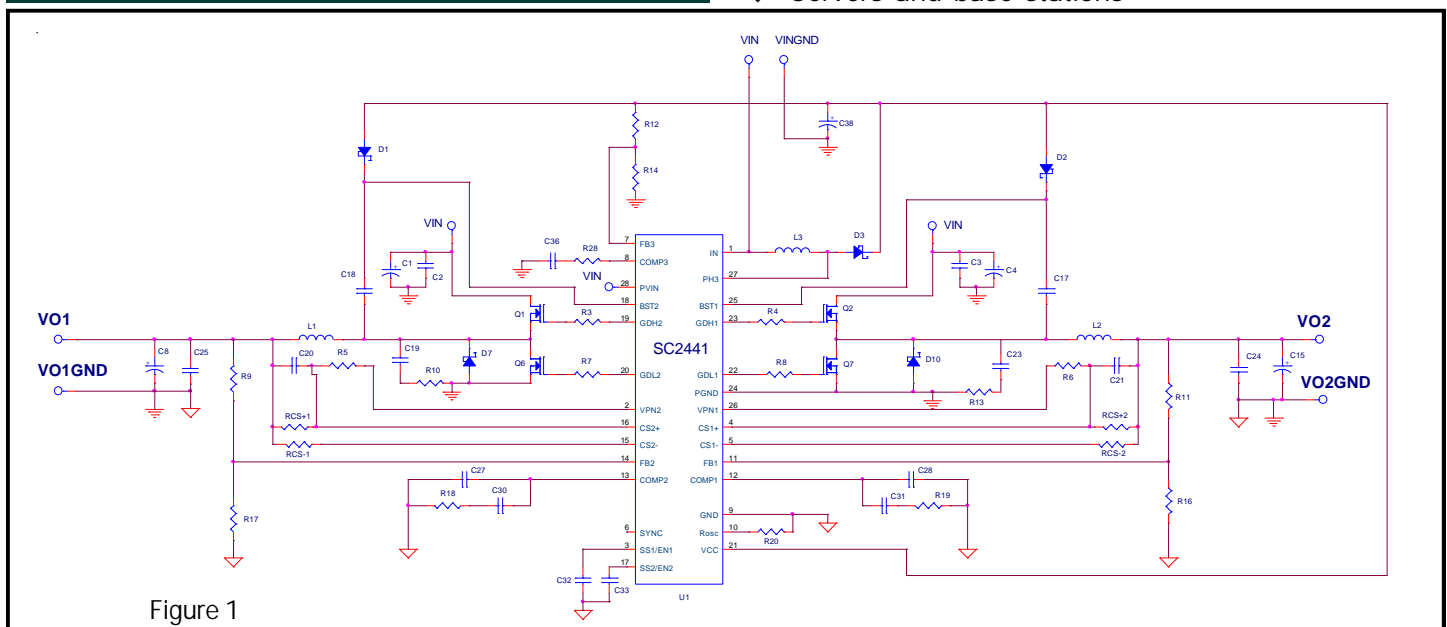


Figure 1

#### Features

2-Phase Synchronous step-down controllers

- ◆ 2-Phase Synchronous Continuous Conduction Mode For High Efficiency Step-down Converters
  - ◆ Out of Phase Operation For Low Input Current Ripples
  - ◆ Operates Up To 1MHz Per Channel
  - ◆ Configurable Dual Outputs Or 2-Phase Single Output Operation with Peak Current Mode Control
  - ◆ Excellent Current Sharing Between Phases
  - ◆ Wide Input Voltage Range: 1.8V to 15V
  - ◆ Duty Cycle Up to 90%
  - ◆ 0.5V Feedback Voltages For Low-Voltage Outputs
  - ◆ Precision 50mV Current-Limit Threshold
  - ◆ Patented Combi-sense Technique for High SNR of Current-Sensing
  - ◆ Individual Soft-Start, Overload Shutdown and Enable
- Step-up Regulator
- ◆ Wide Input Voltage Range: 1.8V to 15V
  - ◆ Operates At Twice The Individual Channel Frequency Of The Buck Controllers
  - ◆ 0.23V  $V_{CESAT}$  Switch at 1A
  - ◆ Fixed Frequency with Current-Mode Control
- Common Features
- ◆ External Synchronization
  - ◆ Industrial Temperature Range

#### Applications

- ◆ Low Voltage Distributed DC-DC Converters
- ◆ Telecommunication Power Supplies
- ◆ Servers and base stations

**POWER MANAGEMENT**
**Absolute Maximum Rating**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum Ratings	Units
Input Voltages	$V_{IN}, V_{PVIN}$	-0.3 to 20	V
Supply Voltage For Step-Down Controller	$V_{CC}$	-0.3 to 20	V
High-Side Driver Supply Voltages	$V_{BST1}, V_{BST2}$	-0.3 to 20	V
FB1, FB2 Voltage	$V_{FB1}, V_{FB2}$	-0.3 to 20	V
COMP1, COMP2 Voltages	$V_{COMP1}, V_{COMP2}$	-0.3 to 4.5	V
CS1(+), CS1(-), CS2(+), and CS2(-) Voltages	$V_{CS1(+)}, V_{CS1(-)}, V_{CS2(+)}, V_{CS2(-)}$	-0.3 to 20	V
SYNC/SHDN Voltage	$V_{S/S}$	-0.3 to 20	V
ROSC Voltage	$V_{ROSC}$	-0.3 to 5	V
SS1/EN1 AND SS2/EN2 Voltages	$V_{SS1}, V_{SS2}$	-0.3 to 6	V
Peak Gate Drive Current	$I_{GDH1}, I_{GDH2}, I_{GDL1}, I_{GDL2}$	3	A
Peak VPN1 and VPN2 Output Currents	$I_{VPN1}, I_{VPN2}$	100	mA
FB3 Voltage	$V_{FB3}$	4	V
COMP3 Voltage	$V_{COMP3}$	-0.3 to 2	V
PH3 Voltage	$V_{PH3}$	-0.3 to 35	V
Ambient Temperature	$T_A$	-40 to 85	°C
Thermal Resistance Junction to Case	$\theta_{JC}$	13	°C/W
Thermal Resistance Junction to Ambient	$\theta_{JA}$	84	°C/W
Storage Temperature Range	$T_{STG}$	-60 to 150	°C
Lead Temperature (Soldering) 10 sec	$T_{LEAD}$	260	°C

**Electrical Characteristics**

Unless specified:  $V_{IN} = 2V, V_{CC} = V_{BST1} = V_{BST2} = 8V, SYNC/SHDN = 2V, R_{OSC} = 51.1k\Omega, -40^\circ C < T_A = T_J < 85^\circ C$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Undervoltage Lockout</b>						
$V_{CC}$ Start Threshold	$V_{CCTH}$	$V_{CC}$ Increasing		4.65	4.72	V
$V_{CC}$ UVLO Threshold	$V_{CCTL}$	$V_{CC}$ Decreasing	4.34	4.45		V
$V_{CC}$ Operating Current	$I_{CC}$	$V_{CC} = 8V, V_{S/S} = 2V$ $V_{CC} < V_{CCTL}, V_{S/S} = 2V$ $V_{CC} = 8V, V_{S/S} = 0V$		14 0.15 10	21 0.25 13	mA
<b>Channel 1 and 2 Error Amplifiers</b>						
Feedback Voltage	$V_{FB1}, V_{FB2}$	$V_{IN} = 3V$ $V_{CCTL} < V_{CC} < 10V$ $-40^\circ C < T_A < 85^\circ C$	0.487	0.496	0.507	V
Feedback Pin Input Bias Current	$I_{FB1}, I_{FB2}$			-160	-400	nA
Amplifier Transconductance	$G_{M1}, G_{M2}$			400		$\mu\Omega^{-1}$
Open Loop Voltage Gain	$a_{o1}, a_{o2}$			75		dB
Amplifier Unity Gain Bandwidth		(Note 1)		5		MHz
Amplifier Output Sink Current		$V_{FB1,2} = 1V, V_{COMP1,2} = 2.5V$	20	32	40	$\mu A$
Amplifier Output Source Current		$V_{FB1,2} = 0V, V_{COMP1,2} = 2.5V$	10	17	30	$\mu A$
COMP Threshold for PWM Operation		$V_{CS1(+)} = V_{CS1(-)} = 0$ $V_{CS2(+)} = V_{CS2(-)} = 0$ $-40^\circ C < T_A < 85^\circ C$	1.3	1.7	2.2	V
FB2 Voltage For 2-Phase Single Output Operation			1.55			V

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

 Unless specified:  $V_{IN} = 2V$ ,  $V_{CC} = V_{BST1} = V_{BST2} = 8V$ ,  $SYNC/\overline{SHDN} = 2V$ ,  $R_{OSC} = 51.1k\Omega$ ,  $-40^\circ C < T_A = T_J < 85^\circ C$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Oscillator</b>						
Step-down Channel Switching Frequency	$f_{OSC1}, f_{OSC2}$	$R_{OSC} = 51.1k\Omega$	470	510	550	KHz
Maximum Duty Cycle	$D_{MAX1}, D_{MAX2}$	$R_{OSC} = 51.1k\Omega$	88	90		%
Minimum Duty Cycle	$D_{MIN1}, D_{MIN2}$	$R_{OSC} = 51.1k\Omega$			0	%
SYNC/ $\overline{SHDN}$ Synchronizing Frequency		$R_{OSC} = 51.1k\Omega$ (Note 1)	1.2		2	MHz
SYNC/ $\overline{SHDN}$ Input High Voltage	$V_{S/SH}$		1.5			V
SYNC/ $\overline{SHDN}$ Input Low Voltage	$V_{S/SL}$				0.5	V
SYNC/ $\overline{SHDN}$ Input Current	$I_{S/S}$	$V_{S/S} = 0.2V$ $V_{S/S} = 2V$		50	1 100	$\mu A$
Shutdown Delay		(Note 1)		85		$\mu s$
<b>Current-Sense Amplifiers and Current-Limit Comparators</b>						
Current Limit Threshold	$V_{ILIM1}, V_{ILIM2}$	$V_{CC} = 8V$ $V_{CS1(-)} = V_{CS2(-)} = 0V$	40	48	56	mV
Current Limit Threshold	$V_{ILIM1}, V_{ILIM2}$	$V_{CC} = 8V$ $V_{CS1(-)} = V_{CS2(-)} = 5V$	40	46.5	56	mV
Positive Current-Sense Input Bias Current	$I_{CS1(+)}, I_{CS2(+)}$	$V_{CS1(+)} = V_{CS1(-)} = 0$ $V_{CS2(-)} = V_{CS2(+)} = 0$		-0.37	-1	$\mu A$
Negative Current-Sense Input Bias Current	$I_{CS1(-)}, I_{CS2(-)}$	$V_{CS1(+)} = V_{CS1(-)} = 0$ $V_{CS2(+)} = V_{CS2(-)} = 0$		-0.32	-1	$\mu A$
Minimum PWM On-time		$T_A = 25^\circ C$ , (Note 1)		180		ns
<b>Gate Drivers</b>						
High-Side Gate Drive Peak Source Current		(Note 1)		2		A
High-Side Gate Drive Peak Sink Current		(Note 1)		2		A
Low-Side Gate Drive Peak Source Current		(Note 1)		2		A
Low-Side Gate Drive Peak Sink Current		(Note 1)		2		A
Gate Drive Rise Time		$C_L = 3300pF$		30		ns
Gate Drive Fall Time		$C_L = 3300pF$		30		ns
Low-side Gate Drive to High-side Gate Drive Non-overlapping Delay		$C_L = 0$		74		ns
High-side Gate Drive to Low-side Gate Drive Non-overlapping Delay		$C_L = 0$		62		ns
<b>Soft-Start, Overload Shutoff and Enable</b>						
Soft-Start Charging Current	$I_{SS1}, I_{SS2}$	$V_{SS1} = V_{SS2} = 1.5V$		2.3		$\mu A$
Soft-Start Voltage to Enable Overload Shutoff	$V_{SSEN1}, V_{SSEN2}$	$V_{SS1}$ and $V_{SS2}$ Increasing		3.25		V
Overload Shutoff FB Threshold	$V_{FBOL1}, V_{FBOL2}$	$V_{SS1,2} = 3.8V$ $FB_1$ and $FB_2$ Decreasing	0.348	0.36	0.372	V
Soft-Start Discharge Current	$I_{SS1(DIS)}, I_{SS2(DIS)}$	$V_{FB1} = V_{FB2} = 0.3V$ $V_{SS1} = V_{SS2} = 3.8V$		1.4		$\mu A$
Soft-Start Voltage to Recover From Overload Shutoff	$V_{SSRCV1}, V_{SSRCV2}$	$V_{SS1}$ and $V_{SS2}$ Decreasing	0.29	0.47	0.63	V

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

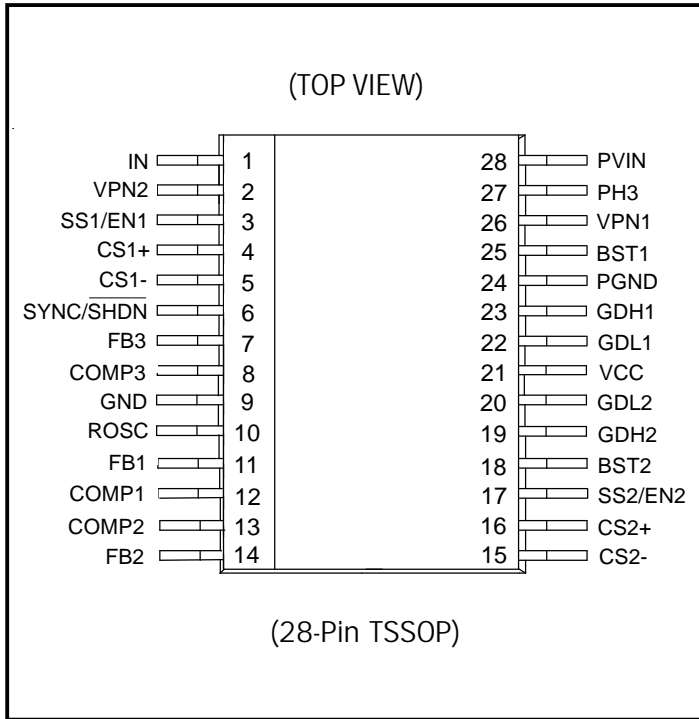
 Unless specified:  $V_{IN} = 2V$ ,  $V_{CC} = V_{BST1} = V_{BST2} = 8V$ ,  $SYNC/\overline{SHDN} = 2V$ ,  $R_{OSC} = 51.1k\Omega$ ,  $-40^{\circ}C < T_A = T_J < 85^{\circ}C$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gate Drive Disable SS/EN Voltage					0.5	V
Gate Drive Enable SS/EN Voltage			1.2			V
<b>Virtual Phase Nodes</b>						
Output High Voltage	$V_{VPN1,2H}$	$I_{VPN1}=0, I_{VPN2}=0$	$PV_{IN} - 0.05$			V
Output Low Voltage	$V_{VPN1,2L}$	$I_{VPN1}=0, I_{VPN2}=0$			20	mV
Output High Voltage	$V_{VPN1,2H}$	$I_{VPN1} = I_{VPN2} = -12mA$	$PV_{IN} - 0.22$			V
Output Low Voltage	$V_{VPN1,2L}$	$I_{VPN1} = I_{VPN2} = 12mA$			200	mV
<b>Boost Converter</b>						
$V_{IN}$ Start Threshold	$V_{INTH}$	$V_{IN}$ Increasing		1.74	1.8	V
$V_{IN}$ UVLO Threshold	$V_{INTL}$	$V_{IN}$ Decreasing	1.45	1.59		V
Feedback Pin Bias Current	$I_{FB3}$			40	250	nA
Feedback Voltage	$V_{FB3}$	$1.55V < V_{IN} < 16.5V$ $-40^{\circ}C < T_A < 85^{\circ}C$	1.225	1.250	1.275	V
Feedback Amplifier Transconductance	$G_{M3}$			180		$\mu\Omega^{-1}$
Feedback Amplifier Open-Loop Gain	$a_{o3}$			50		dB
Boost Converter Switching Frequency	$f_{OSC3}$	$R_{OSC} = 51.1k\Omega$	0.94		1.1	MHz
Maximum Switch Duty Cycle	$D_{MAX3}$		82	86		%
Boost Converter Switch Saturation Voltage	$V_{CESAT}$	$I_{SW} = 1A, T_A = 25^{\circ}C$		0.23	0.35	V
Boost Switch Leakage Current	$I_{LEAKAGE}$	$V_{SW} = 12V$			5	$\mu A$
Boost Switch Current Limit	$I_{LIMIT}$		1.7	2		A

Note 1: Guaranteed by design not tested in production.

POWER MANAGEMENT

Pin Configurations



Ordering Information

Device	Package	Temp. Range( T <sub>A</sub> )
SC2441ITSTRT <sup>(1)(2)</sup>	TSSOP-28	-40 - 85°C
SC2441EVB	Evaluation Board	

Notes:

- (1) Only available in tape and reel packaging. A reel contains 2500 devices for the TSSOP-28 package.
- (2) Lead free product.

## POWER MANAGEMENT

## Pin Descriptions

Pin	Pin Name	Pin Function
1	IN	Power Supply Voltage for the Analog Section of the Boost Converter.
2	VPN2	The Virtual Phase (Unloaded) Node of the Second Step-down Converter. Used for "Combi" current sense only. This pin is left open when sensing current with a sense resistor at the converter output.
3	SS1/EN1	An external capacitor tied to this pin sets (i) the soft-start time (ii) output overload latch off time for step-down converter 1. Pulling this pin below 0.5V shuts off the gate drivers for the first controller.
4	CS1+	The Non-inverting Input of the Current-sense Amplifier/Comparator for the Step-down Controller 1.
5	CS1-	The Inverting Input of the Current-sense Amplifier/Comparator for the Step-down Controller 1. Normally tied to the output of the converter.
6	SYNC/ $\overline{\text{SHDN}}$	Synchronization and Shutdown Input. For normal operation, tie this pin to a voltage above 1.5V. To shut-off both step-down controllers and the boost regulator, force this pin to a voltage less than 0.5V. The master oscillator can be synchronized by driving this pin with an external clock (external $f_{\text{CLK}} >$ frequency set with ROSC). The boost converter runs at the external clock frequency whereas the step-down controllers operate at half the clock frequency.
7	FB3	The Inverting Input of the Error Amplifier for the Boost Converter. FB3 is tied to an external resistive divider for output3 voltage setting.
8	COMP3	The Error Amplifier Output of the Boost Converter. This pin is used for loop compensation. Pulling this pin below 0.4V disables the step-up converter.
9	GND	Analog Signal Ground.
10	ROSC	An external resistor connected from this pin to GND sets the oscillator frequency.
11	FB1	The Inverting Input of the Error Amplifier for the Step-down Controller 1. Tie to an external resistive divider between OUTPUT1 and the ground for output voltage sensing.
12	COMP1	The Error Amplifier Output for Step-down Controller 1. This pin is used for loop compensation.
13	COMP2	The Error Amplifier Output for Step-down Controller 2. This pin is used for loop compensation.
14	FB2	The Inverting Input of the Error Amplifier for the Step-down Controller 2. Tie to an external resistive divider between output2 and the ground for output voltage sensing. Tie to IN or VCC for two-phase single output applications
15	CS2-	The Inverting Input of the Current-sense Amplifier/Comparator for the Step-down Controller 2. Normally tied to the output of the converter.
16	CS2+	The Non-inverting Input of the Current-sense Amplifier/Comparator for the Step-down Controller 2
17	SS2/EN2	An external capacitor tied to this pin sets (i) the soft-start time (ii) output overload latch off time for step-down converter 2. Pulling this pin below 0.5V shuts off the gate drivers for the second controller. Leave open for two-phase single output applications.
18	BST2	Bootstrapped Supply for the High-side Gate Drive 2. Connect to a bootstrap capacitor and an external diode as described in application information.
19	GDH2	Gate Drive Output for the High-side N-channel MOSFET of Output 2. Gate drive voltage swings from ground to VBST2.
20	GDL2	Gate Drive Output for the Low-side N-channel MOSFET of Output 2. Gate drive voltage swings from ground to VCC.

## POWER MANAGEMENT

## Pin Descriptions

21	VCC	Supply Voltage for Both Step-down Controllers and the Low-side Gate Drivers. The boost converter output is tied to VCC if VIN is not high enough to fully enhance the power MOSFET's and the boost converter provides an auxiliary supply voltage for the step-down controllers. Tie VCC to VIN if the boost converter is not needed.
22	GDL1	Gate Drive Output for the Low-side N-channel MOSFET of Output 1. Gate drive voltage swings from ground to VCC.
23	GDH1	Gate Drive Output for the High-side N-channel MOSFET of Output 1. Gate drive voltage swings from ground to VBST1.
24	PGND	Ground Supply of the High-side and the Low-side Gate Drivers of Both Step-down Controllers. It is also the emitter of the boost switch.
25	BST1	Bootstrapped Supply for the High-side Gate Drive 1. Connect to a bootstrap capacitor and an external diode as described in application information.
26	VPN1	The Virtual Phase (Unloaded) Node of the First Step-down Converter. Used for "Combi" current sense only. This pin is left open when sensing current with a sense resistor at the converter output.
27	PH3	Boost Switch Collector. Connect to a boost inductor and a rectifying diode.
28	PVIN	Power Supply Voltage for the Boost Switch and the Virtual Phase Node Drivers.

POWER MANAGEMENT

Block Diagram

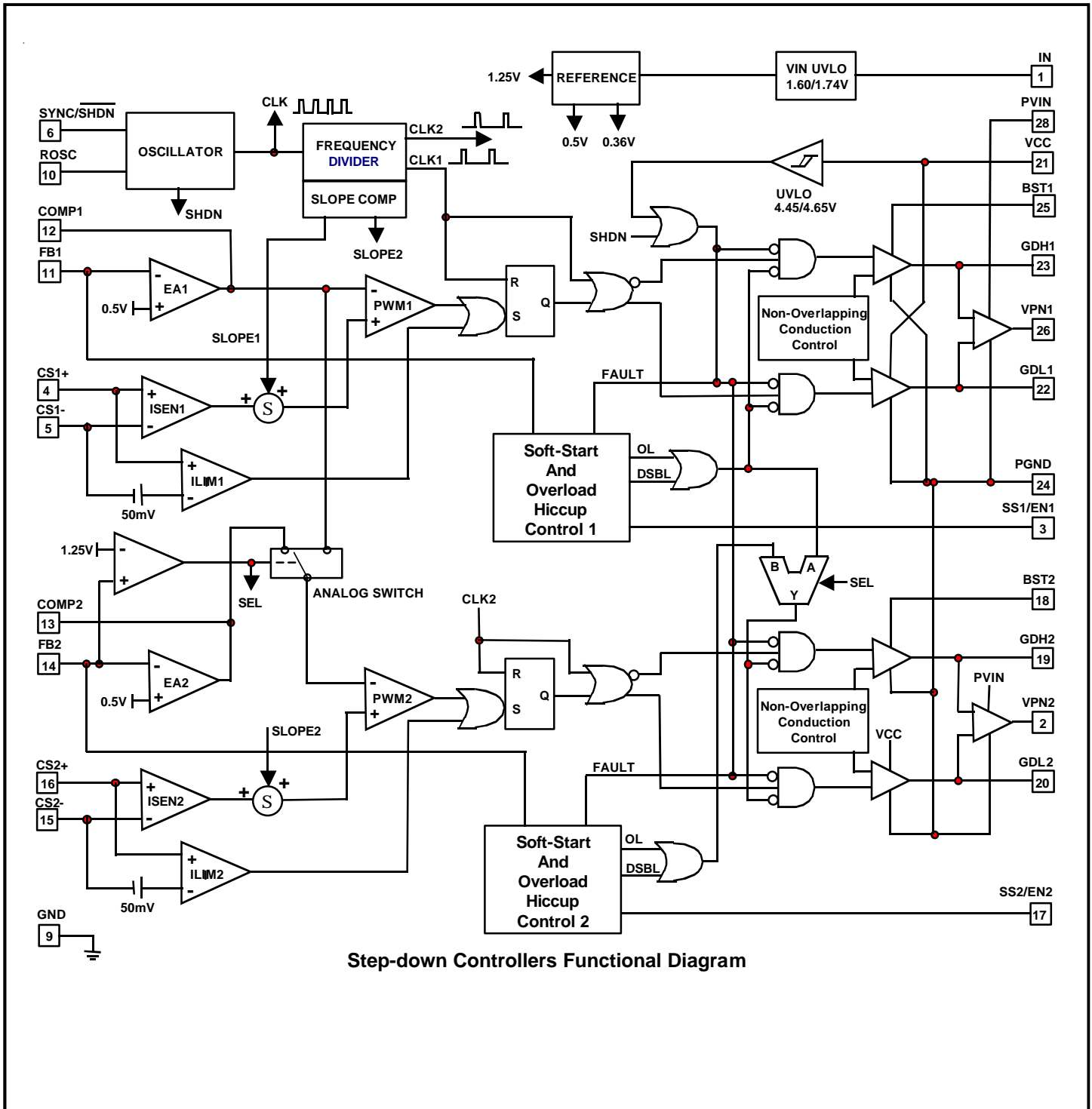


Figure 2



POWER MANAGEMENT

Block Diagram

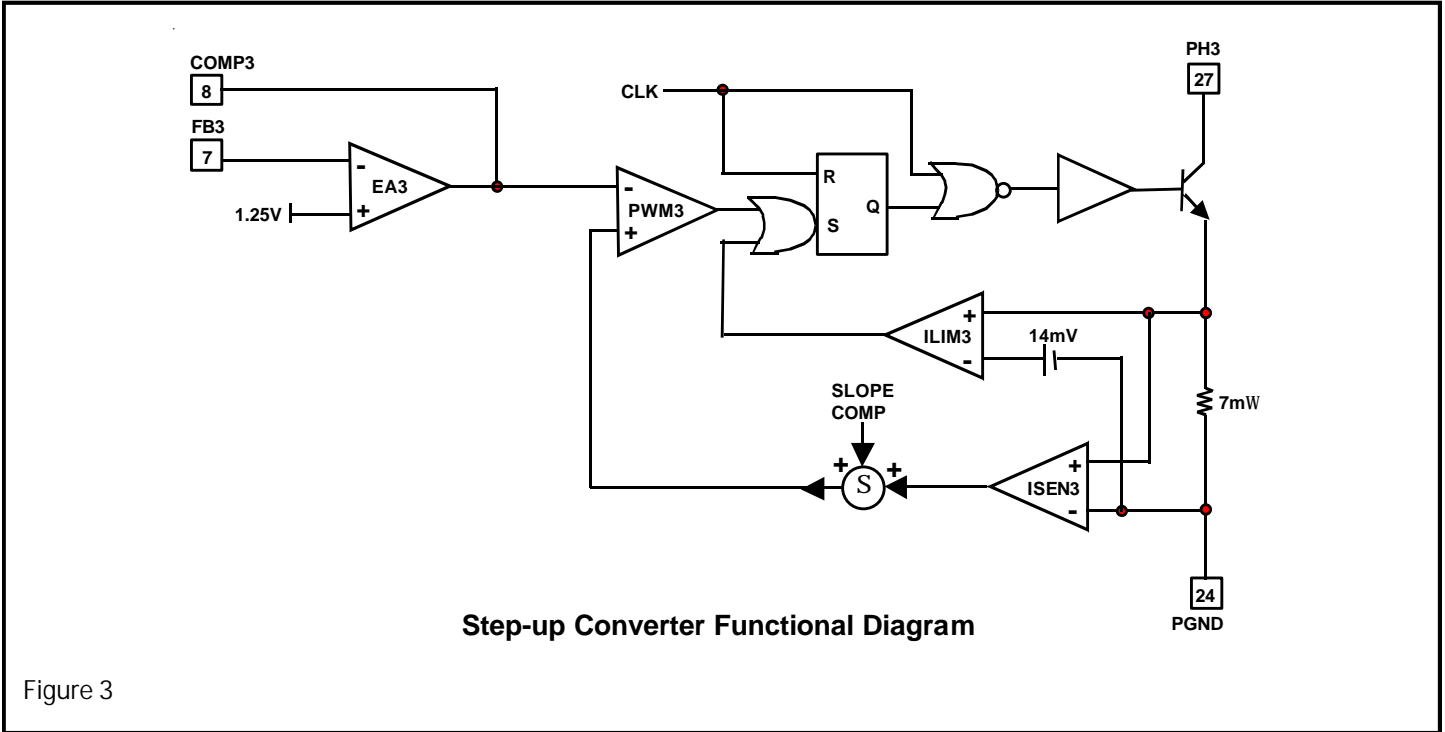


Figure 3

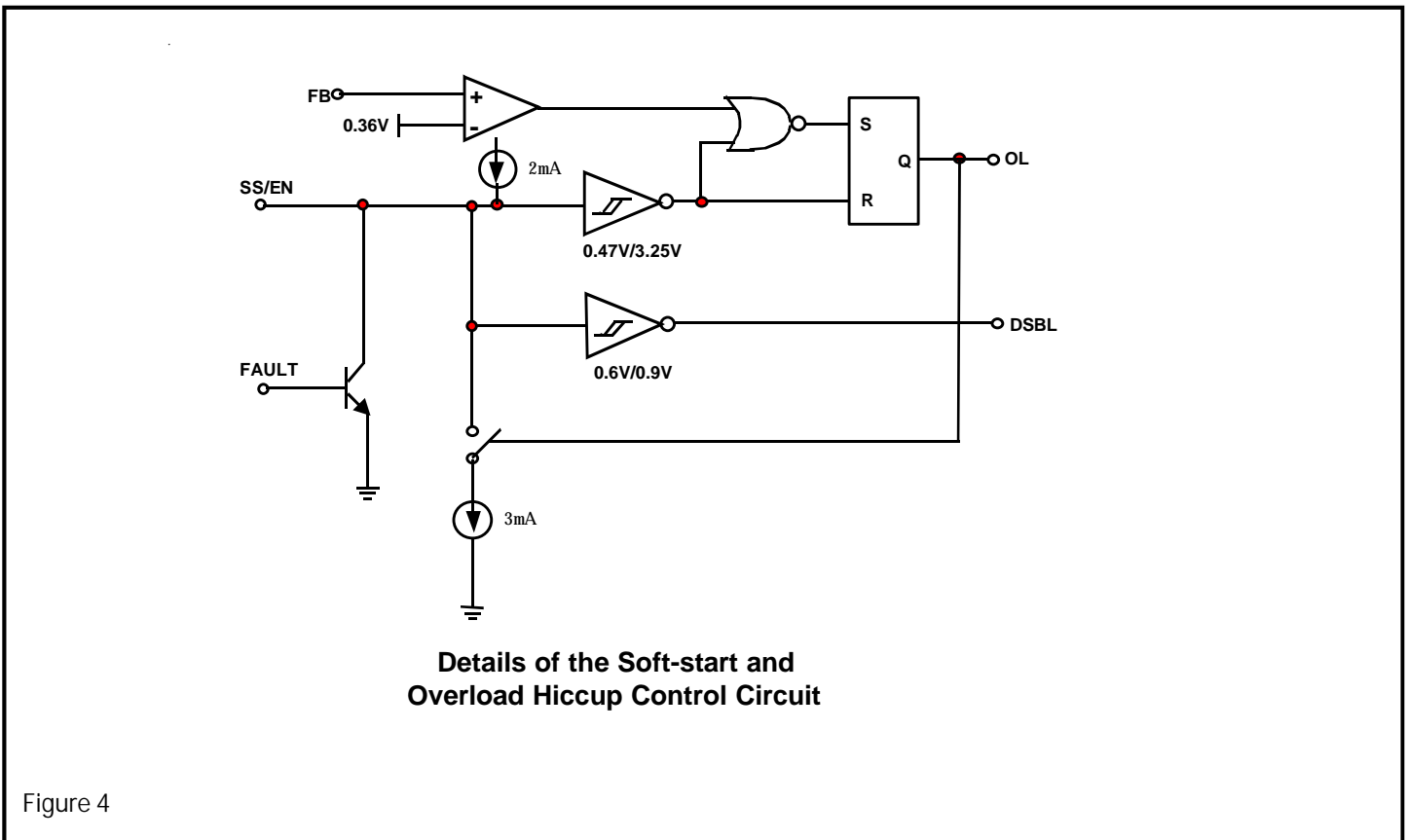
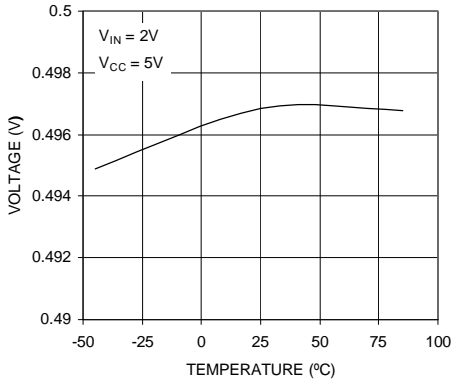


Figure 4

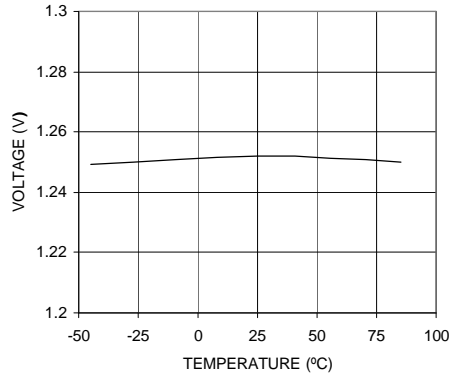
POWER MANAGEMENT

Typical Performance Characteristics

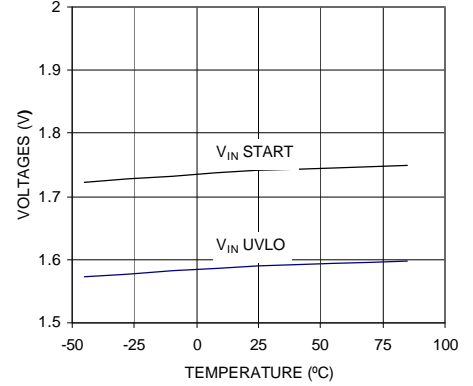
FB1 AND FB2 VOLTAGES vs TEMPERATURE



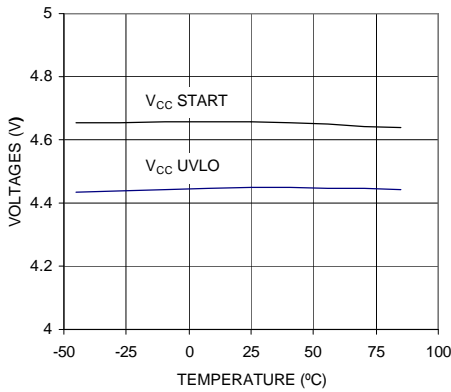
FB3 VOLTAGE vs TEMPERATURE



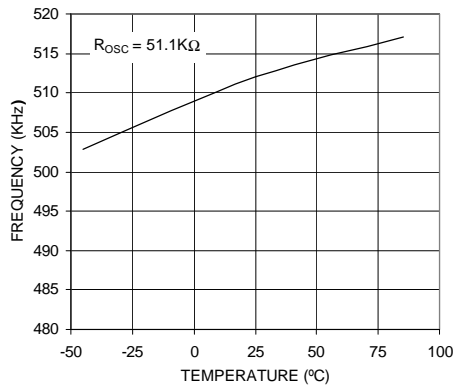
VIN START AND UVLO THRESHOLD VOLTAGES vs TEMPERATURE



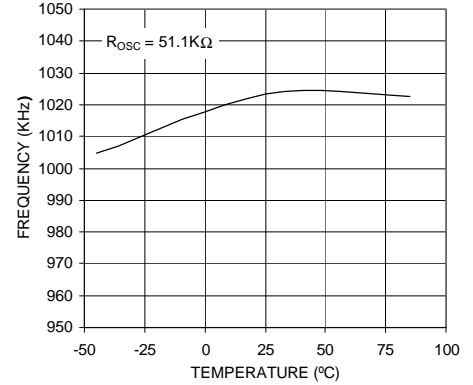
VCC START AND UVLO THRESHOLD VOLTAGES vs TEMPERATURE



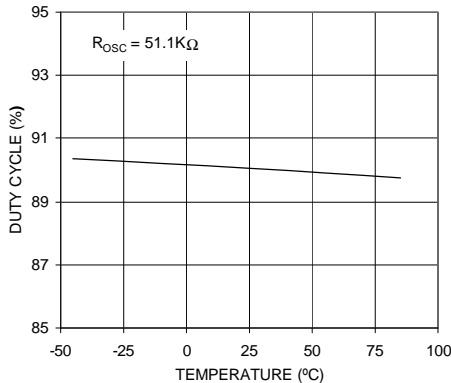
STEP-DOWN CHANNEL SWITCHING FREQUENCY vs TEMPERATURE



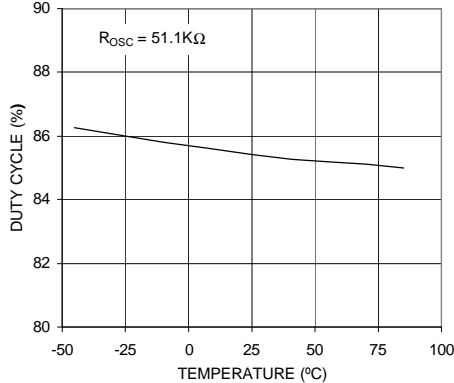
STEP-UP CONVERTER SWITCHING FREQUENCY vs TEMPERATURE



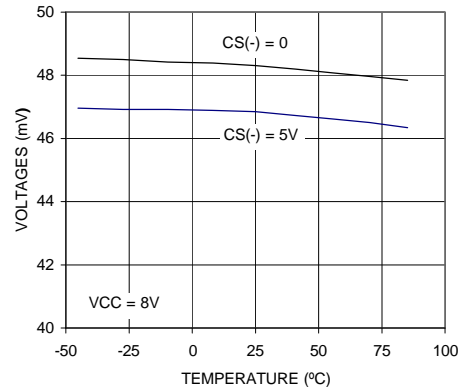
MAXIMUM DUTY-CYCLE OF STEP-DOWN CHANNEL vs TEMPERATURE



STEP-UP SWITCH MAXIMUM DUTY-CYCLE vs TEMPERATURE



STEP-DOWN CONTROLLER CURRENT-LIMIT THRESHOLD vs TEMPERATURE



## POWER MANAGEMENT

## Operation

## Overview

The SC2441 is a constant frequency triple-output switching regulator especially designed for operating from input voltages as low as 1.8V. It consists of two current-mode step-down switch-mode PWM controllers driving all N-channel MOSFET's and a 1.7A step-up current-mode controller with integrated 1.7A power switch. A low voltage input (3.3V, 2.5V or 1.8V) can be stepped up to 5V-10V locally using the boost regulator to provide sufficient gate drives for the step-down converters. The boost converter can also be used to generate a third output.

The two step-down channels of the SC2441 operate at 180 degrees out of phase from each other. Since input currents are interleaved in a two-phase converter, input ripple current is lower and smaller input capacitor can be used for filtering.

The step-down controllers of the SC2441 operate in synchronous continuous-conduction mode. They can be configured either as two independent step-down controllers producing two separate outputs or as a dual-phase single-output controller by tying the FB2 pin to  $V_{CC}$ . In single output operation, the channel-one error amplifier controls both channels and the channel-two error amplifier is disabled. Soft-start and overload hiccup of both channels is also synchronized to channel one.

## Frequency Setting and Synchronization

The step-up regulator in the SC2441 runs at twice the frequency of step-down controllers. Each step-down controller runs at one-half of the oscillator frequency and is 180 degrees out of phase from the other step-down controller. The switching frequency of the step-up regulator is the oscillator frequency and can be set with an external resistor from the  $R_{OSC}$  pin to the ground. The boost regulator and the step-down controllers are capable of operating up to 2 MHz and 1 MHz respectively. It is necessary to consider the operating duty-ratio range before deciding the switching frequency. See Applications Information section for more details.

When synchronized externally, the applied clock frequency (hence switching frequency of the step-up converter) should be twice the individual phase frequency of the step-down controllers. The synchronizing clock frequency

should also be between 1-1.33 times the set free-running frequency.

If not synchronized, the SYNC/SHDN pin should be tied to the input. Pulling the SYNC/SHDN pin below 0.5V shuts off the SC2441 after 85 $\mu$ s time delay.

## Control Loop

The step-down controllers and the boost regulator in the SC2441 use peak current-mode control for fast transient response, ease of compensation and current sharing in single output operation. The low-side MOSFET of each step-down channel is turned off at the falling-edge of the phase clock. After a brief non-overlapping conduction interval of 74ns, the high-side MOSFET is turned on. The phase inductor current ramps up. When the sensed inductor current reaches the threshold determined by the error amplifier output and ramp compensation, the high-side MOSFET is turned off. After a non-overlapping delay of 62ns, the low-side MOSFET is turned on.

The supply voltages for the high-side gate drivers are obtained from two diode-capacitor bootstrap circuits. If the bootstrap capacitor is charged from  $V_{CC}$ , then the high-side gate drive voltage will swing from approximately  $2V_{CC}$  to the ground. The outputs of the low-side gate drivers swing from  $V_{CC}$  to the ground.

All three converters in the SC2441 have internal ramp-compensation to prevent sub-harmonic oscillation when operating above 50% duty cycle. The internal compensating ramp is designed for an inductor ripple-current of between  $\frac{1}{4}$  to  $\frac{1}{3}$  of the maximum inductor current and the peak-to-peak current-sense voltage (CSP-CSN of the step-down controllers) of between  $\frac{1}{4}$  to  $\frac{1}{3}$  of the current-limit threshold (50mV). The current-limits of all three converters are unaffected by the compensation ramps.

## Current-Sensing

Since the inductor current ramp is used as the modulating ramp in current-mode control, the inductor current needs to be sensed. There are two current sensing methods for the step-down controllers. Since the maximum current-sense voltage (CSP-CSN) is only 50mV, a precision sense resistor in series with the inductor can be used at the output without resulting in excessive power dissipation.

## POWER MANAGEMENT

## Operation (Cont.)

Although accurate and far easier to lay out than high-side resistor sensing, a pair of precision sense resistors adds cost to the converter. The SC2441 has provision to reconstruct a differential voltage proportional to the inductor current at the output of the converter. The voltage to current ratio or the equivalent sense resistance  $R_{eq}$  is a combination of high-side and low-side MOSFET  $R_{DS(ON)}$ 's and the inductor series resistance (hence the name "combi-sense"). The SC2441 provides the virtual phase voltages VPN1 and VPN2 (these are unloaded versions of their respective phase voltages) for current sensing. This method does not require precision sense resistor. It is cheaper to implement but is less accurate than resistor current sensing. Since the sensed voltage is developed at the output of the step-down converter, it is less prone to switching transient spikes. This method will be described in more details in the Applications Information section.

Boost switch current is sensed with an integrated sense resistor with a current-limit of 1.7A.

## Error Amplifiers

All error amplifiers in the SC2441 are transconductance amplifiers. Converters are compensated with series RC network from the COMP pins to the ground. An additional small parallel capacitor may be required for stability.

In closed loop operation, the step-down error amplifiers output range from 1.7V to 3.5V. There is no control (high-side) gate drive until the COMP voltage exceeds 1.6V. Both non-inverting inputs of the feedback amplifiers are tied to an internal 0.5V voltage reference.

The error amplifier of the step-up converter has 1.25V as its reference voltage. Its output voltage ranges from 0.8V to 1.35V in closed-loop operation.

## Current-Limit

The maximum current sense voltage of +50mV is the cycle-by-cycle peak current limit when the load is drawing current from the converter.

## Soft-Start and Overload Protection

The undervoltage lockout circuit discharges the SS/EN capacitors. After  $V_{CC}$  rises above 4.65V, the SS/EN capacitors are slowly charged by internal 2.3 $\mu$ A current sources. With internal PNP transistors, the SS/EN voltages clamp the error amplifier outputs. When the error amplifier output rises to 1.7V, the high-side MOSFET starts to switch. As the SS/EN capacitor continues to charge, the COMP voltage follows. The converter gradually delivers increasing power to the output. The inductor current follows the COMP voltage envelope until the output goes into regulation. The SS/EN clamp on COMP is released.

After the SS/EN capacitor is charged above 3.25V (high enough for the error amplifier to provide full load current), the overload detection circuit is activated. If the output voltage falls below 70% of its set value, an overload latch will be set and both the top and the bottom MOSFET's will be turned off. The SS/EN capacitor is slowly discharged with an internal 1.4 $\mu$ A current sink. The overload latch is reset when the SS/EN capacitor is discharged below 0.47V. The SS/EN capacitor is then recharged with the 2.3 $\mu$ A current source and the converter undergoes soft-start. If overload persists, the step-down converters will undergo repetitive shutdown and restart (hiccup). Soft-start process should be slow enough to allow the output to reach 70% of its final value before the SS/EN capacitor is charged above 3.25V (see Figure 4).

If the output is short-circuited, the inductor current will not increase indefinitely between the time the inductor current reaching its current limit and shutdown. This is due to cycle skipping reduces the actual operating frequency.

The SS/EN pin can also be used as the enable input for that channel. Both the high-side and the low-side MOSFET's will be turned off if the SS/EN pin is pulled below 0.5V.

## POWER MANAGEMENT

### Applications Information

The SC2441 consists of two current-mode synchronous buck controllers and an auxiliary boost converter. The SC2441 can be used to generate

- 1) two independent step-down outputs or
- 2) dual phase single output with current sharing and
- 3) a step-up output

The application information using SC2441 for the control of step-down and step-up converters are described below.

#### Step-down Converter

Specifications of a step-down converter are given by the followings

Input voltage range:  $V_{in} \in [V_{in,min}, V_{in,max}]$

Input voltage ripple (peak-to-peak):  $\Delta V_{in}$

Output voltage:  $V_o$

Output voltage accuracy:  $\epsilon$

Output voltage ripple (peak-to-peak):  $\Delta V_o$

Nominal output (load) current:  $I_o$

Maximum output current limit:  $I_{o,max}$

Output (load) current transient slew rate:  $di_o$  (A/s)

Circuit efficiency:  $\eta$ .

Based on these converter specifications, selection criteria and design procedures for the following components are described.

- 1) output inductor ( $L$ ) type and value,
- 2) output capacitor ( $C_o$ ) type and value,
- 3) input capacitor ( $C_{in}$ ) type and value,
- 4) power switch MOSFET's,
- 5) current sensing and limiting circuitry,
- 6) voltage sensing circuitry,
- 7) loop compensation circuitry.

To illustrate the design process, the following example is used:

$V_{in}=3.3V$ ,  $V_o=1.2V$ ,  $I_o=4A$ ,  $f_s=500kHz$ .

#### Operating Frequency ( $f_s$ )

The switching frequency in the SC2441 is user-programmable. The advantages of constant frequency operation are simple passive component selection and fast transient response with simple frequency compensation. Before setting the operating frequency, the following trade-offs should be considered.

- 1) passive component sizes
- 2) converter efficiency
- 3) EMI
- 4) Minimum switch on time and
- 5) Maximum duty ratio

For a given output power, the sizes of the passive components are inversely proportional to the switching frequency, whereas MOSFET's/Diodes switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging and the cost issues are also to be considered. The frequency bands for signal transmission should be avoided because of EM interference.

#### Minimum Switch On Time Limitation

In both step-down controllers, the falling edge of the clock turns on the top MOSFET. The inductor current ramps up so does the sensed voltage. After the sensed voltage crosses a threshold determined by the error amplifier output, the top MOSFET is turned off. The propagation delay time from the turn-on of the controlling FET to its turn-off is the minimum switch on time. The SC2441 has a minimum on time of about 180ns at room temperature. This is the shortest on interval of the controlling FET. The controller either does not turn on the top MOSFET at all or turns it on for at least 180ns.

For a synchronous step-down converter, the operating duty cycle is  $V_o/V_{in}$ . So the required on time for the top MOSFET is  $V_o/(V_{in}f_s)$ . If the frequency is set such that the required pulse width is less than 180ns, then the converter will start skipping cycles. Due to minimum on time limitation, simultaneously operating at very high switching frequency and very short duty cycle is not practical. If the input voltage is 3.3V and the operating frequency is 1MHz, the lowest output voltage will be 0.6V. There will not be enough modulation headroom if the on time is simply made equal to the minimum on time of the SC2441. For ease of control, we recommend the required pulse width to be at least 1.5 times the minimum on time.

#### Maximum Duty-cycle Consideration

When operating at 500KHz, the maximum top MOSFET on duty-cycle is 90%. The top MOSFET therefore turns off for at least 200ns every cycle regardless of the switching frequency. This places an upper bound on the voltage

## POWER MANAGEMENT

## Applications Information (Cont.)

conversion ratio at a given switching frequency. If the desired output voltage requires high operating duty-cycle, then operating frequency will have to be lowered to allow modulating headroom.

## Setting the Step-down Channel Frequency

The switching frequency of both step-down controllers is set with an external resistor from Pin 10 to the ground. The set frequency is inversely proportional to the resistor value (Figure 5).

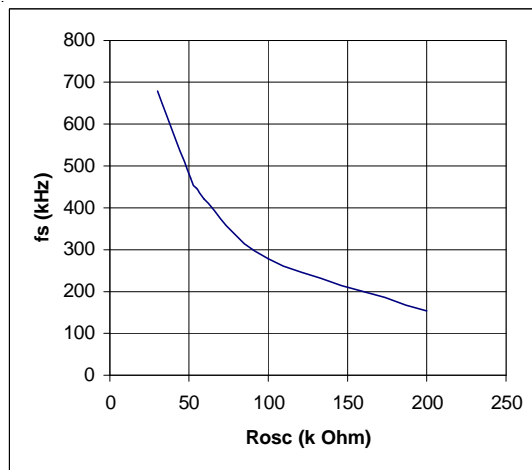


Figure 5. Step-down Channel Free-running frequency vs.  $R_{osc}$ .

## Inductor (L) and Ripple Current

Both step-down controllers in the SC2441 operate in synchronous continuous-conduction mode (CCM) regardless of the output load. The output inductor selection/design is based on the output DC and transient requirements. Both output current and voltage ripples are reduced with larger inductors but it takes longer to change the inductor current during load transients. Conversely smaller inductors results in lower DC copper losses but the AC core losses (flux swing) and the winding AC resistance losses are higher. A compromise is to choose the inductance such that peak-to-peak inductor ripple-current is 20% to 30% of the rated output load current.

Assuming that the inductor current ripple (peak-to-peak) is  $\delta \cdot I_o$ , the inductance will then be

$$L = \frac{V_o(1-D)}{\delta I_o f_s}$$

The peak current in the inductor becomes  $(1+\delta/2) \cdot I_o$  and the RMS current is

$$I_{L,rms} = I_o \sqrt{1 + \frac{\delta^2}{12}}$$

The followings are to be considered when choosing inductors.

- Inductor core material: For high efficiency applications above 350KHz, ferrite, Kool-Mu and polypermalloy materials should be used. Low-cost powdered iron cores can be used for cost sensitive-applications below 350KHz but with attendant higher core losses.
- Select inductance value: Sometimes the calculated inductance value is not available off-the-shelf. The designer can choose the adjacent (larger) standard inductance value. The inductance varies with temperature and DC current. It is a good engineering practice to re-evaluate the resultant current ripple at the rated DC output current.
- Current rating: The saturation current of the inductor should be at least 1.5 times of the peak inductor current under all conditions.

 Output Capacitor ( $C_o$ ) and  $V_{out}$  Ripple

The output capacitor provides output current filtering in steady state and serves as a reservoir during load transient. The output capacitor can be modeled as an ideal capacitor in series with its parasitic ESR ( $R_{esr}$ ) and ESL ( $L_{esl}$ ) (Figure 6).



Figure 6.  $C_o$  equivalent circuit

If the current through the branch is  $i_b(t)$ , the voltage across the terminals will then be

## POWER MANAGEMENT

## Applications Information (Cont.)

$$v_o(t) = V_o + \frac{1}{C_o} \int_0^t i_b(t) dt + L_{\text{esl}} \frac{di_b(t)}{dt} + R_{\text{esr}} i_b(t).$$

This basic equation illustrates the effects of ESR, ESL and  $C_o$  on the output voltage.

The first term is the DC voltage across  $C_o$  at time  $t=0$ . The second term is the ripple-voltage caused by the inductor ripple-current. The third term is the voltage ripple due to ESL and the fourth term is the voltage ripple due to ESR. The total output voltage ripple is then a *vector* sum of the last three terms.

Since the inductor current is a triangular waveform with peak-to-peak value  $\delta^* I_o$ , the ripple-voltage caused by inductor current ripples is

$$\Delta v_C \approx \frac{\delta I_o}{8C_o f_s}$$

The ripple-voltage due to ESL is

$$\Delta v_{\text{ESL}} = L_{\text{esl}} f_s \frac{\delta I_o}{D}$$

and the ESR ripple-voltage is

$$\Delta v_{\text{ESR}} = R_{\text{esr}} \delta I_o.$$

Aluminum capacitors (e.g. electrolytic, solid OS-CON, POSCAP, tantalum) have high capacitances and low ESL's. The ESR has the dominant effect on the output ripple voltage. It is therefore very important to minimize the ESR.

When determining the ESR value, both the steady state ripple-voltage and the dynamic load transient need to be considered. To keep the steady state output ripple-voltage  $< \Delta V_o$ , the ESR should satisfy

$$R_{\text{esr1}} < \frac{\Delta V_o}{\delta I_o}.$$

To limit the dynamic output voltage overshoot/undershoot within  $\alpha$  (say 3%) of the steady state output voltage) under 0 to full load current swing, the ESR value should be

$$R_{\text{esr2}} < \frac{\alpha V_o}{I_o}.$$

The required ESR value of the output capacitors should be

$$R_{\text{esr}} = \min\{R_{\text{esr1}}, R_{\text{esr2}}\}.$$

In the aluminum capacitor selection, the working voltage rating is normally suggested to be greater than  $1.5V_o$ . The allowable current ripple (RMS) should be greater than

$$\frac{\delta I_o}{2\sqrt{3}}.$$

Usually it is necessary to have several capacitors of the same type in parallel to satisfy the ESR requirement. The voltage ripple cause by the capacitor charge/discharge should be an order of magnitude smaller than the voltage ripple caused by the ESR. To guarantee this, the capacitance should satisfy

$$C_o > \frac{10}{2\pi f_s R_{\text{esr}}}.$$

In many application circuits, several low ESR ceramic capacitors are added in parallel with the aluminum capacitors to further reduce ESR and improve high frequency decoupling. Since the capacitances and the ESR's of ceramic and aluminum capacitors are different, the following remarks are made to clarify some practical issues.

**Remark 1:** High frequency ceramic capacitors may not carry most of the ripple current. It also depends on the capacitor value. Only when the capacitor value is set properly, the effect of ceramic capacitor low ESR starts to be significant. For example, if a  $10\mu\text{F}$ ,  $4\text{m}\Omega$  ceramic capacitor is connected in parallel with  $2 \times 1500\mu\text{F}$ ,  $90\text{m}\Omega$  electrolytic capacitors, the ripple current in the ceramic capacitor is only about 42% of the current in the electrolytic capacitors at the ripple frequency. If a  $100\mu\text{F}$ ,  $2\text{m}\Omega$  ceramic capacitor is used, the ripple current in the ceramic capacitor will be about 4.2 times of that in the electrolytic capacitors. When two  $100\mu\text{F}$ ,  $2\text{m}\Omega$  ceramic capacitors are used, the current ratio increases to 8.3. In this case most of the ripple current flows in the ceramic decoupling capacitor. The ESR of the ceramic capacitors will then determine the output ripple-voltage.

**Remark 2:** The total equivalent capacitance of the filter bank is not simply the sum of all the paralleled capacitors. The total equivalent ESR is not simply the parallel combination of all the individual ESR's either. Instead they should be calculated using the following formulae.

$$C_{\text{eq}}(\omega) := \frac{(R_{1a} + R_{1b})^2 \omega^2 C_{1a}^2 C_{1b}^2 + (C_{1a} + C_{1b})^2}{(R_{1a}^2 C_{1a} + R_{1b}^2 C_{1b}) \omega^2 C_{1a} C_{1b} + (C_{1a} + C_{1b})}$$

**POWER MANAGEMENT**

**Applications Information (Cont.)**

$$R_{eq}(\omega) := \frac{R_{1a}R_{1b}(R_{1a} + R_{1b})\omega^2C_{1a}^2C_{1b}^2 + (R_{1b}C_{1b}^2 + R_{1a}C_{1a}^2)}{(R_{1a} + R_{1b})^2\omega^2C_{1a}^2C_{1b}^2 + (C_{1a} + C_{1b})^2}$$

where  $R_{1a}$  and  $C_{1a}$  are the ESR and capacitance of electrolytic capacitors, and  $R_{1b}$  and  $C_{1b}$  are the ESR and capacitance of the ceramic capacitors respectively (Figure 7).

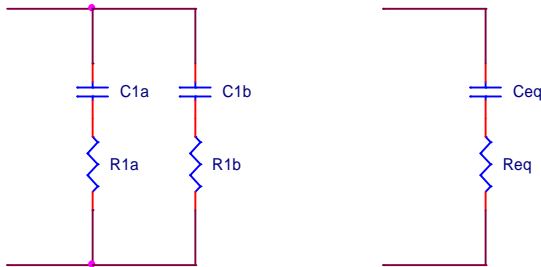


Figure 7. Equivalent RC branch.

$R_{eq}$  and  $C_{eq}$  are both functions of frequency. For rigorous design, the equivalent ESR should be evaluated at the ripple frequency for voltage ripple calculation when both ceramic and electrolytic capacitors are used. If  $R_{1a} = R_{1b} = R_1$  and  $C_{1a} = C_{1b} = C_1$ , then  $R_{eq}$  and  $C_{eq}$  will be frequency-independent and

$$R_{eq} = 1/2 R_1 \text{ and } C_{eq} = 2C_1.$$

**Input Capacitor ( $C_{in}$ )**

The input supply to the converter usually comes from a pre-regulator. Since the input supply is not ideal, input capacitors are needed to filter the current pulses at the switching frequency. A simple buck converter is shown in Figure 8.

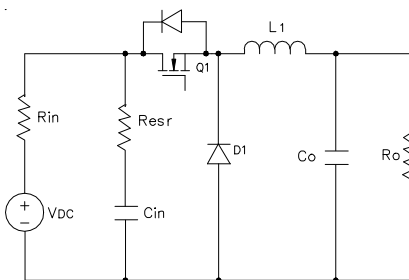


Figure 8. Buck converter input model

In Figure 8 the DC input voltage source has an internal impedance  $R_{in}$  and the input capacitor  $C_{in}$  has an ESR denoted as  $R_{esr}$ . MOSFET and input capacitor current waveforms, ESR voltage ripple and input voltage ripple are shown in Figure 9.

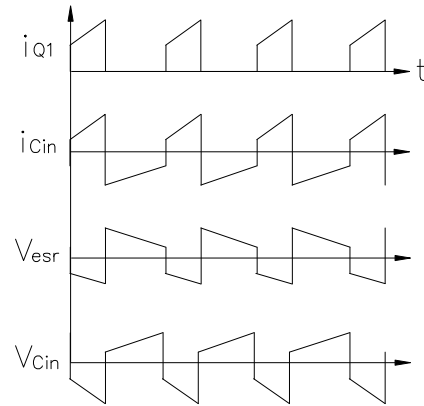


Figure 9. Typical waveforms at the input of a buck converter.

It can be seen that the current in the input capacitor pulses with high di/dt. Capacitors with low ESL should be used. It is also important to place the input capacitor close to the MOSFET's on the PC board to reduce trace inductances around the pulse current loop.

The RMS value of the capacitor current is approximately

$$I_{Cin} = I_o \sqrt{D \left[ \left(1 + \frac{\delta^2}{12}\right) \left(1 - \frac{D}{\eta}\right)^2 + \frac{D}{\eta^2} (1 - D) \right]}$$

The power losses at the input capacitors is then

$$P_{Cin} = I_{Cin}^2 R_{esr}$$

For reliable operation, the maximum power dissipation in the capacitors should not result in more than 10°C of temperature rise. Many manufacturers specify the maximum allowable ripple current (ARMS) rating of the capacitor at a given ripple frequency and ambient temperature. The input capacitance should be high enough to handle the ripple current. For higher power applications, multiple capacitors are placed in parallel to increase the ripple current handling capability.

Sometimes meeting tight input voltage ripple specifications may require the use of larger input capacitance. At full load, the peak-to-peak input voltage ripple due to the ESR is



## POWER MANAGEMENT

## Applications Information (Cont.)

$$\Delta v_{\text{ESR}} = R_{\text{esr}} \left(1 + \frac{\delta}{2}\right) I_o$$

The peak-to-peak input voltage ripple due to the capacitor is

$$\Delta v_c \approx \frac{D I_o}{C_{\text{in}} f_s}$$

From these two expressions,  $C_{\text{IN}}$  can be found to meet the input voltage ripple specification. In a multi-phase converter, channel interleaving can be used to reduce ripple. The two step-down channels of the SC2441 operate at 180 degrees from each other. If both step-down channels in the SC2441 are connected in parallel, both the input and the output RMS currents will be reduced.

Ripple cancellation effect of interleaving allows the use of smaller input capacitors. When converter outputs are connected in parallel and interleaved, smaller inductors and capacitors can be used for each channel. The total output ripple-voltage remains unchanged. Smaller inductors speeds up output load transient.

When two channels with a common input are interleaved, the total DC input current is simply the sum of the individual DC input currents. The combined input current waveform depends on duty ratio and the output current waveform. Assuming that the output current ripple is small, the following formula can be used to estimate the RMS value of the ripple current in the input capacitor.

Let the duty ratios and output currents of Channel 1 and Channel 2 be  $D_1$ ,  $D_2$  and  $I_{o1}$ ,  $I_{o2}$  respectively.

If  $D_1 < 0.5$  and  $D_2 < 0.5$ , then

$$I_{\text{Cin}} \approx \sqrt{D_1 I_{o1}^2 + D_2 I_{o2}^2}$$

If  $D_1 > 0.5$  and  $(D_1 - 0.5) < D_2 < 0.5$ , then

$$I_{\text{Cin}} \approx \sqrt{0.5 I_{o1}^2 + (D_1 - 0.5)(I_{o1} + I_{o2})^2 + (D_2 - D_1 + 0.5) I_{o2}^2}$$

If  $D_1 > 0.5$  and  $D_2 < (D_1 - 0.5) < 0.5$ , then

$$I_{\text{Cin}} \approx \sqrt{0.5 I_{o1}^2 + D_2 (I_{o1} + I_{o2})^2 + (D_1 - D_2 - 0.5) I_{o2}^2}$$

If  $D_1 > 0.5$  and  $D_2 > 0.5$ , then

$$I_{\text{Cin}} \approx \sqrt{(D_1 + D_2 - 1)(I_{o1} + I_{o2})^2 + (1 - D_2) I_{o1}^2 + (1 - D_1) I_{o2}^2}$$

## Power MOSFET Selection and Gate Drive

Main considerations in selecting the MOSFET's are power dissipation, cost and packaging. Switching losses and conduction losses of the MOSFET's are directly related to the total gate charge ( $C_g$ ) and channel on-resistance ( $R_{\text{ds(on)}}$ ). In order to judge the performance of MOSFET's, the product of the total gate charge and on-resistance is used as a figure of merit (FOM). Transistors with the same FOM follow the same curve in Figure 10.

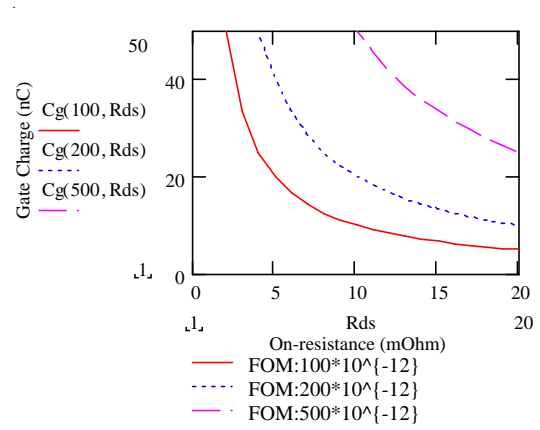


Figure 10. Figure of merit curves.

The closer the curve is to the origin, the lower is the FOM. This means lower switching loss or lower conduction loss or both. It may be difficult to find MOSFET's with both low  $C_g$  and low  $R_{\text{ds(on)}}$ . Usually a trade-off between  $R_{\text{ds(on)}}$  and  $C_g$  has to be made.

MOSFET selection also depends on applications. In many applications, either switching loss or conduction loss dominates for a particular MOSFET. For synchronous buck converters with high input to output voltage ratios, the top MOSFET is hard switched but conducts with very low duty cycle. The bottom switch conducts at high duty cycle but switches at near zero voltage. For such applications, MOSFET's with low  $C_g$  are used for the top switch and MOSFET's with low  $R_{\text{ds(on)}}$  are used for the bottom switch.

## POWER MANAGEMENT

## Applications Information (Cont.)

The losses in power MOSFET's consist of

- conduction loss due to the channel resistance  $R_{ds(on)}$ ,
- switching loss due to the switch rise time  $t_r$  and fall time  $t_f$  and
- the gate loss due to the gate resistance  $R_g$ .

Top Switch:

The *RMS* value of the top switch current is

$$I_{Q1,rms} = I_o \sqrt{D(1 + \frac{\delta^2}{12})}$$

Its conduction loss is then

$$P_{tc} = I_{Q1,rms}^2 R_{ds(on)}$$

$R_{ds(on)}$  varies with temperature and gate-source voltage. Curves showing  $R_{ds(on)}$  variations can be found in manufacturers' data sheet. From the Si7882DP datasheet,  $R_{ds(on)}$  is less than  $4.5m\Omega$  when  $V_{gs}$  is greater than 5V. **However**  $R_{ds(on)}$  increases by nearly 40% as the junction temperature increases from  $25^\circ C$  to  $125^\circ C$ .

The switching losses can be estimated using the simple formula

$$P_{ts} = \frac{1}{2}(t_r + t_f)(1 + \frac{\delta}{2})I_o V_{in} f_s$$

where  $t_r$  is the rise time and  $t_f$  is the fall time of the switching process. Different manufactures have different definitions and test conditions for  $t_r$  and  $t_f$ . To clarify these, we sketch the typical MOSFET switching characteristics under clamped inductive mode in Figure 11.

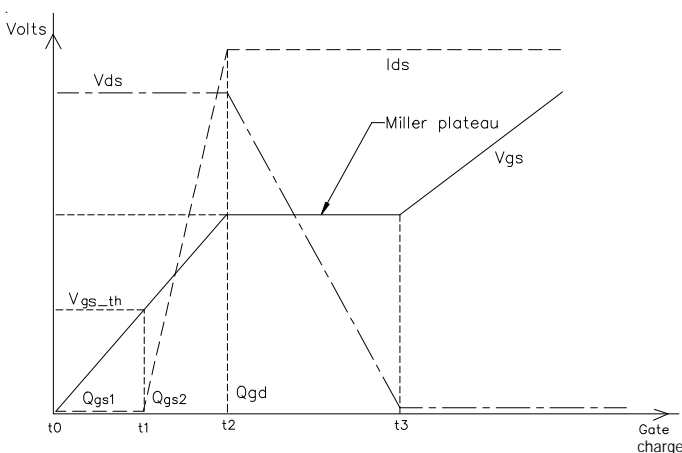


Figure 11. MOSFET switching characteristics

In Figure 11,

$Q_{gs1}$  is the gate charge needed to bring the gate-to-source voltage  $V_{gs}$  to the threshold  $V_{gs-th}$

$Q_{gs2}$  is the additional gate charge required for the switch current to reach its full-scale value  $I_{ds}$  and

$Q_{gd}$  is the charge needed to charge gate-to-drain (Miller) capacitance when  $V_{ds}$  is falling.

Switching losses occur during the time interval  $[t_1, t_3]$ .

Defining  $t_r = t_3 - t_1$ ,  $t_r$  can be approximated as

$$t_r = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{cc} - V_{gsp}}$$

where  $R_{gt}$  is the total resistance from the driver supply rail to the gate of the MOSFET. It includes the gate driver internal impedance  $R_{gd}$ , external resistance  $R_{ge}$  and the gate resistance  $R_g$  within the MOSFET i.e.

$$R_{gt} = R_{gd} + R_{ge} + R_g$$

$V_{gsp}$  is the Miller plateau voltage shown in Figure 11.

Similarly an approximate expression for  $t_f$  is

$$t_f = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{gsp}}$$

Only a portion of the total losses  $P_g = Q_g V_{cc} f_s$  is dissipated in the MOSFET package. Here  $Q_g$  is the total gate charge specified in the datasheet. The power dissipated within the MOSFET package is

$$P_{tg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s$$

The total power loss of the top switch is then

$$P_t = P_{tc} + P_{ts} + P_{tg}$$

If the input supply of the power converter varies over a wide range, then it will be necessary to weigh the relative importance of conduction and switching losses. This is because conduction loss is inversely proportional to the input voltage. Switching loss however increases with the input voltage. The total power loss of MOSFET should be calculated and compared for high-line and low-line cases. The worst case is then used for thermal design.

Bottom Switch:

The *RMS* current in bottom switch can be shown to be

$$I_{Q2,rms} = I_o \sqrt{(1-D)(1 + \frac{\delta^2}{12})}$$

## POWER MANAGEMENT

## Applications Information (Cont.)

The conduction loss is then

$$P_{bc} = I_{O2,rms}^2 R_{ds(on)}$$

where  $R_{ds(on)}$  is the channel resistance of bottom MOSFET. If the input voltage to output voltage ratio is high (e.g.  $V_{in} = 12V$ ,  $V_o = 1.5V$ ), the duty ratio  $D$  will be small. Since the bottom switch conducts with duty ratio  $(1-D)$ , the corresponding conduction losses can be quite high.

Due to non-overlapping conduction between the top and the bottom MOSFET's, the internal body diode or the external Schottky diode across the drain and source terminals always conducts prior to the turn on of the bottom MOSFET. The bottom MOSFET switches on with only a diode voltage between its drain and source terminals. The switching loss

$$P_{bs} = \frac{1}{2}(t_r + t_f)(1 + \frac{r_s}{r_o}) V_o V_d f_s$$

is negligible due to near zero-voltage switching.

The gate loss is estimated as

$$P_{bg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s$$

The total bottom switch loss is then

$$P_b = P_{bc} + P_{bs} + P_{bg}$$

Once the power losses  $P_{loss}$  for the top ( $P_t$ ) and bottom ( $P_b$ ) MOSFET's are known, thermal and package design at component and system level should be done to verify that the maximum die junction temperature ( $T_{j,max}$ , usually  $125^\circ C$ ) is not exceeded under the worst-case conditions. The equivalent thermal impedance from junction to ambient ( $\theta_{ja}$ ) should satisfy

$$\theta_{ja} \leq \frac{T_{j,max} - T_{a,max}}{P_{loss}}$$

$\theta_{ja}$  depends on the die to substrate bonding, packaging material, the thermal contact surface, thermal compound property, the available effective heat sink area and the air flow condition (free or forced convection). Actual temperature measurement of the prototype should be carried out to verify the thermal design.

### Integrated Power MOSFET Drivers

There are four internal MOSFET drivers in step-down section of the SC2441 for driving all the MOSFET's in a dual-channel step-down converter.

Using low gate charge MOSFET's reduces switching loss. It is possible to trade driver IC losses for MOSFET switching losses by adjusting the gate resistance. Lower gate resistance results in higher gate driving current and faster MOSFET switching. However the driver incurs higher losses. Conversely higher gate drive resistance limits the gate drive current, thus lowering the driver dissipation. MOSFET switching loss is higher.

To prevent shoot-through between the top and the bottom MOSFET's during commutation, one MOSFET should be completely turned off before the other is turned on. In the SC2441 the top and the bottom gate drive pulses are made non-overlapping. When not driving any load, the non-overlapping commutation intervals from the top to the bottom and from the bottom to the top gate drives are set at 62ns and 74ns respectively. If MOSFET's are driven from the SC2441, the non-overlapping commutation times will decrease due to finite gate-source voltage rise and fall times. The gate-source voltage waveforms of the MOSFET's should not overlap above their respective thresholds when driven from the SC2441. Use of low gate charge MOSFET's reduces transition times and the tendency of shoot-through. The combined rise and fall times during both commutations should be less than the preset non-overlapping intervals

### Current Sensing (Combi-Sense)

Inductor current sensing is required for the current-mode control. Although the inductor current can be sensed with a precision resistor in series with the inductor, a novel (US patent 6,441,597) lossless combi-sense technique can also be used in the SC2441. This Semtech proprietary technique has the following advantages

- 1) lossless current sensing
- 2) higher signal-to-noise ratio and
- 3) preventing thermal run-away.

The basic arrangement of the combi-sense is shown in Figure 12.

In Figure 12  $R_L$  is the equivalent series resistance of the output inductor.  $R_s$  and  $C_s$  form a RC network for inductor current sensing. This branch is driven from a small totem pole driver (Q3 and Q4) within the SC2441. The base driving signals  $V_{be3}$  and  $V_{be4}$

**POWER MANAGEMENT**

**Applications Information (Cont.)**

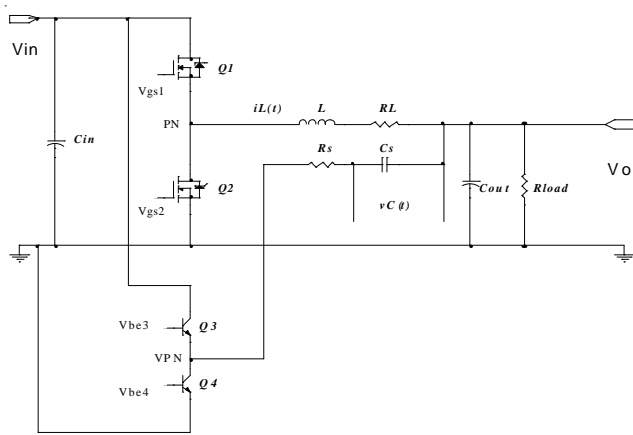


Figure 12. The basic structure of combi-sense.

follow the gate drive signals Vgs1 and Vgs2 respectively with minimal delay. The transition edges at the Virtual Phase Node (VPN) therefore matches closely to those of the Phase Node (PN).

When Q1/Q3 are on and Q2/Q4 are off, the circuit in Figure 12 is reduced to that of Figure 13 a). Here Rds1 is the on-resistance of the top MOSFET. The branches  $\{(R_{ds1}+R_L), L\}$  and  $\{R_s, C_s\}$ , are in parallel. The DC voltage across L and the DC current through  $C_s$  are both zero. There is no DC voltage across  $R_s$  either. Therefore on average, the voltage drop  $(R_{ds1}+R_L)I_o$  equals  $V_{cs}$ . The DC inductor current can be sensed from  $V_{cs}$  if  $(R_{ds1}+R_L)$  is known.

When Q1/Q3 are off and Q2/Q4 are on, the equivalent circuit of Figure 12 reduces to the sub-circuit in Figure 13b). Here Rds2 is the channel resistance of the bottom MOSFET. In this case, the branch  $\{R_s, C_s\}$  is in parallel with  $\{(R_{ds2}+R_L), L\}$  and  $V_{cs}=(R_{ds2}+R_L)I_o$ . Averaging over one switching cycle,

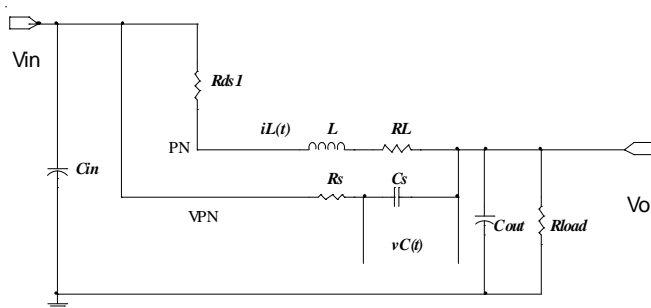


Figure 13. a) Equivalent sub-circuit.

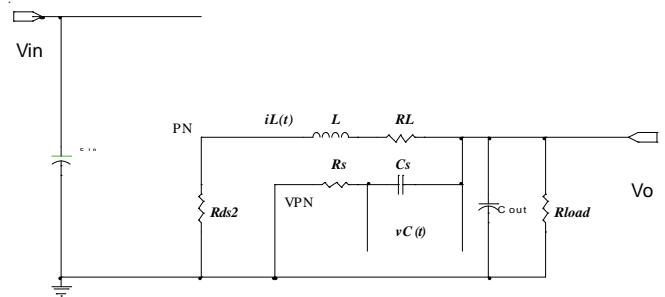


Figure 13. b) Equivalent sub-circuit.

$$V_{cs} = [D(R_{ds1}+R_L) + (1-D)(R_{ds2}+R_L)]I_o$$

or

$$V_{cs} = [D R_{ds1} + (1-D)R_{ds2} + R_L]I_o = R_{eq}I_o$$

The DC voltage across  $V_{cs}$  is independent of L,  $R_s$  and  $C_s$ . If only the average load current is needed (as in average current-mode control), this current sensing method will be sufficient without any additional time-constant matching constraint.

In peak current-mode control, the voltage ripple on  $C_s$  is used as the modulating ramp. The  $V_{cs}$  peak-to-peak amplitude (denoted as  $\Delta V_{cs}$ ) directly affects the signal-to-noise ratio of the PWM operation. Small  $\Delta V_{cs}$  leads to lower signal-to-noise ratio and more jittery operation. Large  $\Delta V_{cs}$  leads to more circuit (power stage) sensitive operation. A good compromise is to make

$$\Delta V_{cs} \sim R_{eq} \delta I_o$$

The above condition holds if the following time-constants are made equal.

$$\frac{L}{R_{eq}} \approx R_s C_s$$

If  $R_{ds1} = R_{ds2}$ , then  $R_{eq} = R_{ds1} + R_L$ . For example, in the application circuit,  $L = 1.3 \mu H$ ,  $R_L = 1.56 m\Omega$  and  $R_{ds1} = R_{ds2} = 8 m\Omega$ , the time constant  $R_s C_s$  should be set as  $136 \mu s$ . If  $C_s = 33 nF$ , then  $R_s = 4.12 k\Omega$ .

## POWER MANAGEMENT

## Applications Information (Cont.)

## Setting the Current Limit

When the voltage difference between CS1+(CS2+) and CS1- (CS2-) exceeds 50 mV, the top MOSFET will be turned OFF and the bottom MOSFET will be turned ON to limit the output inductor current. In the circuit of Figure 12, the converter output current limit is

$$I_{LMcp} = \frac{50mV}{R_{eq}}$$

In the application circuit,  $R_{eq} = 9.56m\Omega$  so  $I_{LM} = 5.23A$ . In other applications, different current limits may be required. The circuit in Figure 14 allows the user to set current-limit different from  $50mV/R_{eq}$ .

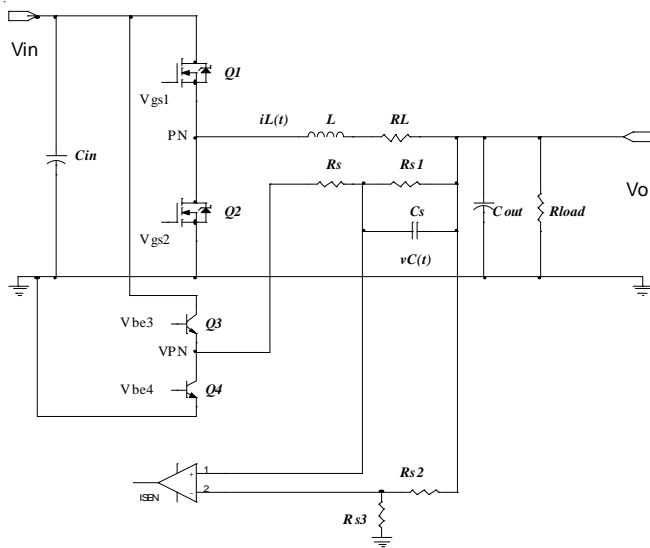


Figure 14. Circuit for setting current-limit different from  $50mV/R_{eq}$

a) The required current limit  $I_{LM}$  is higher than  $I_{LMcp}$ .  $R_{s3}$  is deleted from Figure 14.  $R_{s2}$  is given by

$$R_{s2}C_s = \frac{L}{R_{eq}}$$

$R_s$  is obtained from

$$I_{LM}R_{eq} \frac{R_{s2}}{R_s} = 50mV,$$

$R_{s1}$  is then computed from

$$R_{s1} = \frac{R_{s2}R_s}{R_s - R_{s2}}$$

If the current limit is to be set to  $I_{LM} = 15A$  in the example given in last section with  $C_s = 33nF$ , then  $R_{s2} = 4.12k\Omega$ ,

$R_s = 11.8k\Omega$  and  $R_{s1} = 6.36k\Omega$ .

b) The required current limit  $I_{LM}$  is less than  $I_{LMcp}$ .  $R_{s1}$  is deleted from Figure 14.  $R_s$  is given by

$$R_sC_s = \frac{L}{R_{eq}}$$

$R_{s3}$  is obtained from

$$I_{LM}R_{eq} + \frac{R_s}{R_{s3}}V_o = 50mV,$$

Lastly  $R_{s2}$  is computed from

$$R_{s2} = \frac{R_{s3}R_s}{R_{s3} - R_s}$$

If the current limit is to be set to  $I_{LM} = 2.5A$  with  $V_o = 1.2V$  and  $C_s = 33nF$  in the same example, then  $R_s = 4.12k\Omega$ ,  $R_{s3} = 190k\Omega$  and  $R_{s2} = 4.21k\Omega$ .

**Remark 3:** If the current limit  $I_{LM}$  is lower than  $I_{LMcp}$ , the circuit designer will have the option to use MOSFET's with higher  $R_{ds(ON)}$  to reduce the cost. As a result,  $R_{eq}$  is increased and  $I_{LMcp}$  is reduced. Although the use of low-cost MOSFET's is always preferred, the current-limit setting technique described above allows quick adjustment on a well-tested prototype without the need to replace the power MOSFET's.

## Over Current Protection and Hiccup Mode

During start-up, the capacitor from the SS/EN pin to ground functions as a soft-start capacitor. After the converter starts and enters regulation, the same capacitor operates as overload shutoff timing capacitor. As the load current increases, the cycle-by-cycle current-limit comparator will first limit the inductor current. Further increase in loading will cause the output voltage (hence the feedback voltage) to fall. If the feedback voltage falls to less than 70% of the normal, the controller will shut off both the top and the bottom MOSFET's. Meanwhile an internal current source ( $1.4\mu A$ ) discharges the soft start capacitor  $C_{32}$  ( $C_{33}$ ) connected to the SS/EN pin.

When the capacitor is discharged to 0.47V, a  $2.3\mu A$  current source recharges the SS/EN capacitor and the controller re-initiates soft-start. If the overload persists, the controller will shut down the converter as the soft start capacitor voltage exceeds 3.25V. The converter will repeatedly start and shut off until it is no longer overloaded. This hiccup mode of overload protection is a

## POWER MANAGEMENT

## Applications Information (Cont.)

form of foldback current limiting. The following calculations estimate the average inductor current when the converter output is shorted to the ground.

a) The time taken to discharge the capacitor from 3.25V to 0.47V is

$$t_{\text{ssf}} = C_{32} \frac{(3.25 - 0.47)V}{1.4\mu\text{A}}$$

If  $C_{32} = 0.1\mu\text{F}$ ,  $t_{\text{ssf}}$  will then be 200ms.

b) The soft-start time from 0.47V to 3.25V is

$$t_{\text{ssr}} = C_{32} \frac{(3.25 - 0.47)V}{2.3\mu\text{A}}$$

If  $C_{32} = 0.1\mu\text{F}$ ,  $t_{\text{ssr}}$  will then be 121ms. Note that during soft-start, the converter only starts switching when the voltage at SS/EN exceeds 1.3V.

c) The effective start-up time is

$$t_{\text{ss0}} = C_{32} \frac{(3.25 - 1.3)V}{2.3\mu\text{A}}$$

The average inductor current is then

$$I_{\text{Leff}} = I_{\text{LMcp}} \frac{t_{\text{ss0}}}{t_{\text{ssf}} + t_{\text{ssr}}}$$

$I_{\text{Leff}} = 0.27I_{\text{LMcp}}$  and is independent of the soft start capacitance. The converter will not overheat in hiccup.

## Setting the Output Voltage

The non-inverting inputs of the error amplifiers are internally biased to 0.5V voltage reference. A simple voltage divider ( $R_{01}$  at top and  $R_{02}$  at bottom) sets the converter output voltage.  $R_{02}$  can be expressed as a function of the voltage feedback gain  $h=0.5/V_o$  and  $R_{01}$

$$R_{02} = \frac{h}{1-h} R_{01}$$

Once either  $R_{01}$  or  $R_{02}$  is chosen, the other can be calculated for the desired output voltage  $V_o$ . Since the number of standard resistance values is limited, the calculated

resistance may not be available as a standard value resistor. As a result, there will be a set error in the converter output voltage. This non-random error is caused by the feedback voltage divider ratio. It cannot be corrected by the feedback loop.

The following table lists a few standard resistor combinations for realizing some commonly used output voltages.

$V_o$ (V)	<b>0.6</b>	0.9	<b>1.2</b>	<b>1.5</b>	1.8	2.5	3.3
(1-h)/h	<b>0.2</b>	0.8	<b>1.4</b>	<b>2</b>	2.6	4	5.6
$R_{01}$ (Ohm)	<b>200</b>	806	<b>1.4K</b>	<b>2K</b>	2.61K	4.02K	5.62K
$R_{02}$ (Ohm)	<b>1K</b>	1K	<b>1K</b>	<b>1K</b>	1K	1K	1K

Only the voltages in boldface can be precisely set with standard 1% resistors.

The input bias current of the error amplifier also causes an error in the output voltage. The inverting input bias currents of error amplifiers 1 and 2 are  $-160\text{nA}$  and  $-260\text{nA}$  respectively. Since the non-inverting input is biased to 0.5V, the percentage error in the second output voltage will be  $-100\% \cdot (0.26\mu\text{A}) \cdot R_{01} R_{02} / [0.5 \cdot (R_{01} + R_{02})]$ . To keep this error below 0.2%,  $R_{02} < 4\text{k}\Omega$ .

## Loop Compensation

The SC2441 uses current-mode control for both step-down channels. Current-mode control is a dual-loop control system in which the inductor peak current is loosely controlled by the inner current-loop. The higher gain outer loop regulates the output voltage. Since the current loop makes the inductor appear as a current source, the complex high-Q poles of the output LC networks is split into a dominant pole determined by the output capacitor and the load resistance and a high frequency pole. This pole-splitting property of current-mode control greatly simplifies loop compensation.

The inner current-loop is unstable (sub-harmonic oscillation) unless the inductor current up-slope is steeper than the inductor current down-slope. For stable operation above 50% duty-cycle, a compensation ramp is added to the

## POWER MANAGEMENT

## Applications Information (Cont.)

sensed-current. In the SC2441 the compensation ramp is made duty-ratio dependent. The compensation ramp is approximately

$$I_{\text{ramp}} = D e^{1.1D} * 4.8 \mu\text{A}.$$

The incremental slope of such current ramp is then

$$S_e = (1 + 1.1D) e^{1.1D} f_s * 4.8 \mu\text{A}.$$

Once the inner current loop is stabilized, the output voltage is then regulated with the outer voltage feedback loop. An equivalent circuit of current-mode Buck converter is shown in Figure 15.

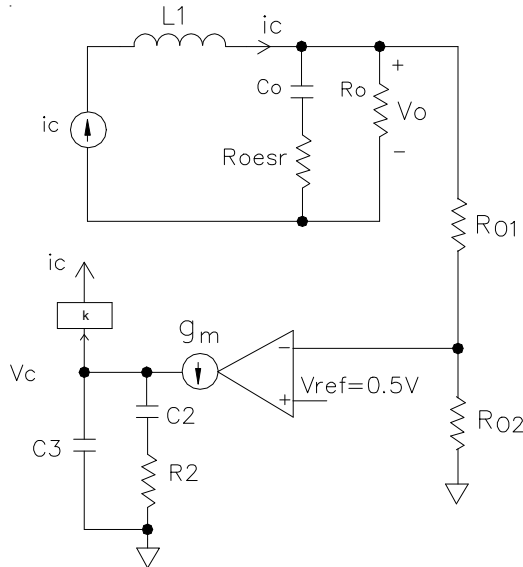


Figure 15. A simple model of current-mode buck converter

The voltage transconductance error amplifier (in the SC2441) has a  $g_m$  of  $400 \mu\text{A}/V$ .  $C_2$ ,  $C_3$  and  $R_2$  of the compensation network are to be determined for stable operation with optimized load transient response.

The feedback gain  $h$  and the resistor values are determined using the equations given in the "Setting the Output Voltage" section with

$$h = \frac{0.5}{V_o}.$$

For the rated output current  $I_o$ , the first-order gain  $k$  is determined as

$$k = \frac{\Delta I_o}{\Delta V_c}.$$

Furthermore the transfer function from the voltage error amplifier output  $v_c$  to the converter output  $v_o$  can be derived from Figure 15.

$$\frac{V_o(s)}{V_c(s)} := G_{vc}(s) = k R_o \frac{1 + \frac{s}{s_{z1}}}{1 + \frac{s}{s_{p1}}},$$

where the single dominant-pole is

$$s_{p1} = \frac{1}{(R_o + R_{oesr}) C_o}$$

and the zero associated with the output capacitor ESR is

$$s_{z1} = \frac{1}{R_{oesr} C_o}.$$

The dominant-pole changes with the converter output load. The controller transfer function (from the converter output  $v_o$  to the voltage error amplifier output  $v_c$ ) is

$$C(s) = \frac{g_m h}{s(C_2 + C_3)} \frac{1 + \frac{s}{s_{z2}}}{1 + \frac{s}{s_{p2}}},$$

where

$$s_{z2} = \frac{1}{R_2 C_2}$$

and

$$s_{p2} = \frac{1}{R_2 \frac{C_2 C_3}{C_2 + C_3}}.$$

The loop transfer function is then

$$T(s) = G_{vc}(s) C(s).$$

## POWER MANAGEMENT

## Applications Information (Cont.)

$P_2$  is a pole for suppressing high-frequency switching noise. So  $P_2 \gg Z_2$ . To simplify design, one usually assumes that  $C_3 \ll C_2$ ,  $R_{oesr} \ll R_o$ ,  $S_{p1} = S_{z2}$  and specifies the loop crossover frequency  $f_c$ . The loop crossover frequency determines the converter dynamic response. With these assumptions, the controller parameters are determined as follows

$$C_2 = \frac{g_m h k R_o}{2\pi f_c}$$

$$R_2 = \frac{R_o C_o}{C_2}$$

and

$$C_3 = \frac{R_{oesr} C_o}{R_2}$$

For example, if  $V_{in} = 3.3V$ ,  $V_o = 1.2V$ ,  $I_o = 4A$ ,  $f_s = 500kHz$ ,  $C_o = 390\mu F$ ,  $R_{oesr} = 16m\Omega$ , one can calculate that

$$R_o = \frac{V_o}{I_o} = 300m\Omega,$$

$$h = \frac{0.5}{V_o} = 0.42$$

and

$$k = \frac{\Delta I_o}{\Delta V_c} = 2.60.$$

If the converter crossover frequency is set around 1/10 of the switching frequency,  $f_c = 50kHz$ , the controller parameters then can be calculated.

$$C_2 = \frac{g_m h k R_o}{2\pi f_c} \approx 0.497nF,$$

use  $C_2 = 0.47nF$ .

$$R_2 = \frac{R_o C_o}{C_2} \approx 150.8k\Omega,$$

use  $R_2 = 150k\Omega$ .

It is further calculated that

$$C_3 = \frac{R_{oesr} C_o}{R_2} \approx 4.97pF,$$

use  $C_3 = 5pF$ . The Bode plots of the loop transfer function (magnitude and phase) are shown in Figure 16.

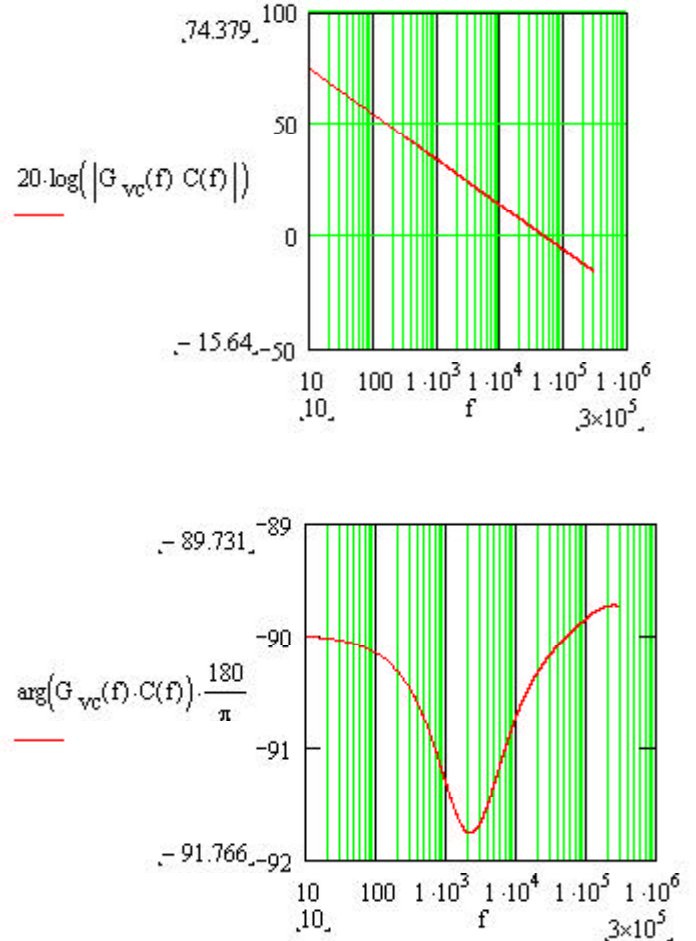


Figure 16. Bode plots of the loop response.

The resulting crossover frequency is about 49.2kHz with **phase margin 90°**.

If the circuit noise makes the converter jitter, a larger  $C_3$  than the calculated value can be used. Effectively the converter bandwidth is reduced to reject high frequency noises. The final circuit should be checked for stability under load transients at different line voltages. The load transient also needs to be measured to ensure that the output voltage is within the specification window.

### Step-up Converter

The step-up regulator in the SC2441 is integrated with a 1.7A power switch. Switch current sensing and ramp compensation are implemented internally. The switching frequency  $f_{s3}$  of the step-up regulator is twice those of the step-down controllers.



## POWER MANAGEMENT

## Applications Information (Cont.)

Given the input voltage  $V_{in}$ , the output voltage  $V_{o3}$  and the load current  $I_{o3}$ , the following circuit parameters are to be determined.

## Inductor Selection

For a specified inductor current ripple (peak-to-peak)  $d_3$ , the inductor value is

$$L_3 = \frac{V_{in}}{f_{s3} \delta_3 I_{o3}} \left(1 - \frac{V_{in}}{V_{o3}}\right) \frac{V_{in}}{V_{o3}}$$

If  $V_{in} = 3.3V$ ,  $V_{o3} = 5V$  and  $I_{o3} = 1A$  with  $d_3 = 0.3$  and  $f_{s3} = 1MHz$ , then,  $L_3 = 2.5\mu H$ .

For operation above 1MHz, Ferrite core material should be used for lower core losses and better circuit efficiency. The peak inductor current is

$$(1 + 0.5 * d_3) I_{o3}$$

The saturation current rating of the selected inductor should be at least 1.2~1.5 times of the calculated peak current value. In the example above, the peak inductor current is 1.74A.

## Capacitor Selection

**Input capacitor:** The input capacitance should be large such that the input transients due to both the step-up and the step-down converters do not trip the UVLO threshold 1.59V. Since the SC2441 controls a 2-phase low input voltage step-down converter, the input capacitance is sized to handle the input ripple current of the buck converter. This is usually sufficient for the auxiliary boost converter because the input current in a boost converter is continuous. A small ( $< 1\mu F$ ) ceramic bypass capacitor can be soldered close to the PVIN pin for high frequency filtering.

**Output capacitor:** Unlike buck converter, pulse current is delivered to the output of a boost converter. To reduce the output ripple voltage, low ESR capacitors should be used. The output capacitor should also be able handle the output ripple current. The SC2441 is designed to use multi-layer ceramic capacitor as the sole output capacitor.

## Maximum Output Current

Figure 4 shows that the boost switch current is sensed with an internal sense resistor  $R_s$ . With a current limit threshold voltage of 14mV, the maximum output current is

$$I_{o3,max} = \frac{(1 - D_3) 14mV}{R_s (1 + \delta_3 / 2)}$$

The boost switch current limit is internally set at 1.7A.

## Voltage Feedback

With the internal reference voltage  $V_{ref3} = 1.25V$ , the voltage feedback gain is

$$h_3 = \frac{V_{ref3}}{V_{o3}} = \frac{1.25}{5} = 0.25$$

The values of the feedback resistors can be determined from the equation in "Setting the Output Voltage" section.

## Loop Compensation

A simple small signal model for current-mode boost converter in continuous-conduction mode is shown in Figure 17.

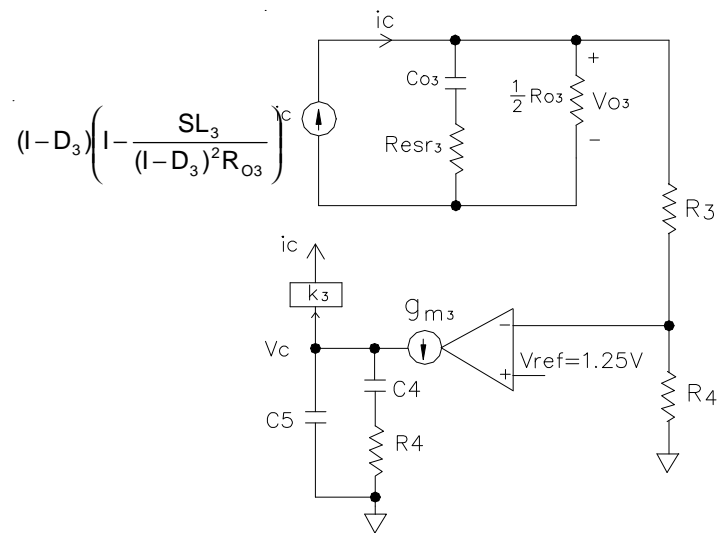


Figure 17. Small signal model of Boost converter.

## POWER MANAGEMENT

## Applications Information (Cont.)

In Figure 17,  $C_{o3}$  and  $R_{esr3}$  are the capacitance and the ESR of the output capacitor,  $g_{m3}$  is the error amplifier transconductance and  $k_3$  is the current loop gain. If one specifies the loop crossover frequency  $f_c$ , the compensation component values are readily calculated as

$$C_4 = h_3 g_{m3} k_3 (1 - D_3) \frac{R_{o3}}{2} \left| 1 - \frac{f_c}{f_{z1}} \right| \frac{1}{2\pi f_c} \frac{R_{esr3}}{R_{esr3} + 0.5R_{o3}},$$

$$R_4 = \frac{1}{C_4} C_{o3} (R_{esr3} + \frac{R_{o3}}{2})$$

and

$$C_5 = C_4 \frac{2R_{esr3}}{R_{o3}}$$

with

$$f_{z1} = \frac{(1 - D_3)^2 R_{o3}}{2\pi L_3}.$$

Bode plots of the loop response are shown in Figure 18.

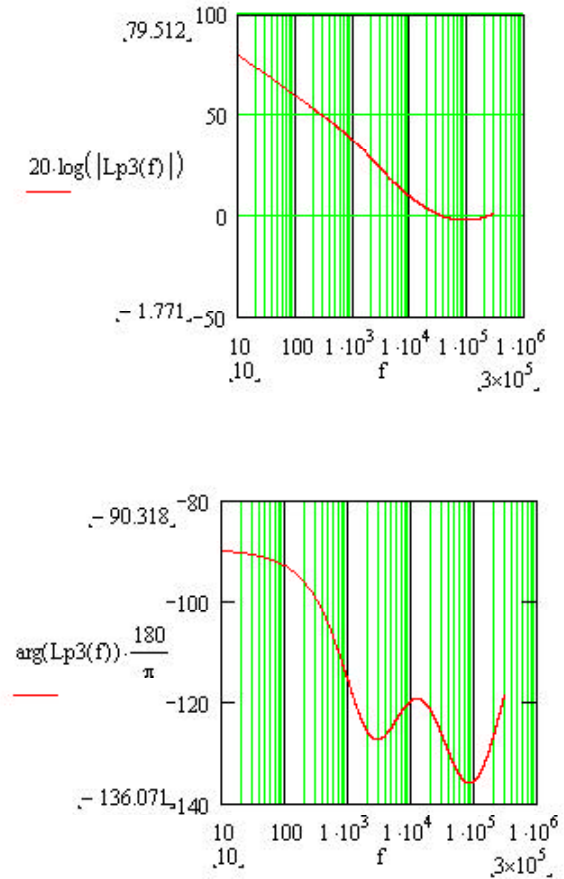


Figure 18. Typical loop transfer function Bode plot of the Boost converter.

## POWER MANAGEMENT

## Applications Information (Cont.)

## PC Board Layout Issues

Circuit board layout is very important for the proper operation of high frequency switching power converters. A power ground plane is required to reduce ground bounces. The followings are suggested for proper layout.

## Power Stage

1) Separate the power ground from the signal ground. In SC2441 the power ground PGND should be tied to the source terminal of lower MOSFETs. The signal ground AGND should be tied to the negative terminal of the output capacitor (output return terminal).

2) Minimize the size of pulse current loop. Place the top MOSFET, the bottom MOSFET and the input capacitors close to each other with short and wide traces. In addition to the aluminum energy storage capacitors, add multi-layer ceramic (MLC) capacitors from the input to the power ground to improve high frequency bypass.

3) Reduce high frequency voltage ringing. Widen and shorten the drain and source traces of the MOSFET's to reduce stray inductances. Add a small RC snubber if necessary to reduce the high frequency ringing at the phase node. Sometimes slowing down the gate drive signal also helps in reducing the high frequency ringing at the phase node.

4) Shorten the gate driver path. Integrity of the gate drive (voltage level, leading and falling edges) is important for circuit operation and efficiency. Short and wide gate drive traces reduce trace inductances. Bond wire inductance is about 2~3nH. If the length of the PCB trace from the gate driver to the MOSFET gate is 1 inch, the trace inductance will be about 25nH. If the gate drive current is 2A with 10ns rise and falling times, the voltage drops across the bond wire and the PCB trace will be 0.6V and 5V respectively. This may slow down the switching transient of the MOSFET's. These inductances may also ring with the gate capacitance.

5) Put the decoupling capacitor for the gate drive power supplies (BST and VCC) close to the IC and power ground.

## Control Section

6) The frequency-setting resistor  $R_{osc}$  should be placed close to Pin 10. Trace length from this resistor to the analog ground should be minimized.

7) Solder the VCC decoupling capacitor next to the VCC and power ground PGND pins.

8) Place the combi-sense components away from the power circuit and close to the corresponding CS+ and CS- pins. Use X7R type ceramic capacitors for combi-sensing due to their thermal stability.

9) Use an isolated local ground plane for the controller and tie it to the negative side of output capacitor bank.

A note for  $V_{in} = 12V$  application

Figure 21 shows an application where the input voltage is 12V. A LDO is used to provide 5V bias for SC2441. The voltages at BST1 (Pin 25) and BST2 (Pin 18) should not exceed their maximum voltage rating (20V).

POWER MANAGEMENT

Application Information

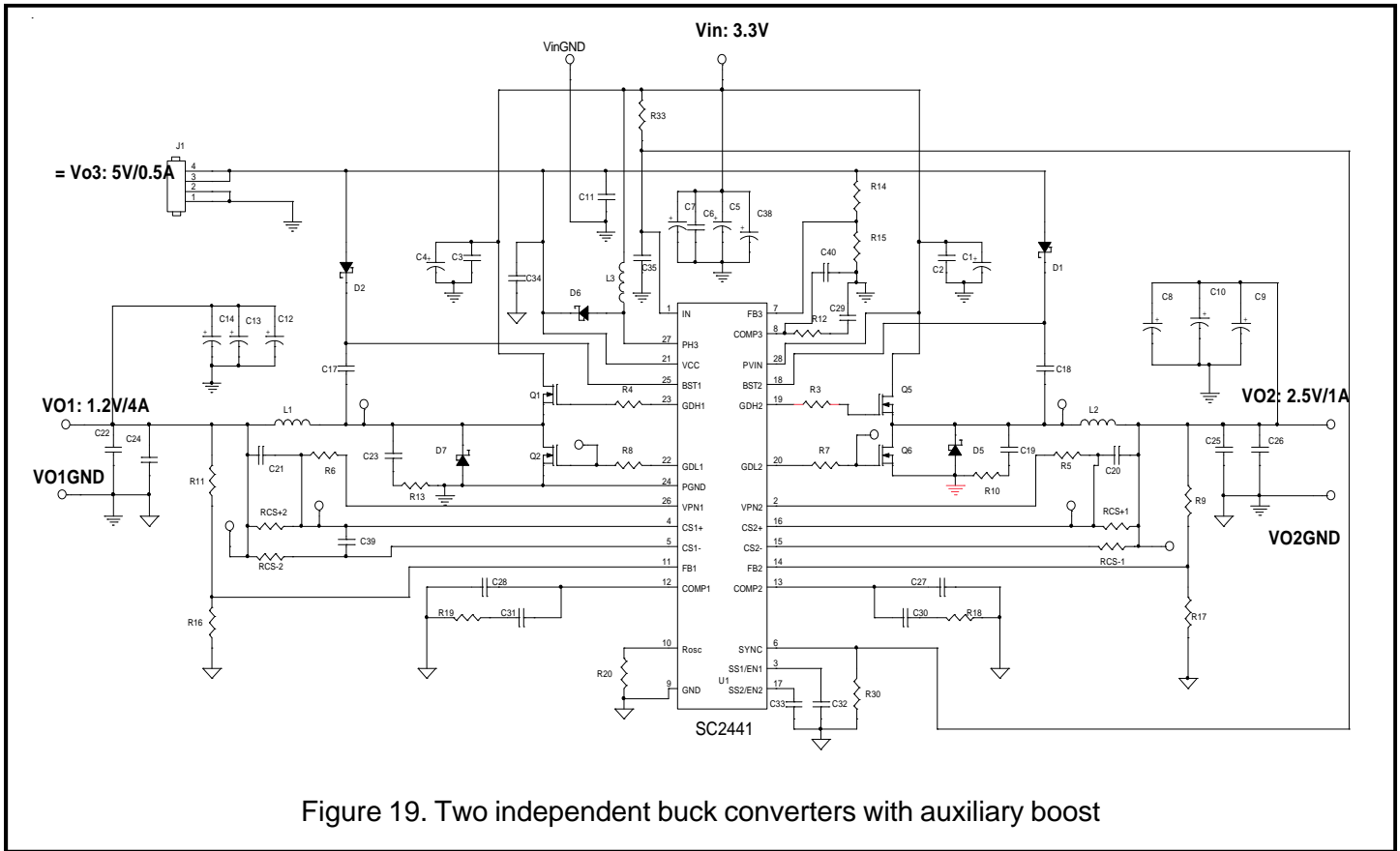


Figure 19. Two independent buck converters with auxiliary boost

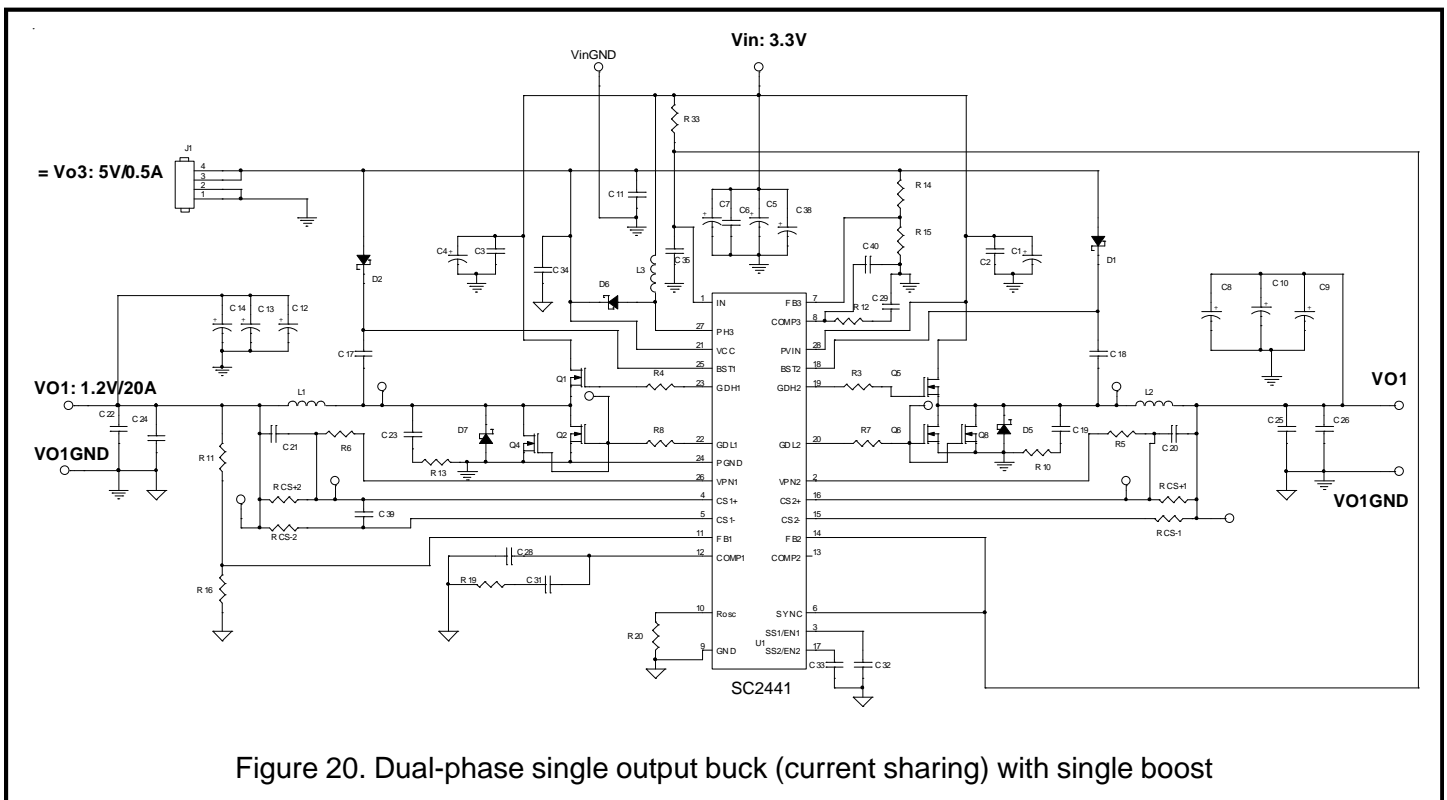


Figure 20. Dual-phase single output buck (current sharing) with single boost

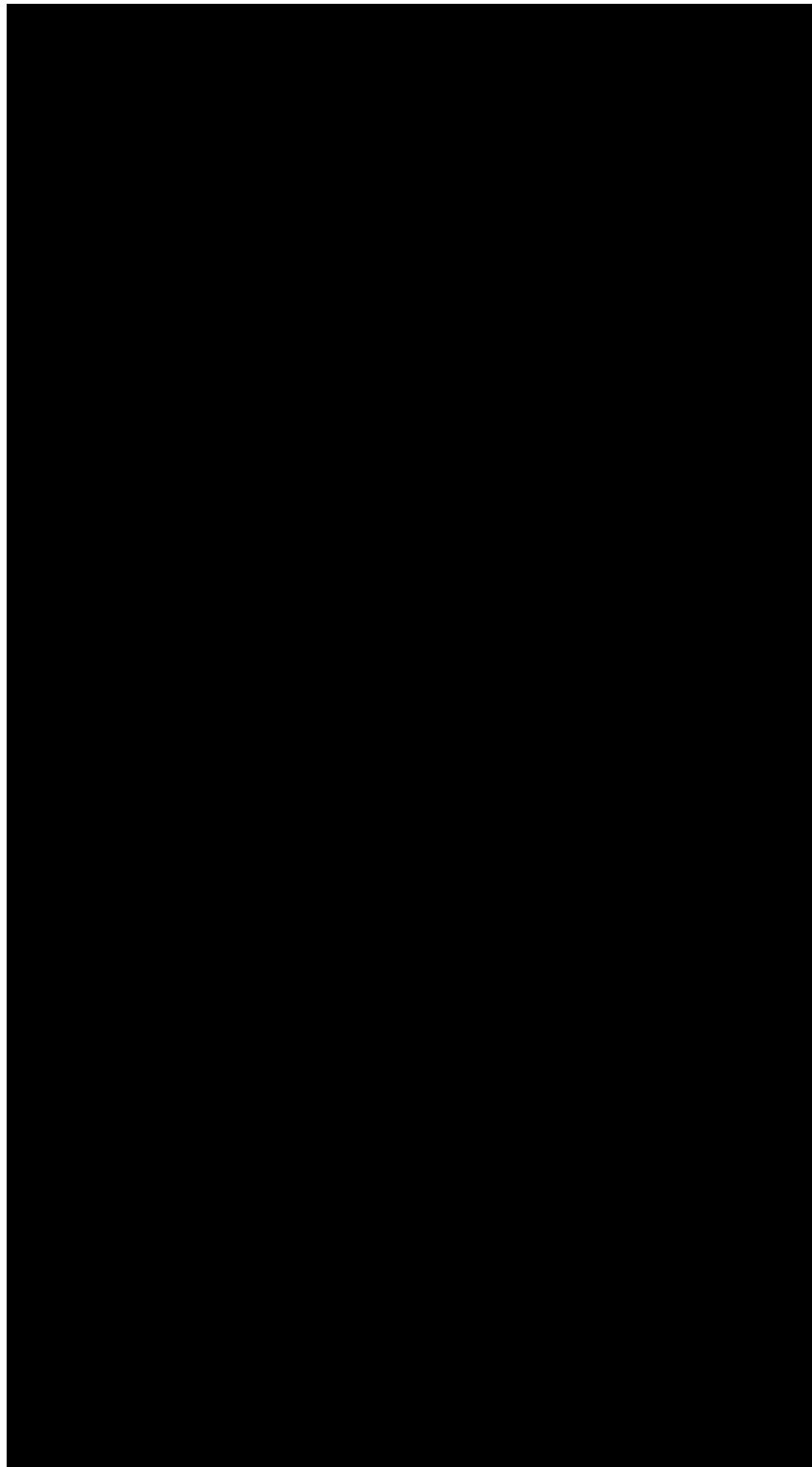


Figure 21. Dual output Buck with 12V input

## POWER MANAGEMENT

## Evaluation Board - Bill of Materials

Ref	Qty	Reference	Part Number/Value	Manufacturer
1	1	C7	150uF, 6.3V, 30mohm, Alum. or OS-CON	Sanyo P/N: 6SP150M
2	3	C2,C3,C6	22uF, 6.3V, X5R, Ceramic 1210	Taiyo Yuden P/N: YMK325BJ226MM
4	1	C11	47uF, 6.3V, X5R, Ceramic	TDK P/N: C3225X5R0J476MJ
5	1	C12	100uF, 6.3V, X5R, Ceramic	TDK P/N: C3225X5R0J107M
6	2	C17,C18	0.33uF, 50V, X5R (or X7R) 1206	Vishay P/N: VJ1206Y334KXAAT
7	2	C19,C23	2.2nF, X5R, Ceramic, 0805	Any
8	1	C20	22nF, X5R, Ceramic, 0805	Any
9	1	C21	10nF, 16V, X5R, Ceramic, 0805	Any
10	2	C22,C25	22uF, 6.3V, X5R, Ceramic, 1210	Taiyo Yuden P/N: YMK325BJ226MM
11	3	C24,C26,C34	10uF, 6.3V, X5R, Ceramic, 1206	TDK P/N: C3216X5R0J106MT
12	1	C27	10pF, X5R, Ceramic, 0805	Any
13	1	C28	10pF, Ceramic, 0805	Any
14	1	C29	1nF, 16V, X5R, Ceramic, 0805	Any
15	1	C30	0.22nF, X5R, Ceramic, 0805	Any
16	1	C31	0.47nF, X5R, Ceramic, 0805	Any
17	2	C32,C33	100nF, X5R, Ceramic, 0805	Any
18	1	C35	1uF, 16V, X5R, Ceramic, 0805	Any
19	1	C40	100pF, 16V, X5R, Ceramic, 0805	Any
20	2	D1,D2	40V, 1A, Schottky	General Semi P/N: 1N5819M, MELF Motorola P/N: MBR5140T3
21	1	D6	40V, 3A, B340A SMA, Shottky, SOD-123	Diode Inc.
22	1	L1	1.8uH, 14A, 3.3mohm	Panasonic P/N: ETQP6F1R8BFA
23	1	L2	6.8uH, 1.5A, 52mohm	Panasonic P/N: ELL6SH6R8M
24	1	L3	9uH, 1.9A, 57mohm	Pulse Eng. P/N: P1167.123T

## POWER MANAGEMENT

## Evaluation Board - Bill of Materials

Ref	Qty	Reference	Part Number/Value	Manufacturer
25	2	(Q1,Q2), (Q5,Q6)	12V, 11.8A, 17mohm, Power pack	Vishay P/N: Si7940DP
26	1	RCS+1	2K, 0805	Any
27	1	RCS+2	5.1K, 0805	Any
28	1	RCS-1	100 Ohm, 0805	Any
29	1	RCS-2	10K, 0805	Any
30	4	R3,R4,R7,R8	1 Ohm 5%, 0805	Any
31	2	R5,R6	15k, 0805	Any
32	1	R9	3.92K, 1%, 0805	Any
33	2	R10,R13	5.1 Ohm, 0805	Any
34	2	R11,R14	4.02K, 1%, 0805	Any
35	1	R12	33.2K, 1%, 0805	Any
36	1	R15	1.43K, 1%. 0805	Any
37	1	R16	3.01K, 1%. 0805	Any
38	1	R17	1.02K, 1%. 0805	Any
39	1	R18	301K, 0805	Any
40	1	R19	150K, 0805	Any
41	1	R20	47.5K, 1%. 0805	Any
42	1	R33	0 Ohm, 0805	Any
43	1	U1	SC2441	Semtech Corp.

\* Dual output Buck with single Boost.

**POWER MANAGEMENT**

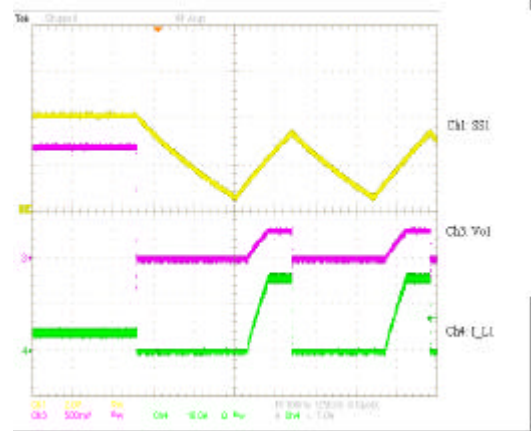
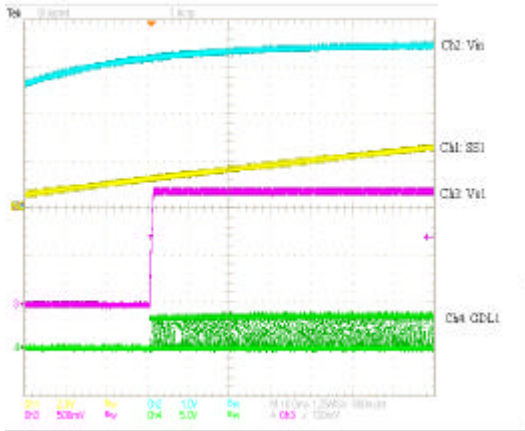
**Typical Characteristics**

Typical waveforms in the evaluation circuit board

Channel 1:  $V_o=1.2V @ 4A$

No load start up

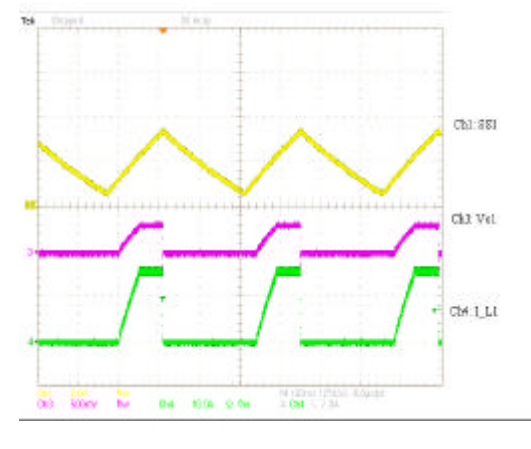
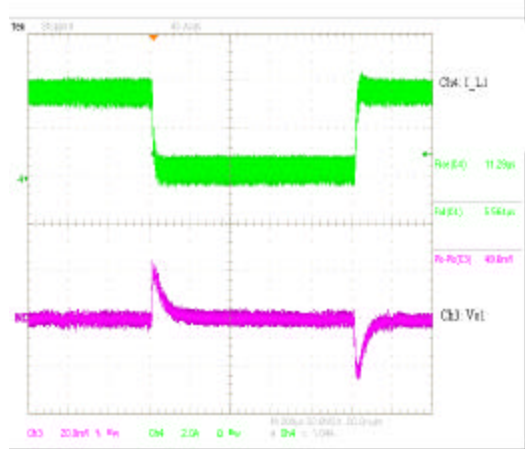
Overload protection  
Output shorted



Load transient response

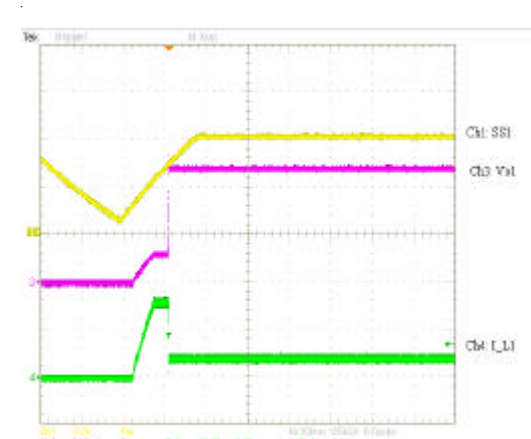
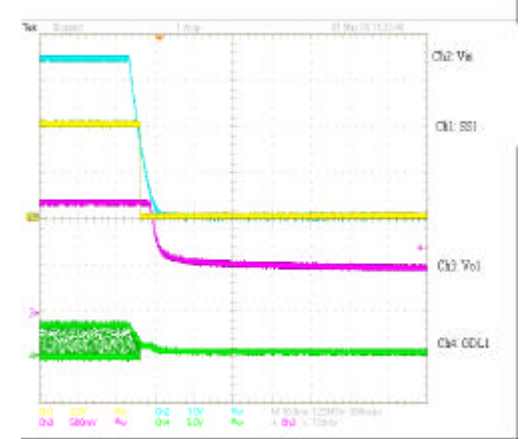
Loading: 0.4A to 3.6A to 0.4A, 2.5A/uS

output short persists



Shut down

Output short removed



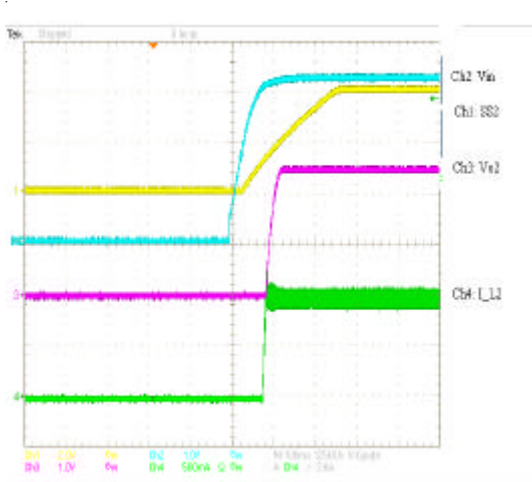


**POWER MANAGEMENT**

**Typical Characteristics (Cont.)**

Typical waveforms in the evaluation circuit board

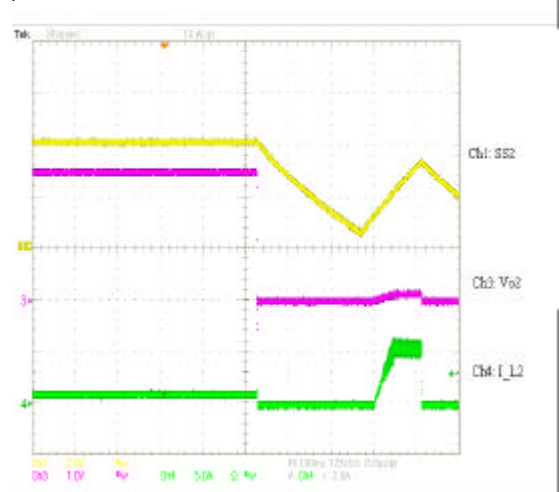
Full load start up



Channel 2:  $V_o=2.5V @ 1A$

Overload protection

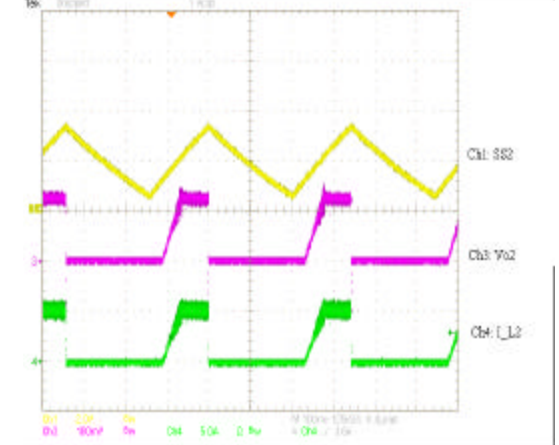
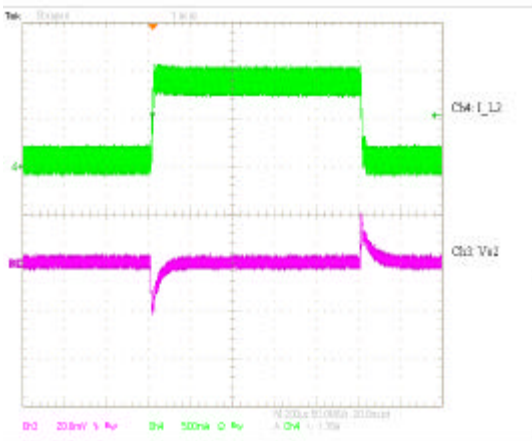
Output shorted



Load transient response

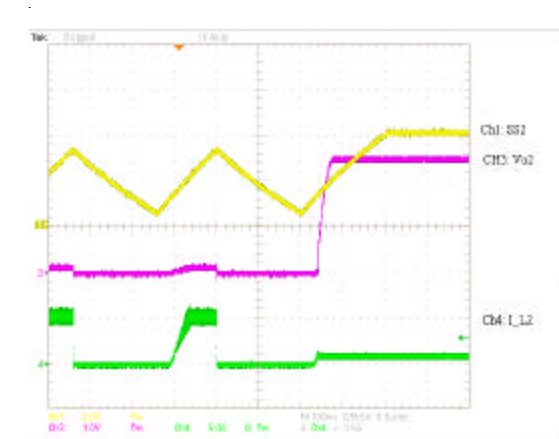
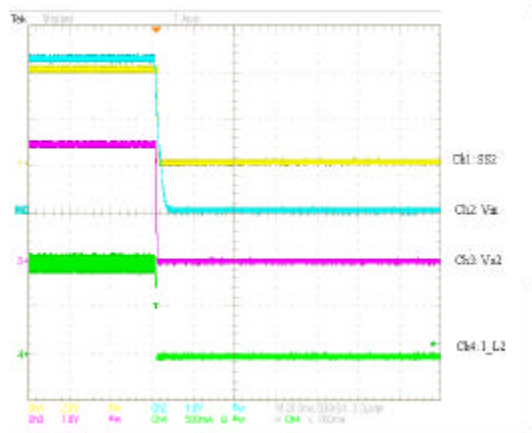
Loading: 0.1A to 0.9A to 0.1A at 2.5A/uS

Output short persists



Shut down

Output short removed



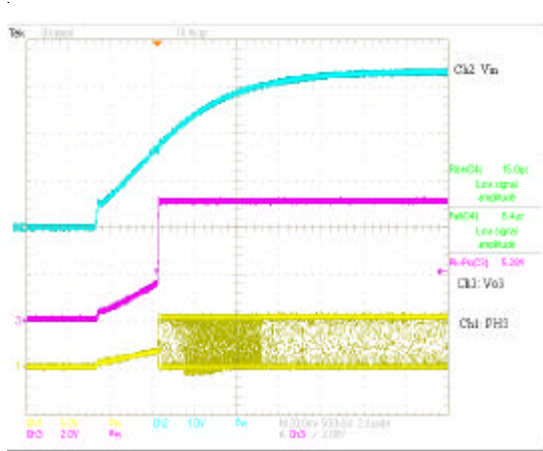
POWER MANAGEMENT

Typical Characteristics (Cont.)

Typical waveforms in the evaluation circuit board

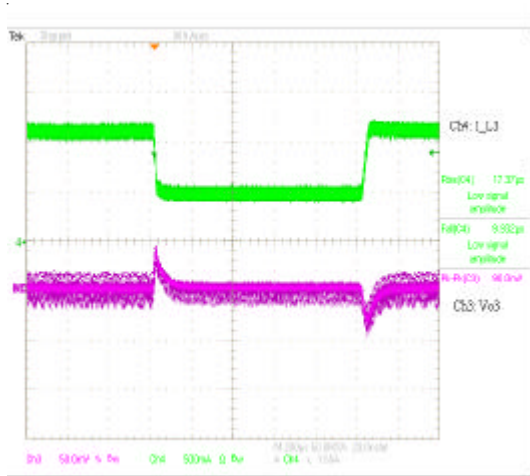
Channel 3:  $V_o=5V @ 0.4A$

Start up



Load transient response

Loading: 0.04A to 0.36A to 0.04A at 2.5A/µs



Shut down

