SC2453
High Performance Quad Output Switching Regulator

Description

The SC2453 is a high performance controller for multi-output converters that can be configured for a wide variety of applications. The SC2453 utilizes PWM synchronous buck topologies where efficiency is most important. It also provides dedicated programmable positive and negative linear regulators using external transistors. Each of the three positive outputs is adjustable down to 0.5V. The two PWM switchers are synchronized 180° out of phase reducing input ripple, allowing for fewer input capacitors. Power up sequencing prevents converter latch-up.

The SC2453 can be synchronized to other converters to prevent beat frequencies. The wide range programmable operating frequency allows users to optimize a converter design. The PWM switchers sense the voltage across the low-side MOSFETs on-resistance to efficiently provide adjustable current-limit, eliminating costly current-sense resistors. A POK signal is issued when soft-start is complete on both PWM switchers and their outputs are within 10% of the set point.

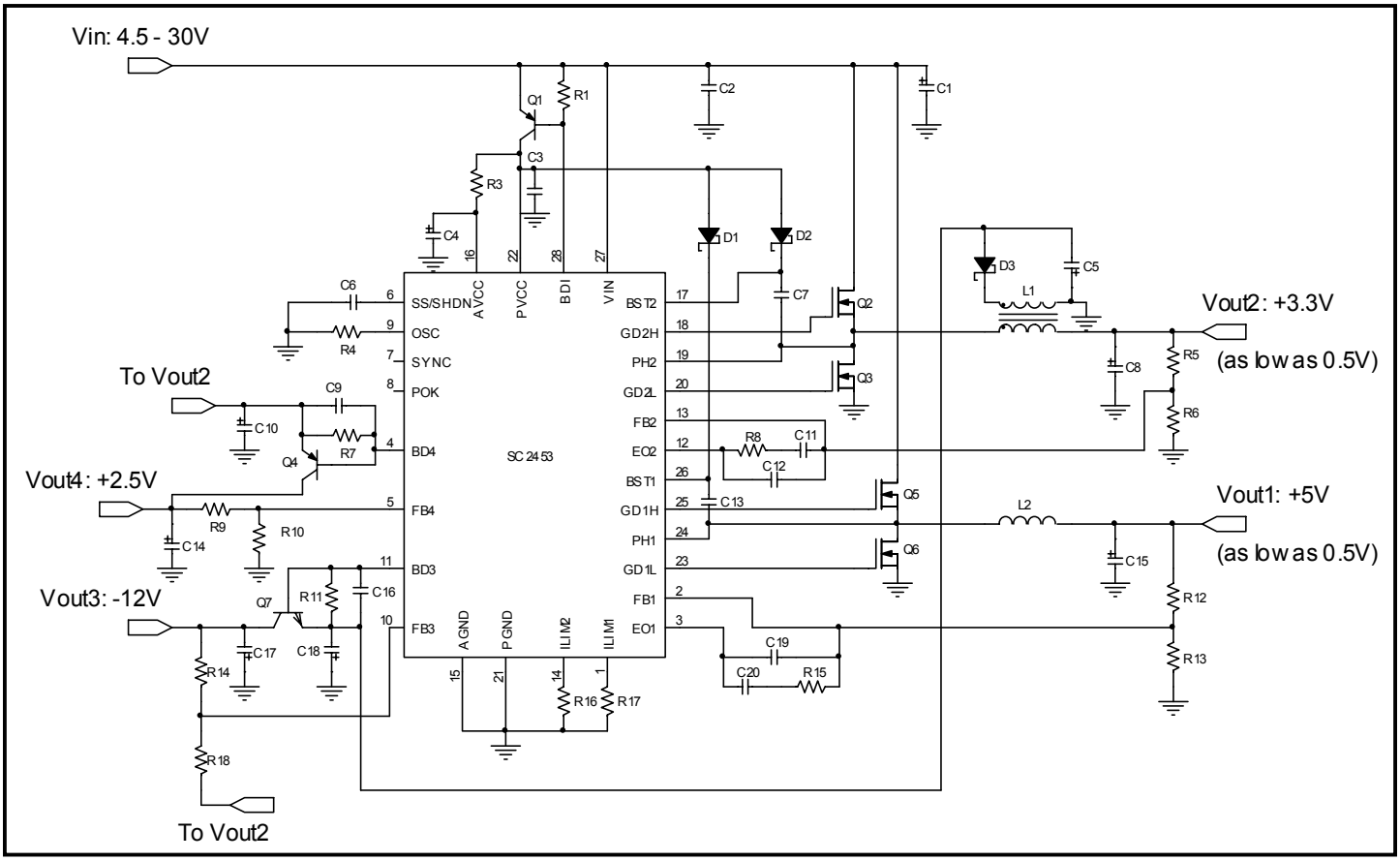
Features

- Two synchronized converters for low noise
- Power up sequencing to prevent latch-up
- Out of phase operation for low input ripple
- Over current protection
- Wide input range, 4.5 to 30V
- Programmable frequency up to 700KHz
- Two synchronous bucks for high efficiency at high current
- One dedicated programmable positive linear regulator and one dedicated programmable negative linear regulator
- Output voltage as low as 0.5V
- Small package TSSOP-28. Also offered in lead free, WEEE and RoHS compliant package

Applications

- DSL applications with multiple input voltage requirements
- Mixed-Signal applications requiring positive and negative voltages
- Cable modem power management
- Base station power management

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Maximum	Units
BST1, BST2 to PGND	35	V
VIN, BDI to AGND	30	V
PVCC, AVCC to PGND	7	V
PGND to AGND	±0.3	V
PH1 to BST1, PH2 to BST2	-6 to 0.3	V
GD1H to PH1, GD2H to PH2	7	V
GD1L, GD2L to PGND	7	V
ILIM1, ILIM2 to AGND	7	V
OSC, SYNC, POK, SS to AGND	7	V
BD3 to AVCC	-25 to 0.3	V
BD4 to AGND	7	V
FB1, FB2, FB3, FB4, EO1, EO2 to AGND	-0.3 to 7	V
GD1H, GD1L, GD2H, DG2L Source or Sink Current	1	A
Storage Temperature Range	-60 to +150	°C
Junction Temperature	-40 to +150	°C
Lead Temperature (Soldering) 10 Sec.	300	°C

Electrical Characteristics

Unless specified: V_{CC} = 5V, fs = 600KHz, SS/SHDN = 5V, SYNC = 0V, $T_A = T_J$ = -35°C to 105°C

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply					
Quiescent Current	SS/SHDN = 0V		3.8	4.5	mA
Operating Current	No load		9	12	mA
AVCC	VIN > 5.5V	4.5	5	5.5	V
PVCC	VIN > 5.5V	4.5	5	5.5	V
Undervoltage Lockout					
Start Threshold		4.05	4.23	4.50	V
UVLO Hysteresis			200		mV
PWM Comparator					
Delay to Output			70		nS

Electrical Characteristics (Cont.)

Unless specified: V_{CC} = 5V, fs = 600KHz, SS/SHDN = 5V, SYNC = 0V, $T_A = T_J$ = -35°C to 105°C

Parameter	Test Conditions	Min	Typ	Max	Unit
Positive Linear Regulator					
Feedback Voltage		0.475	0.5	0.525	V
Feedback Input Leakage Current			150		nA
Amplifier Transconductance	V_{FB4} = 0.5V, I_{BD4} = 0.5 to 5mA (sink) @ 1V output		-2	-10	mV
Drive Sink Current			5		mA
Negative Linear Regulator					
Feedback Voltage		-25	0	25	mV
Feedback Input Leakage Current			150		nA
Amplifier Trandconductance	V_{FB3} = 0V, I_{BD3} = 0.5 to 5mA (source) @ -12V output		-5	-10	mV
Driver Source Current			5		mA
PWM Error Amplifier					
Feedback Voltage		0.49	0.5	0.51	V
Input Bias Current				200	nA
Input Offset Voltage			3	6	mV
Open Loop Gain		90			dB
Unity Gain Bandwidth			3		MHz
Output Sink Current			2		mA
Output Source Current			2		mA
Slew Rate			1		V/µS
Oscillator					
Frequency Range		100		700	KHz
Frequency	R_T = 12.5K	540	600	660	KHz
CT Peak Voltage			3.0		V
CT Valley Voltage			0.1		V
SYNC Input High Pulse Width		100			nS
SYNC Rise/Fall Time				50	nS
SYNC Frequency Range		FOSC		FOSC +10%	kHz
SYNC High/Low Threshold			1.5		V

Electrical Characteristics (Cont.)

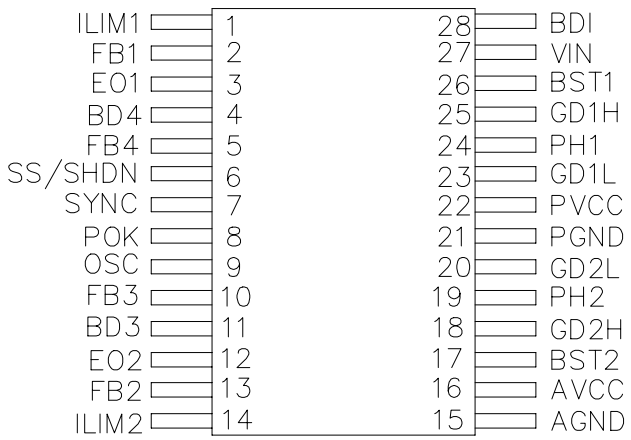
Unless specified: V_{CC} = 5V, fs = 600KHz, SS/SHDN = 5V, SYNC = 0V, $T_A = T_J$ = -35°C to 105°C

Parameter	Test Conditions	Min	Typ	Max	Units
Duty Cycle					
PWM 1 & 2 Maximum Duty Cycle	fs = 100kHz		90		%
PWM 1 & 2 Maximum Duty Cycle	fs = 700kHz		71		%
PWM 1 & 2 Minimum Duty Cycle			2		%
Current Limit					
CH1& 2 ILIM Set Voltage		1.8	2	2.2	V
Soft Start/Shut Down					
Charge Current		5	10	15	µA
Discharge Current			1		mA
Disable Threshold Voltage		0.45	0.5	0.55	V
Disable Low to Shut Down			50		µs
Output					
Gate Drive On-Resistance(H)	I_{SOURCE}=15mA		2	5	Ω
Gate Drive On-Resistance(L)	I_{SINK}=15mA		2	5	Ω
Rise Time(H)	C_{OUT} = 1000pF		15		nS
Fall Time(H)	C_{OUT} = 1000pF		25		nS
Rise Time(L)	C_{OUT} = 1000pF		15		nS
Fall Time(L)	C_{OUT} = 1000pF		15		nS
Power Good					
FB1 & FB2 Trip Level above FB		2	10	20	%
Hysteresis			1		%
FB1 & FB2 Trip Level below FB		-20	-10	-2	%
Hysteresis			1		%
PWR OK Output Low Level	Pullup resistor = 10K		0.4	0.6	V
PWR OK Output High Leakage	Pullup resistor = 10K			30	µA

Note:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Pin Configuration

Top View



(28 Pin TSSOP)

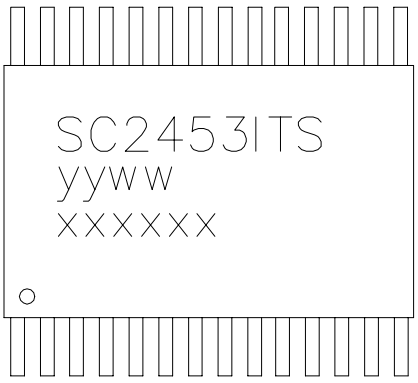
Ordering Information

Part Number	Package[1]	Temp. Range (T_J)
SC2453ITSTR	TSSOP-28	-35°C to +105°C
SC2453ITSTRT[2]		

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Marking Information

TOP



nnnn = Part Number (Example: 1406)
yyww = Date Code (Example: 0012)
xxxxx = Semtech Lot No. (Example: P94A01)

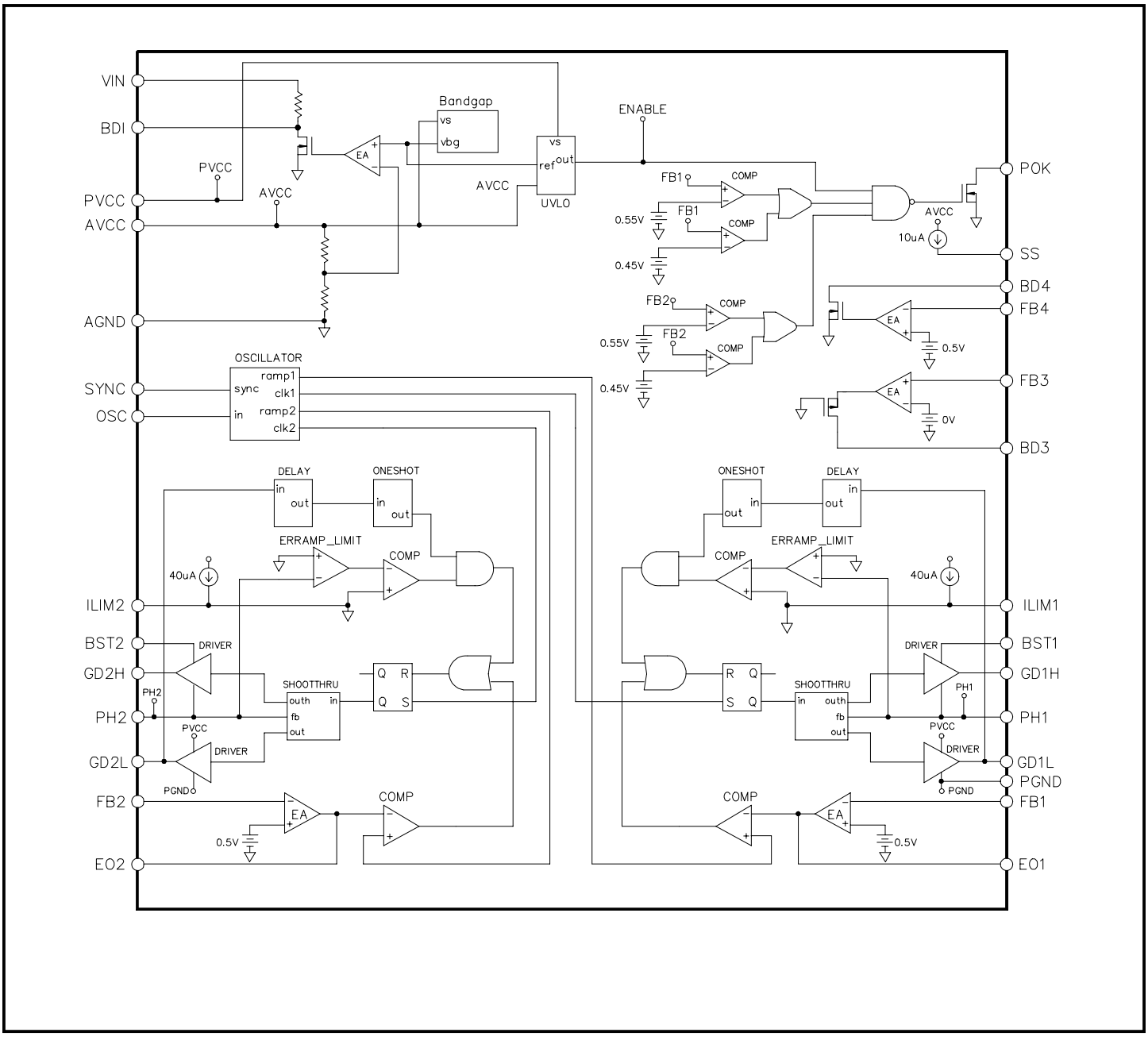
Pin Descriptions

Pin #	Pin Name	Pin Function
1	ILIM1	Adjustable current-limit pin set for the PWM switcher1. Connect a resistor from this pin to AGND.
2	FB1	Voltage mode PWM switcher1 feedback input. Connect to a resistor-divider from output to FB1 to AGND to adjust the output voltage between 0.5V and 0.9 x V_{IN} as maximum duty cycle allowed. The feedback set point is 0.5V.
3	EO1	The PWM switcher1 loop compensation pin. Connect a compensation network to compensate the control loop. Type 3 compensation network is usually used.
4	BD4	Open-drain output PNP transistor driver. Internally connected to the drain of an N-channel MOSFET. This pin connects to the base of an external PNP pass transistor to form a positive linear regulator.
5	FB4	PNP transistor positive linear regulator feedback input. Connect to a resistor-divider between the positive linear regulator and AGND to adjust the output voltage. The feedback set point is 0.5V.
6	SS/SHDN	The pin provides a soft-start function for the PWM switchers and positive linear regulator. When the pin reaches 0.5V, the regulated 10uA pull-up current source charges the capacitor connected from this pin to AGND. The error amplifier reference voltage of switcher1, switcher2 and positive linear regulators ramps from 0.7V to 2V respectively following the sequence. If the pin is pulled down below 0.5V, the SC2453 is disabled.
7	SYNC	The pin can be used to synchronize two or more controllers. This pin requires a 10K resistor to AGND when it is not used.
8	POK	Open-drain power-good output. POK is low when the output voltage is more than 10% below or above the regulation point. POK is high impedance when the output is in regulation. Connect a resistor between the pin and PVCC.
9	OSC	Oscillator frequency adjustable input. Connect a resistor between the pin and AGND to set the PWM frequency.
10	FB3	NPN transistor negative linear regulator feedback input. Connect to a resistor-divider between a positive reference voltage and the negative output to adjust the output voltage. The feedback set point is 0V.
11	BD3	Open-drain output NPN transistor driver. Internally connected to the drain of a P-channel MOSFET. This pin connects to the base of an external NPN pass transistor to form a negative linear regulator.
12	EO2	The PWM switcher2 loop compensation pin. Connect a compensation network to compensate the control loop. Type 3 compensation network is usually used.
13	FB2	Voltage mode PWM switcher2 feedback input. Connect to a resistor-divider from output to FB2 to AGND to adjust the output voltage between 0.5V and 0.9 x V_{IN} as maximum duty cycle allowed. The feedback set point is 0.5V.
14	ILIM2	Adjustable current-limit pin set for the PWM switcher2. Connect a resistor from this pin to AGND.
15	AGND	This is small signal ground and must be routed separately from the high current ground PGND. All voltage levels are measured with respect to this pin. A ceramic capacitor should be connected right to this pin for noise decoupling.

Pin Descriptions (Cont.)

Pin #	Pin Name	Pin Function
16	AVCC	This pin is connected to the output of the external linear regulator to supply the IC. The IC may be powered directly from a single 5V (±10%) supply at this pin. The pin must be always decoupled to PGND with a minimum of 1uF ceramic capacitor, place very close to the pin.
17	BST2	The pin powers the upper MOSFET driver of PWM switcher2. Connect this pin to the junction of the bootstrap capacitor and cathode of the bootstrap diode. The anode of the bootstrap diode is connected to the PVCC.
18	GD2H	Switcher2 upper MOSFET gate driver output. It swings between BST2 and PH2.
19	PH2	The pin is connected to the junction of the upper MOSFET's source, output inductor and lower MOSFET's drain.
20	GD2L	Switcher2 lower MOSFET gate driver output. It swings between PVCC and PGND.
21	PGND	The pin provides the power ground for the lower gate drivers for both PWM switchers. It should be connected to the sources of the lower MOSFETs and the negative terminal of the input capacitors.
22	PVCC	This pin is connected to the output of the external linear regulator to supply the internal lower gate drivers for both PWM switchers. It may be powered directly from a single 5V (±10%) supply at this pin. The pin must be always decoupled to PGND with a minimum of 10uF ceramic capacitor, place very close to the pin.
23	GD1L	Switcher1 lower MOSFET gate driver output. It swings between PVCC and PGND.
24	PH1	The pin is connected to the junction of the upper MOSFETs source, output inductor and lower MOSFETs drain.
25	GD1H	Switcher1 upper MOSFET gate driver output. It swings between BST1 and PH1.
26	BST1	The pin powers the upper MOSFET driver of PWM switcher1. Connect this pin to the junction of the bootstrap capacitor and cathode of the bootstrap diode. The anode of the bootstrap diode is connected to the PVCC.
27	VIN	The pin is internally connected to the pull-up resistor of an N-channel MOSFET to regulate the bias for the IC.
28	BDI	The external bias pass PNP transistor driver. Internally connected to the drain of an N-channel MOSFET.

Block Diagram



Applications Information

The SC2453 is designed to control and drive two N-Channel MOSFET PWM synchronous buck switchers and two positive linear regulators. The two PWM switchers are synchronized 180° out of phase for low input ripple and noise. The switching frequency is programmable to optimize design. The SC2453 PWM switchers feature lossless current sensing and programmable over current limit. The two positive linear regulators output voltages are adjustable.

Power Supplies

Supplies VIN, PVCC and AVCC from the input source are used to power the SC2453. An external PNP transistor linear regulator supplies AVCC and PVCC. The AVCC supply provides the bias for the oscillator, the switchers, the linear regulator controllers and the POK circuitry. PVCC is used to drive the low side MOSFET gate. In low shutdown current mode, the PNP transistor is turned off, disabling AVCC and PVCC.

Soft-start, Sequencing and Disabling

A 10A current source pulls up on the SS/SHDN pin. When the SS/SHDN pin reaches 0.5V, the first switcher is activated and the reference input of the error amplifier is ramped up with the soft-start voltage. When the SS/SHDN pin reaches 2V, the SS/SHDN pin is pulled down to approximately 0.7V and the second switcher begins to soft-start in an identical fashion to the first switcher. When the SS/SHDN pin reaches 2V for the second time, the SS/SHDN pin is pulled down to approximately 0.7V again, and then the positive linear regulators ramp up with the SS/SHDN pin voltage. The SS/SHDN pin is eventually pulled up to the supply AVCC. The soft-start time is controlled by the value of the capacitor connected to the SS/SHDN pin.

If the SS/SHDN pin is pulled down below 0.5V, the SC2453 is disabled. If the SS/SHDN pin is pulled down below 0.34V, the bias PNP transistor for SC2453 is disabled and the supply current is only 100uA.

The power-ok circuitry monitors the FB inputs of the error amplifiers of the switchers. If the voltage on these inputs goes above 0.55V or below 0.45V then the POK pin is pulled low. The POK pin is held low until the end of the start-up sequence.

Frequency Setting and Synchronization

The internal oscillator free-running frequency of the SC2453 is set by an external resistor using the following formula:

$$R_{freq} = \frac{7.9 \times 10^9}{fs - 12 \times 10^3}$$

When it is synchronized externally, the applied clock frequency should be equal or greater than the free-running frequency.

Setting Current Limit

SC2453 monitors the voltage drop in the lower MOSFETs Rdson voltage to sense an over current condition. This method of current sensing minimizes any unnecessary losses due to external sense resistance.

The SC2453 utilizes an internal current source and an external resistor connected from the ILIM pins to the AGND pin to program a current limit level. This limit is programmable by choosing the resistor relative to the level required. The value of the resistor can be selected by the following formula:

$$Rilim = 2000/(Ilim * Rdson)$$

Rilim should be between 10K and 100K.
An internal comparator with a reference from the level set by the external resistor monitors the voltage drop across the lower MOSFET. Once the Vdson of the MOSFET exceeds this level, the low side gate is turned on and the upper MOSFET is turned off in the next switching cycle.

Gate Drives

The low side gate driver is supplied from PVCC and provides a peak source/sink current of 1A. The high side gate drive is also capable of sourcing and sinking peak currents of 1A. The high side MOSFET gate drive can be provided by an external 12V supply that is connected from BST to GND. The actual gate to source voltage of the upper MOSFET will approximately equal 7V (12V-VCC). If the external 12V supply is not available, a classical bootstrap technique can be implemented from the PVCC supply. A bootstrap capacitor is connected from BST to Phase while PVCC is connected through a diode (Schottky or other fast low VF diode) to the BST. This will provide a gate to source voltage approximately equal to the VCC-

Vdiode drop.

Shoot through control circuitry provides a 30ns dead time to ensure both the upper and lower MOSFET will not turn on simultaneously and cause a shoot through condition.

Error Amplifier and PWM Controller

In closed loop operation, the internal oscillator ramp ranges from 0.75V to 3.8V. The error amplifier output ranges determines duty-ratio of a converter. The synchronous continuous-conduction mode of operation allows the SC2453 to regulate the output irrespective of the direction of the load current.

The SC2453 uses voltage-mode control for good noise immunity and ease of compensation. The low-side MOSFET of each channel is turned off at the falling-edge of the phase timing clock. After a brief non-overlapping time interval of 30ns, the high-side MOSFET is turned on. The phase inductor current ramps up. When the internal ramp reaches the threshold determined by the error amplifier output, the high-side MOSFET is turned off. As long as phase voltage collapses below 1.5V, the low-side MOSFET is turned on.

Buck Converter

Buck converter design includes the following specifications:

Input voltage range: $V_{in} \in [V_{in,min}, V_{in,max}]$
Input voltage ripple (peak-to-peak): ΔV_{in}
Output voltage: V_o
Output voltage accuracy: ε
Output voltage ripple (peak-to-peak): ΔV_o
Nominal output (load) current: I_o
Maximum output current limit: $I_{o,max}$
Output (load) current transient slew rate: dI_o (A/s)
Circuit efficiency: η

Selection criteria and design procedures for the following are described.
1) output inductor (L) type and value,
2) output capacitor (C_o) type and value,
3) input capacitor (C_{in}) type and value,
4) power MOSFET's,
5) current sensing and limiting circuit,
6) voltage sensing circuit,
7) loop compensation network.

Operating Frequency (f_s)

The switching frequency in the SC2453 is user-programmable. The advantages of using constant frequency operation are simple passive component selection and ease of feedback compensation. Before setting the operating frequency, the following trade-offs should be considered.

1) Passive component size
2) Circuitry efficiency
3) EMI condition
4) Minimum switch on time and
5) Maximum duty ratio

For a given output power, the sizes of the passive components are inversely proportional to the switching frequency, whereas MOSFET's/Diodes switching losses are proportional to the operating frequency. Other issues such as heat dissipation, packaging and the cost issues are also to be considered. The frequency bands for signal transmission should be avoided because of EM interference.

Minimum Switch On Time Consideration

In the SC2453, the falling edge of the clock turns on the top MOSFET. The inductor current and the sensed voltage ramp up. After the internal ramp voltage crosses a threshold determined by the error amplifier output, the top MOSFET is turned off. The propagation delay time from the turn-on of the controlling FET to its turn-off is the minimum switch on time. The SC2453 has a minimum on time of about 50ns at room temperature. This is the shortest on interval of the controlling FET. The controller either does not turn on the top MOSFET at all or turns it on for at least 50ns.

For a synchronous step-down converter, the operating duty cycle is V_O/V_{IN}. So the required on time for the top MOSFET is $V_O/(V_{IN}fs)$. If the frequency is set such that the required pulse width is less than 50ns, then the converter will start skipping cycles. Due to minimum on time limitation, simultaneously operating at very high switching frequency and very short duty cycle is not practical. If the voltage conversion ratio V_O/V_{IN} and hence the required duty cycle is higher, the switching frequency can be increased to reduce the size of passive components.

Applications Information (Cont.)

There will not be enough modulation headroom if the on time is simply made equal to the minimum on time of the SC2453. For ease of control, we recommend the required pulse width to be at least 1.5 times the minimum on time.

Inductor (L) and Ripple Current

Both step-down controllers in the SC2453 operate in synchronous continuous-conduction mode (CCM) regardless of the output load. The output inductor selection/design is based on the output DC and transient requirements. Both output current and voltage ripples are reduced with larger inductors but it takes longer to change the inductor current during load transients. Conversely smaller inductors results in lower DC copper losses but the AC core losses (flux swing) and the winding AC resistance losses are higher. A compromise is to choose the inductance such that peak-to-peak inductor ripple-current is 20% to 30% of the rated output load current.
Assuming that the inductor current ripple (peak-to-peak) value is $\delta * I_o$, the inductance value will then be:

$$L = \frac{V_o(1-D)}{\delta I_o f_s}$$

The peak current in the inductor becomes (1+δ/2)*Io and the RMS current is:

$$I_{L,rms} = I_o\sqrt{1+\frac{\delta^2}{12}}$$

The followings are to be considered when choosing inductors.

a) Inductor core material: For high efficiency applications above 350KHz, ferrite, Kool-Mu and polypermalloy materials should be used. Low-cost powdered iron cores can be used for cost sensitive-applications below 350KHz but with attendant higher core losses.

b) Select inductance value: Sometimes the calculated inductance value is not available off-the-shelf. The designer can choose the adjacent (larger) standard inductance value. The inductance varies with temperature and DC current. It is a good engineering practice to re-evaluate the resultant current ripple at the rated DC output current.

c) Current rating: The saturation current of the inductor should be at least 1.5 times of the peak inductor current under all conditions.

Output Capacitor (C_o) and V_{out} Ripple

The output capacitor provides output current filtering in steady state and serves as a reservoir during load transient. The output capacitor can be modeled as an ideal capacitor in series with its parasitic ESR (R_{esr}) and ESL (L_{esl}) (Figure 1).

Figure 1. An equivalent circuit of C_o.

If the current through the branch is $i_b(t)$, the voltage across the terminals will then be:

$$v_o(t) = V_o + \frac{1}{C_o}\int_0^t i_b(t)dt + L_{esl}\frac{di_b(t)}{dt} + R_{esr}i_b(t)$$

This basic equation illustrates the effect of ESR, ESL and C_o on the output voltage.

The first term is the DC voltage across C_o at time *t=0*. The second term is the voltage variation caused by the charge balance between the load and the converter output. The third term is voltage ripple due to ESL and the fourth term is the voltage ripple due to ESR. The total output voltage ripple is then a *vector* sum of the last three terms.

Since the inductor current is a triangular waveform with peak-to-peak value $\delta * I_o$, the ripple-voltage caused by inductor current ripples is:

$$\Delta v_C \approx \frac{\delta I_o}{8C_o f_s}$$

the ripple-voltage due to ESL is:

$$\Delta v_{ESL} = L_{esl} f_s \frac{\delta I_o}{D}$$

and the ESR ripple-voltage is:

$$\Delta v_{ESR} = R_{esr}\delta I_o$$

Aluminum capacitors (e.g. electrolytic, solid OS-CON, POSCAP, tantalum) have high capacitances and low ESL's. The ESR has the dominant effect on the output ripple voltage. It is therefore very important to minimize the ESR.

When determining the ESR value, both the steady state ripple-voltage and the dynamic load transient need to be considered. To keep the steady state output ripple-voltage < ΔV_o, the ESR should satisfy:

$$R_{esr1} < \frac{\Delta V_o}{\delta I_o}$$

To limit the dynamic output voltage overshoot/ undershoot within α (say 3%) of the steady state output voltage) from no load to full load, the ESR value should satisfy:

$$R_{esr2} < \frac{\alpha V_o}{I_o}$$

Then, the required ESR value of the output capacitors should be:

$$R_{esr} = \min\{R_{esr1}, R_{esr2}\}$$

The voltage rating of aluminum capacitors should be at least $1.5V_o$. The RMS current ripple rating should also be greater than:

$$\frac{\delta I_o}{2\sqrt{3}}$$

Usually it is necessary to have several capacitors of the same type in parallel to satisfy the ESR requirement. The voltage ripple cause by the capacitor charge/ discharge should be an order of magnitude smaller than the voltage ripple caused by the ESR. To guarantee this, the capacitance should satisfy:

$$C_o > \frac{10}{2\pi f_s R_{esr}}$$

In many applications, several low ESR ceramic capacitors are added in parallel with the aluminum capacitors in order to further reduce ESR and improve high frequency decoupling. Because the values of capacitance and ESR are usually different in ceramic and aluminum capacitors, the following remarks are made to clarify some practical issues.

Remark 1: High frequency ceramic capacitors may not carry most of the ripple current. It also depends on the capacitor value. Only when the capacitor value is set properly, the effect of ceramic capacitor low ESR starts to be significant.

For example, if a 10µF, 4mΩ ceramic capacitor is connected in parallel with 2x1500µF, 90mΩ electrolytic capacitors, the ripple current in the ceramic capacitor is only about 42% of the current in the electrolytic capacitors at the ripple frequency. If a 100µF, 2mΩ ceramic capacitor is used, the ripple current in the ceramic capacitor will be about 4.2 times of that in the electrolytic capacitors. When two 100µF, 2mΩ ceramic capacitors are used, the current ratio increases to 8.3. In this case most of the ripple current flows in the ceramic decoupling capacitor. The ESR of the ceramic capacitors will then determine the output ripple-voltage.

Remark 2: The total equivalent capacitance of the filter bank is not simply the sum of all the paralleled capacitors. The total equivalent ESR is not simply the parallel combination of all the individual ESR's either. Instead they should be calculated using the following formulae.

$$C_{eq}(\omega) := \frac{(R_{1a}+R_{1b})^2\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}{(R_{1a}{}^2 C_{1a}+R_{1b}{}^2 C_{1b})\omega^2 C_{1a}C_{1b}+(C_{1a}+C_{1b})}$$

$$R_{eq}(\omega) := \frac{R_{1a}R_{1b}(R_{1a}+R_{1b})\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (R_{1b}C_{1b}{}^2 + R_{1a}C_{1a}{}^2)}{(R_{1a}+R_{1b})^2\omega^2 C_{1a}{}^2 C_{1b}{}^2 + (C_{1a}+C_{1b})^2}$$

where R_{1a} and C_{1a} are the ESR and capacitance of electrolytic capacitors, and R_{1b} and C_{1b} are the ESR and capacitance of the ceramic capacitors respectively. (Figure 2)

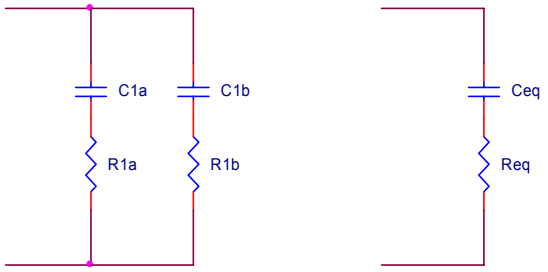


Figure 2. Equivalent RC branch.

Req and Ceq are both functions of frequency. For rigorous design, the equivalent ESR should be evaluated at the ripple frequency for voltage ripple calculation when both ceramic and electrolytic capacitors are used. If $R_{1a} = R_{1b}$

= R_1 and $C_{1a} = C_{1b} = C_1$, then R_{eq} and C_{eq} will be frequency-independent and

$$R_{eq} = 1/2\ R_1 \text{ and } C_{eq} = 2C_1$$

Input Capacitor (C_{in})

The input supply to the converter usually comes from a pre-regulator. Since the input supply is not ideal, input capacitors are needed to filter the current pulses at the switching frequency. A simple buck converter is shown in Figure 3.

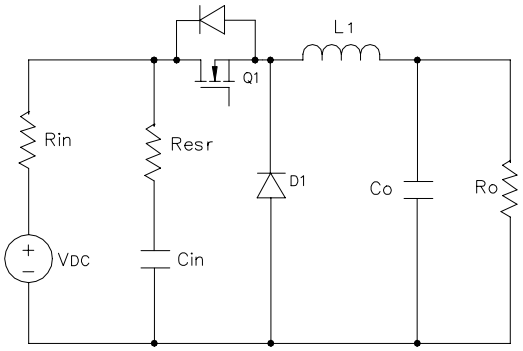


Figure 3. A simple model for the converter input

In Figure 3 the DC input voltage source has an internal impedance R_{in} and the input capacitor C_{in} has an ESR of R_{esr}. MOSFET and input capacitor current waveforms, ESR voltage ripple and input voltage ripple are shown in Figure 4.

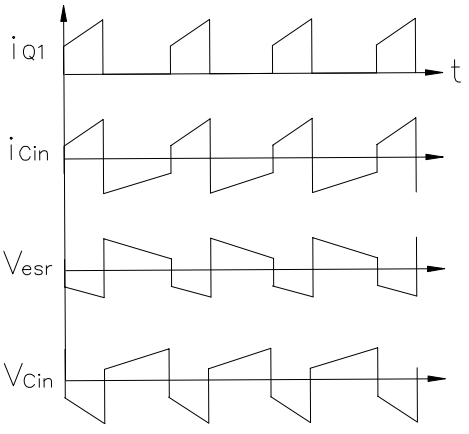


Figure 4. Typical waveforms at converter input.

It can be seen that the current in the input capacitor pulses with high di/dt. Capacitors with low ESL should be used. It is also important to place the input capacitor close to the MOSFET's on the PC board to reduce trace inductances around the pulse current loop.

The RMS value of the capacitor current is approximately

$$I_{Cin} = I_o\sqrt{D[(1+\frac{\delta^2}{12})(1-\frac{D}{\eta})^2 + \frac{D}{\eta^2}(1-D)]}$$

The power dissipated in the input capacitors is then:

$$P_{Cin} = I_{Cin}{}^2 R_{esr}$$

For reliable operation, the maximum power dissipation in the capacitors should not result in more than 10°C of temperature rise. Many manufacturers specify the maximum allowable ripple current (ARMS) rating of the capacitor at a given ripple frequency and ambient temperature. The input capacitance should be high enough to handle the ripple current. For higher power applications, multiple capacitors are placed in parallel to increase the ripple current handling capability.

Sometimes meeting tight input voltage ripple specifications may require the use of larger input capacitance. At full load, the peak-to-peak input voltage ripple due to the ESR is:

$$\Delta v_{ESR} = R_{esr}(1+\frac{\delta}{2})I_o$$

The peak-to-peak input voltage ripple due to the capacitor is:

$$\Delta v_C \approx \frac{DI_o}{C_{in} f_s}$$

From these two expressions, C_{IN} can be found to meet the input voltage ripple specification. In a multi-phase converter, channel interleaving can be used to reduce ripple. The two step-down channels of the SC2453 operate at 180 degrees from each other. If both step-down channels in the SC2453 are connected in parallel, both the input and the output RMS currents will be reduced.

Ripple cancellation effect of interleaving allows the use of smaller input capacitors. When converter outputs are connected in parallel and interleaved, smaller inductors and capacitors can be used for each channel. The total output ripple-voltage remains unchanged. Smaller inductors speeds up output load transient.

When two channels with a common input are interleaved, the total DC input current is simply the sum of the individual DC input currents. The combined input current waveform depends on duty ratio and the output current

waveform. Assuming that the output current ripple is small, the following formula can be used to estimate the *RMS* value of the ripple current in the input capacitor.

Let the duty ratio and output current of Channel 1 and Channel 2 be D_1, D_2 and I_{o1}, I_{o2}, respectively.

If $D_1<0.5$ and $D_2<0.5$, then:

$$I_{Cin} \approx \sqrt{D_1 I_{o1}^2 + D_2 I_{o2}^2}$$

If $D_1>0.5$ and $(D_1-0.5) < D_2<0.5$, then:

$$I_{Cin} \approx \sqrt{0.5 I_{o1}^2 + (D_1 - 0.5)(I_{o1} + I_{o2})^2 + (D_2 - D_1 + 0.5) I_{o2}^2}$$

If $D_1>0.5$ and $D_2 < (D_1-0.5) < 0.5$, then:

$$I_{Cin} \approx \sqrt{0.5 I_{o1}^2 + D_2 (I_{o1} + I_{o2})^2 + (D_1 - D_2 - 0.5) I_{o2}^2}$$

If $D_1>0.5$ and $D_2 > 0.5$, then:

$$I_{Cin} \approx \sqrt{(D_1 + D_2 - 1)(I_{o1} + I_{o2})^2 + (1 - D_2) I_{o1}^2 + (1 - D_1) I_{o2}^2}$$

Choosing Power MOSFET's

Main considerations in selecting the MOSFET's are power dissipation, cost and packaging. Switching losses and conduction losses of the MOSFET's are directly related to the total gate charge (C_g) and channel on-resistance ($R_{ds(on)}$). In order to judge the performance of MOSFET's, the product of the total gate charge and on-resistance is used as a figure of merit (FOM). Transistors with the same FOM follow the same curve in Figure 5.

The closer the curve is to the origin, the lower is the FOM. This means lower switching loss or lower conduction loss or both. It may be difficult to find MOSFET's with both low C_g and low $R_{ds(on}$. Usually a trade-off between $R_{ds(on}$ and C_g has to be made.

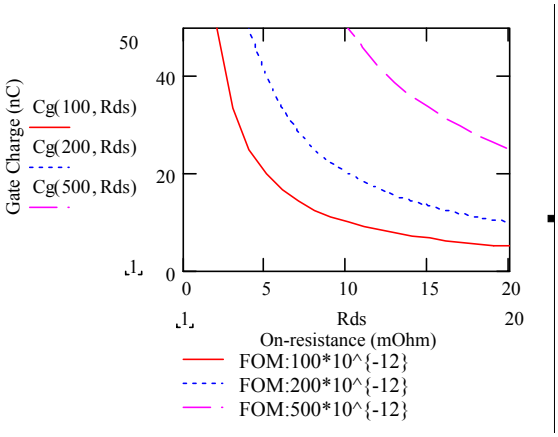


Figure 5. Figure of Merit curves.

MOSFET selection also depends on applications. In many applications, either switching loss or conduction loss dominates for a particular MOSFET. For synchronous buck converters with high input to output voltage ratios, the top MOSFET is hard switched but conducts with very low duty cycle. The bottom switch conducts at high duty cycle but switches at near zero voltage. For such applications, MOSFET's with low C_g are used for the top switch and MOSFET's with low $R_{ds(on)}$ are used for the bottom switch.

MOSFET power dissipation consists of
a) conduction loss due to the channel resistance $R_{ds(on)}$,
b) switching loss due to the switch rise time t_r and fall time t_f, and
c) the gate loss due to the gate resistance R_G.

Top Switch:
The *RMS* value of the top switch current is calculated as:

$$I_{Q1,rms} = I_o \sqrt{D(1 + \frac{\delta^2}{12})}$$

The conduction losses are then:

$$P_{tc} = I_{Q1,rms}^2 R_{ds(on)}$$

$R_{ds(on)}$ varies with temperature and gate-source voltage. Curves showing $R_{ds(on)}$ variations can be found in manufacturers' data sheet. From the Si4860 datasheet, $R_{ds(on)}$ is less than 8mW when V_{gs} is greater than 10V. However $R_{ds(on)}$ increases by 50% as the junction temperature increases from 25°C to 110°C.

The switching losses can be estimated using the simple formula

$$P_{ts} = \frac{1}{2}(t_r + t_f)(1+\frac{\delta}{2})I_o V_{in} f_s$$

where t_r is the rise time and t_f is the fall time of the switching process. Different manufactures have different definitions and test conditions for t_r and t_f. To clarify these, we sketch the typical MOSFET switching characteristics under clamped inductive mode in Figure 6.

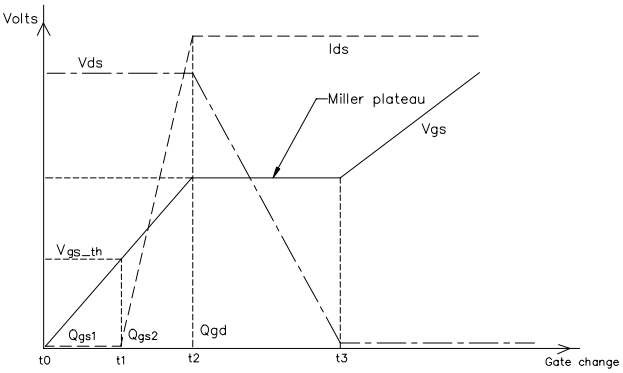


Figure 6. MOSFET switching characteristics

Where,

Q_{gs1} is the gate charge needed to bring the gate-to-source voltage V_{gs} to the threshold voltage V_{gs_th},

Q_{gs2} is the additional gate charge required for the switch current to reach its full-scale value I_{ds} and

Q_{gd} is the charge needed to charge gate-to-drain (Miller) capacitance when V_{ds} is falling.

Switching losses occur during the time interval [t_1, t_3]. Defining $t_r = t_3 - t_1$ and t_r can be approximated as:

$$t_r = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{cc} - V_{gsp}}$$

where R_{gt} is the total resistance from the driver supply rail to the gate of the MOSFET. It includes the gate driver internal impedance R_{gi}, external resistance R_{ge} and the gate resistance R_g within the MOSFET i.e.:

$$R_{gt} = R_{gi} + R_{ge} + R_g$$

V_{gsp} is the Miller plateau voltage shown in Figure 11. Similarly an approximate expression for t_f is:

$$t_f = \frac{(Q_{gs2} + Q_{gd})R_{gt}}{V_{gsp}}$$

Only a portion of the total losses $P_g = Q_g V_{cc} f_s$ is dissipated in the MOSFET package. Here Q_g is the total gate charge specified in the datasheet. The power dissipated within the MOSFET package is:

$$P_{tg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s$$

The total power loss of the top switch is then:

$$P_t = P_{tc} + P_{ts} + P_{tg}$$

If the input supply of the power converter varies over a wide range, then it will be necessary to weigh the relative importance of conduction and switching losses. This is because conduction losses are inversely proportional to the input voltage. Switching loss however increases with the input voltage. The total power loss of MOSFET should be calculated and compared for high-line and low-line cases. The worst case is then used for thermal design.

Bottom Switch:

The *RMS* current in bottom switch can be shown to be:

$$I_{Q2,rms} = I_o\sqrt{(1-D)(1+\frac{\delta^2}{12})}$$

The conduction losses are then:

$$P_{bc} = I_{Q2,rms}{}^2 R_{ds(on)}$$

where $R_{ds(on)}$ is the channel resistance of bottom MOSFET. If the input voltage to output voltage ratio is high (e.g. V_{in}=12V, V_o=1.5V), the duty ratio D will be small. Since the bottom switch conducts with duty ratio (1-D), the corresponding conduction losses can be quite high.

Due to non-overlapping conduction between the top and the bottom MOSFET's, the internal body diode or the external Schottky diode across the drain and source terminals always conducts prior to the turn on of the bottom MOSFET. The bottom MOSFET switches on with only a diode voltage between its drain and source terminals. The switching loss is:

$$P_{bs} = \frac{1}{2}(t_r + t_f)(1+\frac{\delta}{2})I_o V_d f_s$$

is negligible due to near zero-voltage switching.

The gate losses are estimated as :

$$P_{bg} = \frac{R_g}{R_{gt}} Q_g V_{cc} f_s$$

The total bottom switch losses are then:

$$P_b = P_{bc} + P_{bs} + P_{bg}$$

Once the power losses P_{loss} for the top (P_t) and bottom (P_b) MOSFET's are known, thermal and package design at component and system level should be done to verify that the maximum die junction temperature ($T_{j,max}$, usually 125°C) is not exceeded under the worst-case condition. The equivalent thermal impedance from junction to ambient (θ_{ja}) should satisfy:

$$\theta_{ja} \le \frac{T_{j,max} - T_{a,max}}{P_{loss}}$$

θ_{ja} depends on the die to substrate bonding, packaging material, the thermal contact surface, thermal compound property, the available effective heat sink area and the air flow condition (free or forced convection). Actual temperature measurement of the prototype should be carried out to verify the thermal design.

Setting the Output Voltage

The non-inverting input of the channel-one error amplifier is internally tied the 0.5V voltage reference output. A simple voltage divider (R_{o1} at top and R_{o2} at bottom) sets the converter output voltage. The voltage feedback gain $h=0.5/V_o$ is related to the divider resistors value as:

$$R_{o2} = \frac{h}{1-h} R_{o1}$$

Once either R_{o1} or R_{o2} is chosen, the other can be calculated for the desired output voltage V_o. Since the number of standard resistance values is limited, the calculated resistance may not be available as a standard value resistor. As a result, there will be a set error in the converter output voltage. This non-random error is caused by the feedback voltage divider ratio. It cannot be corrected by the feedback loop.
The following table lists a few standard resistor combinations for realizing some commonly used output voltages.

Only the voltages in boldface can be precisely set with standard 1% resistors.

From this table, one may also observe that when the value:

$$\frac{1-h}{h} = \frac{V_o - 0.5}{0.5}$$

Vo (V)	**0.6**	0.9	**1.2**	**1.5**	1.8	2.5	3.3
(1-h)/h	**0.2**	0.8	**1.4**	**2**	2.6	4	5.6
Ro1 (Ohm)	**200**	806	**1.4K**	**2K**	2.61K	4.02K	5.62K
Ro2 (Ohm)	**1K**	1K	**1K**	**1K**	1K	1K	1K

and its multiples fall into the standard resistor value chart (1%, 5% or so), it is possible to use standard value resistors to exactly set up the required output voltage value.
The input bias current of the error amplifier also causes an error in setting the output voltage. The maximum inverting input bias currents of error amplifiers 1 or 2 is 200nA. Since the non-inverting input is biased to 0.5V, the percentage error in the second output voltage will be $100\% \bullet (0.2uA)\ R_{01} \bullet R_{o2} / [0.5 \bullet (R_{o1} + R_{o2})]$.

Valley Current Sensing for Current-Limit

The valley current sensing for current limiting is a unique scheme which could sense the voltage across the bottom switch MOSFET when it is on. The scheme is robust with good noise immunity due to reference to ground.

The current sensing point is at a delay time t_{dv} before the beginning of a switching cycle. Therefore, the actual valley current is:

$$I_V = -\frac{V_o}{R_{DS(ON)\_B} + R_L}\left(1 - e^{-\frac{t_{dv}}{\tau_2}}\right) + I_{VS} e^{-\frac{t_{dv}}{\tau_2}}$$

where, I_{VS} is the preset valley current limiting threshold.

If a sensed current exceeds the threshold, the top switch will keep off in the next cycle until the current goes back below the threshold. In steady state, since the output voltage is out of regulation in over current condition, the control loop will try to make maximum duty cycle for the top switch as it is on, which is usually greater than 80%. Therefore, as the current falls back below the threshold, it is on in the next almost full cycle. The peak current is not controlled and only depends upon circuit parameters and operating condition in this cycle. The peak current I_P is:

$$I_P = \frac{V_{in} - V_o}{R_{DS(ON)\_T} + R_L}\left(1 - e^{-\frac{T}{\tau_1}}\right) + I_V e^{-\frac{T}{\tau_1}}$$

Where, T is switching cycle period.

Because the inductor current ramps up according to Vin –Vo, and down with Vo, a falling output voltage in over current condition moves the inductor “ramp up” current up faster and the peak current I_p larger but the “ramp down” current slower. As long as the current is still larger than the current limiting threshold, the top switch is held off. The switching frequency is folded back lower but average current is relatively still high.

An example is shown in Typical Characteristics section with input voltage 12V and output voltage 5V with output current 3.5A.

The preset valley current limit is 5A, which has to be greater than full load current 3.5. When the output is shorted, the inductor peak current and the load current, both are a function of the input voltage and the output inductance, would be higher than the current limit. Therefore, proper thermal management and inductor saturation current rating have to be considered at the worst conditions.

Loop Compensation

SC2453 is a voltage mode buck controller with high gain bandwidth error amplifier utilizing external network compensation to regulate output voltage.

For a DC/DC converter, it is usually required that the converter has a loop gain of a high crossover frequency for fast load response, high DC and low frequency gain for low steady state error, and enough phase margin for its operating stability. Often one can not have all these properties at the same time. The purpose of the loop compensation is to arrange the poles and zeros of the compensation network to meet the requirements for a specific application.

The power stage of a buck converter control-to-output transfer function is as shown below:

$$G_{VD}(s) = V_{IN}\frac{1+sR_CC}{1+s\frac{L}{R}+s^2LC}$$

where,

$$\omega_O = \frac{1}{\sqrt{LC}}$$

L - Output inductance

C - Output capacitance

R_C - Output capacitor ESR

V_{IN} - Input voltage

The transfer function of the error amplifier with external compensation network is as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s}\cdot\frac{(1+\frac{s}{\omega_{Z1}})(1+\frac{s}{\omega_{Z2}})}{(1+\frac{s}{\omega_{P1}})(1+\frac{s}{\omega_{P2}})}$$

where,

$$\omega_{Z1} = \frac{1}{R_2C_1}, \omega_{Z2} = \frac{1}{(R_1+R_3)C_2}$$

$$\omega_I = \frac{1}{R_1(C_1+C_3)}, \omega_{P1} = \frac{1}{R_3C_2}, \omega_{P2} = \frac{1}{R_2\frac{C_1C_3}{C_1+C_3}}$$

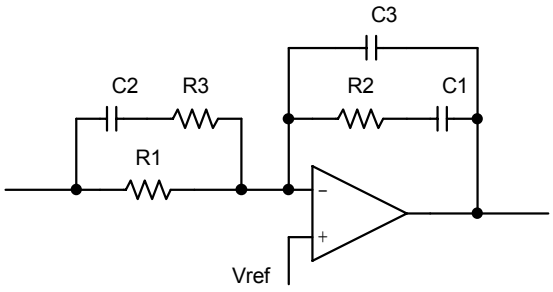


Figure 7. Voltage Mode Buck Converter Compensation Network

With the compensation, the converter total loop gain is as follows:

$$T(s) = G_{PWM}\cdot G_{COMP}(s)\cdot G_{VD}(s) = \frac{\frac{1}{V_M}\cdot\omega_I\cdot V_I}{s}\cdot\frac{1+\frac{s}{\omega_{Z1}}}{1+\frac{s}{\omega_{P1}}}\cdot\frac{1+\frac{s}{\omega_{Z2}}}{\cdot 1+\frac{s}{\omega_{P2}}}\cdot\frac{1+\frac{s}{\frac{1}{R_C\cdot C_4}}}{1+s\frac{L_1}{R}+s^2L_1C}$$

Where:

G_{PWM} = PWM gain

V_M = 3.0V, ramp peak to valley voltage of SC2453

The design guidelines are as following:

1. Set the loop gain crossover frequency ω_C less than1/5th the switching frequency.
2. Place an integrator in the origin to increase DC and low frequency gains.

3. Select ω_{Z1} and ω_{Z2} such that they are placed near ω_0 to dampen peaking; the loop gain has –20dB rate to go across the 0dB line for obtaining a wide bandwidth.
4. Cancel ω_{ESR} with compensation pole ω_{P1} ($\omega_{P1} = \omega_{ESR}$).
5. Place a high frequency compensation pole ω_{P2} at the half switching frequency to get the maximum attenuation of the switching ripple and the high frequency noise with the adequate phase lag at ω_C.

The compensated loop gain will be as given in Figure 8:

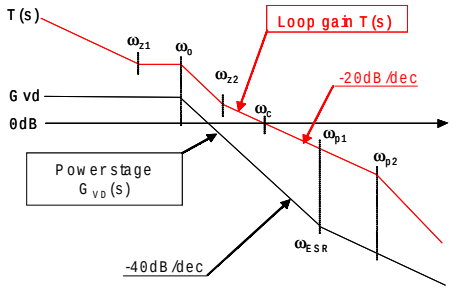


Figure 8. Asymptotic diagram of buck power stage and its compensated loop gain.

Positive and Negative LDO Controllers

The SC2453 provides positive and negative adjustable linear regulator controllers. The positive linear regulator uses a PNP transistor to regulate output voltage. This is set by a voltage divider connected from the output to FB to AGND. Referring to the front page Application Circuit, select R10 in the 5KΩ to 20KΩ range. Calculate R9 with the following equation:

$$R_9 = R_{10}\left(\frac{V_{OUT}}{0.5} - 1\right)$$

The negative linear regulator uses a NPN transistor to regulate output voltage. This is set by a voltage divider connected from the output to FB to a positive reference. Referring to the front page Application Circuit, select R18 in the 5KΩ to 20KΩ range. Calculate R14 with the following equation:

$$P_{14} = P_{18}\left(\frac{V_{OUT}}{V_{REF}}\right)$$

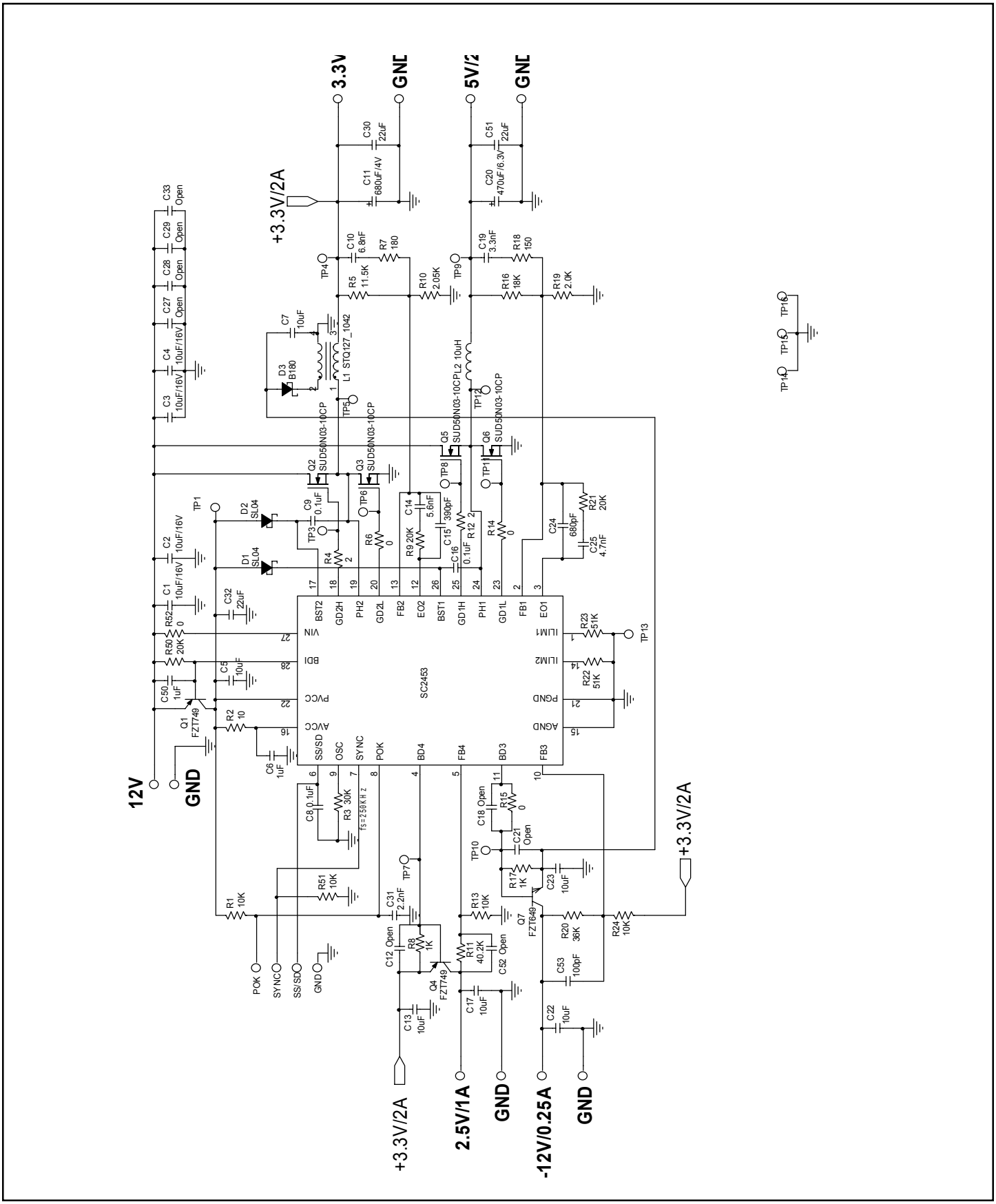
The maximum voltage to drive an NPN transistor is AVCC minus the voltage drop across the internal P-MOSFET which is the product of On-Resistance and sourcing current. The maximum driving voltage with 5mA sourcing current is minimum AVCC (4.5V) minus 5mA times maximum On-Resistance 140Ω, i.e. 3.8V.

Layout Guidelines

In order to achieve optimal electrical, thermal and noise performance for high frequency converters, attention must be paid to the PCB layouts. The goal of layout optimization is to place components properly and identify the high di/dt loops to minimize them. The following guideline should be used to ensure proper functions of the converters.

1. A ground plane is recommended to minimize noises and copper losses, and maximize heat dissipation.
2. Start the PCB layout by placing the power components first. Arrange the power circuit to achieve a clean power flow route. Put all the connections on one side of the PCB with wide copper filled areas if possible.
3. The PVCC and AVCC bypass capacitors should be placed next to the PVCC, AVCC and PGND, AGND pins respectively.
4. Separate the power ground from the signal ground. In SC2453, the power ground PGND should be tied to the source terminal of lower MOSFETs. The signal ground AGND should be tied to the negative terminal of the output capacitor.
5. The trace connecting the feedback resistors to the output should be short, direct and far away from the noise sources such as switching node and switching components. Minimize the traces between DRXH/DRXL and the gates of the MOSFETs to reduce their impedance to drive the MOSFETs.
7. Minimize the loop including input capacitors, top/bottom MOSFETs. This loop passes high di/dt current. Make sure the trace width is wide enough to reduce copper losses in this loop.
8. Maximize the trace width of the loop connecting the inductor, bottom MOSFET and the output capacitors.
9. Connect the ground of the feedback divider and the compensation components directly to the GND pin of the SC2453 by using a separate ground trace. Then connect this pin to the ground of the output capacitor as close as possible.

Evaluation Board Schematic



Bill of Materials - Evaluation Board

Item	Quantity	Reference	Part	Manufacturer	Manufacturer #	Foot Print
1	4	C1,C2,C3,C4	10uF/16V	TDK	C3216X5R1C106MT	SM/C_1206
2	1	C5	10uF			SM/C_0805
3	2	C6,C50	1uF			SM/C_0805
4	5	C7,C13,C17,C22,C23	10uF	TDK	C3216X5R1C106MT	SM/C_1206
5	1	C8	0.1uF			SM/R_0805
6	2	C16	0.1uF			SM/C_0805
		C9	0.1uF			SM/C_0805
7	1	C10	0.01uF			SM/C_0805
8	1	C11	680uF/4V	SANYO	4TPB680M	SM/CT_7343
9	4	C12	Open			SM/C_0805
		C18	Open			SM/C_0805
		C21	Open			SM/C_0805
		C52	Open			SM/C_0805
10	1	C14	8.2nF			SM/C_0805
11	2	C24	680pF			SM/C_0805
		C15	680pF			SM/C_0805
12	1	C19	3.3nF			SM/C_0805
13	1	C20	470uF/6.3V	SANYO	6TPB470M	SM/CT_7343
14	1	C25	4.7nF			SM/C_0805
15	4	C27	Open			SM/C_1210
		C28	Open			SM/C_1210
		C29	Open			SM/C_1210
		C33	Open			SM/C_1210
16	3	C30	22uF			SM/C_1210
		C32	22uF			SM/C_1210
		C51	22uF			SM/C_1210
17	1	C31	2.2nF			SM/C_0805
18	1	C53	100pF			SM/C_0805
19	2	D2	SL04	VISAY	SL04	SOD123
		D1	SL04	VISAY	SL04	SOD123
20	1	D3	B150	VISAY	SS15	SM/_SMB
28	1	L1	STQ127_1042	DELTA	STQ127_1042	
29	1	L2	10uH	COILCRAFT	DO5022P-103	DO5022
30	2	Q4	FZT749	ZETEX	FZT749TA	SM/SOT223
		Q1	FZT749	ZETEX	FZT749TA	SM/SOT223
31	4	Q2	SUD50N03-10CP	VISHAY	SUD50N03-10CP	SM/_DPAK
		Q3	SUD50N03-10CP	VISHAY	SUD50N03-10CP	SM/_DPAK
		Q5	SUD50N03-10CP	VISHAY	SUD50N03-10CP	SM/_DPAK
		Q6	SUD50N03-10CP	VISHAY	SUD50N03-10CP	SM/_DPAK
32	1	Q7	FZT649	ZETEX	FZT649	SM/SOT223
33	4	R1	10K			SM/R_0805
		R13	10K			SM/R_0805
		R24	10K			SM/R_0805
		R51	10K			SM/R_0805
34	1	R2	10			SM/R_0805
35	1	R3	30K			SM/R_0805
36	2	R4	2			SM/R_0805
		R12	2			SM/R_0805
37	1	R5	11.3K			SM/R_0805

Bill of Materials - Evaluation Board

38	3	R6	0			SM/R_0805
		R14	0			SM/R_0805
		R15	0			SM/R_0805
39	1	R7	470			SM/R_0805
40	2	R8	1K			SM/R_0805
		R17	1K			SM/R_0805
41	4	R9	20K			SM/R_0805
		R16	20K			SM/R_0805
		R21	20K			SM/R_0805
		R50	20K			SM/R_0805
42	1	R10	2.0K			SM/R_0805
43	1	R11	40.2K			SM/R_0805
44	1	R18	150			SM/R_0805
45	1	R19	2.21K			SM/R_0805
46	1	R20	36K			SM/R_0805
47	2	R23	51K			SM/R_0805
		R22	51K			SM/R_0805
48	1	R52	0			SM/R_0805
49	1	U1	SC2453	SEMTECH	SC2453	TSSOP-28