SC3102

2A Synchronous Step-Down Regulator

POWER MANAGEMENT

Features

- V_{IN} Range: 2.9 – 5.5V
- Preset V_{OUT} Range: 1.0V to 3.3V
- Up to 2A Output Current
- Ultra-Small Footprint, <1mm Height
- 1.5MHz Switching Frequency
- Selectable Forced PSAVE or Forced PWM Operation
- Efficiency Up to 95%
- Low Output Noise Across Load Range
- Excellent Transient Response
- Start Up into Pre-Bias Output
- 100% Duty-Cycle Low Dropout Operation
- <1µA Shutdown Current
- Externally Programmable Soft-Start Time
- Power Good indicator
- Input Under-Voltage Lockout
- Output Over-Voltage, Current Limit Protection
- Over-Temperature Protection
- 3mm x 3mm x 0.6mm thermally enhanced MLPQ-UT16 package
- -40 to +85°C Temperature Range
- Pb-free, Halogen free, and RoHS/WEEE compliant

Applications

- Office Automation
- Switches and Routers
- Network Cards
- LCD TV

Description

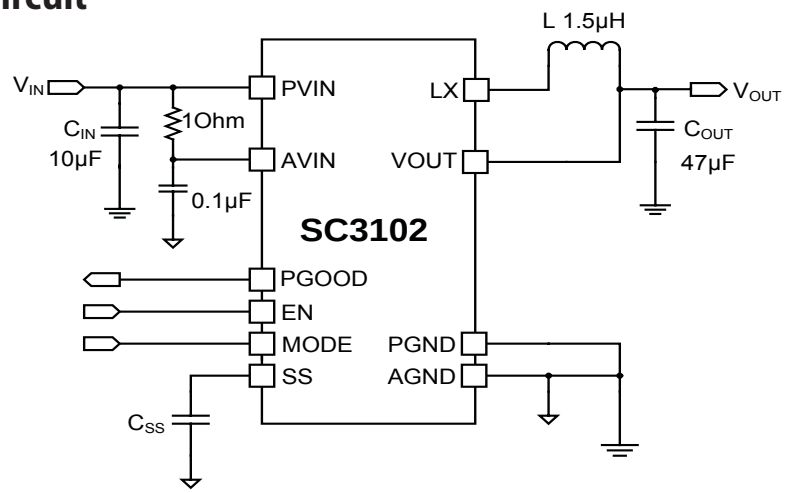
The SC3102 is a 2A synchronous step-down regulator designed to operate with an input voltage range of 2.9V to 5.5V. The device requires minimal external components for a complete step down regulator solution. The output voltage is factory predetermined with an available range of 1.0V to 3.3V.

The SC3102 is optimized for maximum efficiency over a wide range of load currents. During full load operation, the SC3102 operates in forced PWM mode with a fixed 1.5MHz oscillator frequency, allowing the use of small surface mount external components. As the load decreases, the regulator has the option to transition, via the MODE pin, into forced Power Save mode to maximize efficiency or to stay in forced PWM mode.

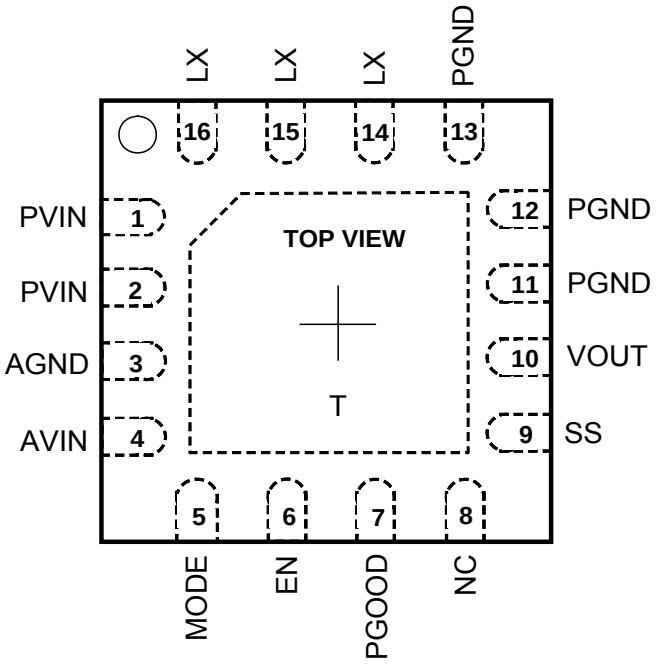
The SC3102 offers output short circuit and thermal protection to safe guard the device under extreme operating conditions. The enable pin provides on/off control of the regulator. When connected to logic low, the device enters shutdown and consumes less than 1µA of current. Other protection features include programmable soft-start with Power Good indicator, over voltage protection and under voltage lockout.

The SC3102 is available in a thermally-enhanced, 3mm x 3mm x 0.6mm MLPQ-UT16 package and has a rated temperature range of -40 to +85°C.

Typical Application Circuit



Pin Configuration



3mm x 3mm x 0.6mm MLPQ-UT16

θ_{JA} = 40°C/W (1); θ_{JC} = 7°C/W

Ordering Information

Device	Package
SC3102xULTRT(2)(3)(4)	3mm x 3mm x 0.6mm MLPQ-UT16
SC3102xEVB(5)	Evaluation Board

Notes:

(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

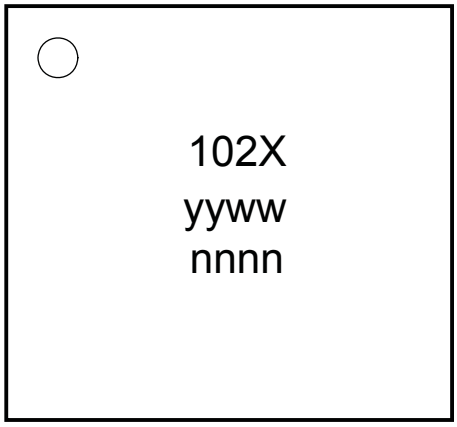
(2) Available in tape and reel only. A reel contains 3,000 devices.

(3) Device is Pb-free, Halogen free, and RoHS/WEEE compliant.

(4) "x" is the code of the output voltage. See Table 1 for the code. For example, the device number for VOUT= 1.50V is SC3102HULTRT.

(5) "x" is the code of the output voltage. See Table 1 for the code. For example, the EVB with VOUT= 1.50V is SC3102HEVB.

Marking Information



Marking for 3mm x 3mm MLPQ-UT 16 Lead Package:
x = Code of the output voltage (Example: H for VOUT=1.50V)
yyww = Datecode (Example: 0852)
nnnn = Semtech Lot number (Example: E901)

Table 1: Available Output Voltages

Code	VOUT(6)
D	1.10
E	1.20
H	1.50

Notes:

(6) Contact Semtech marketing for alternative output voltage options.

Absolute Maximum Ratings

PVIN and AVIN Supply Voltages ..... -0.3 to 6.0V
LX Voltage[9] ..... -0.3 to PVIN+0.3V, 6V Max
VOUT Voltage ..... -0.3 to AVIN+0.3V
CTLx pins Voltages ..... -0.3 to AVIN+0.3V
Peak IR Reflow Temperature ..... 260°C
ESD Protection Level[8] 2kV

Recommended Operating Conditions

Supply Voltage PVIN and AVIN ..... 2.9 to 5.5V
Maximum DC Output Current 2.0A
Maximum DC Output Current in Forced PSAVE Mode ... 0.35A
Temperature Range ..... -40 to +85°C
Input Capacitor 10µF
Output Capacitor ..... 47µF (or 2 x 22µF)
Output Inductor ..... 1.5 µH

Thermal Information

Thermal Resistance, Junction to Ambient[7] ..... 40 °C/W
Thermal Resistance, Junction to Case ..... 7 °C/W
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65 to +150 °C

Exceeding the absolute maximum ratings may result in permanent damage to the device and/or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

Notes:
(7) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.
(8) Tested according to JEDEC standard JESD22-A114-B.
(9) Due to parasitic board inductance, the transient LX pin voltage at the point of measurement may appear larger than that which exists on silicon. The device is designed to tolerate the short duration transient voltages that will appear on the LX pin due to the deadtime diode conduction, for inductor currents up to the current limit setting of the device.

Electrical Characteristics

Unless specified: PVIN= AVIN= 5.0V, VOUT= 1.50V, C_{IN}= 10µF, C_{OUT}= 2 x 22µF; L= 1.5µH; -40°C≤ T_J ≤ +125 °C; Unless otherwise noted typical values are T_A= +25 °C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under-Voltage Lockout	UVLO	Rising AVIN, PVIN=AVIN	2.70	2.80	2.90	V
		Hysteresis		300		mV
Output Voltage Tolerance[10]	ΔV_{OUT}	PVIN= AVIN= 2.9 to 5.5V; I_{OUT}=0A	-1.25		+1.25	%
Current Limit	I_{LIMIT}	Peak LX current	2.5	3.0	3.75	A
Supply Current	I_Q	No load, MODE= High		12		mA
		No load, MODE= Low		60		µA
Shutdown Current	I_{SHDN}	EN= AGND		1	10	µA
High Side Switch Resistance[11]	R_{DSON_P}	I_{LX}= 100mA, T_J= 25 °C		50	85	mΩ
Low Side Switch Resistance[11]	R_{DSON_N}	I_{LX}= -100mA, T_J= 25 °C		35	60	
L_X Leakage Current[11]	$I_{LK(LX)}$	PVIN= AVIN= 5.5V; LX= 0V; EN= AGND		1	10	µA
		PVIN= AVIN= 5.5V; LX= 0V; EN= AGND	-20	-1		
Load Regulation	$\Delta V_{LOAD-REG}$	PVIN= AVIN= 5.0V, MODE=High, I_{OUT}=1mA to 2A		±0.3		%
Oscillator Frequency	f_{OSC}		1.275	1.5	1.725	MHz
Soft-Start Charging Current[11]	I_{SS}			+5		µA
Foldback Holding Current	I_{CL_HOLD}	Average LX Current		1		A

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Forced PSAVE Mode Current		Maximum output current loading	350			mA
Impedence of PGOOD Low	R_{PGOOD_LO}			10		Ω
PGOOD Threshold	V_{PG_TH}	VOUT rising		90		%
PGOOD Delay	V_{PG_DLY}	Asserted		2		ms
		PGOOD= Low		20		µs
EN Delay	t_{EN_DLY}	From EN Input High to SS starts rising		50		µs
EN Input Current(11)	I_{EN}	EN =AVIN or AGND	-2.0		2.0	µA
EN Input High Threshold	V_{EN_HI}		1.2			V
EN Input Low Threshold	V_{EN_LO}				0.4	V
MODE Input Current(11)	I_{MODE}	MODE= AVIN or AGND	-2.0		2.0	µA
MODE Input High Threshold	V_{MODE_HI}		1.2			V
MODE Input Low Threshold	V_{MODE_LO}				0.4	V
V_{OUT} Over Voltage Protection	V_{OVP}		110	115	120	%
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			10		°C

Notes:

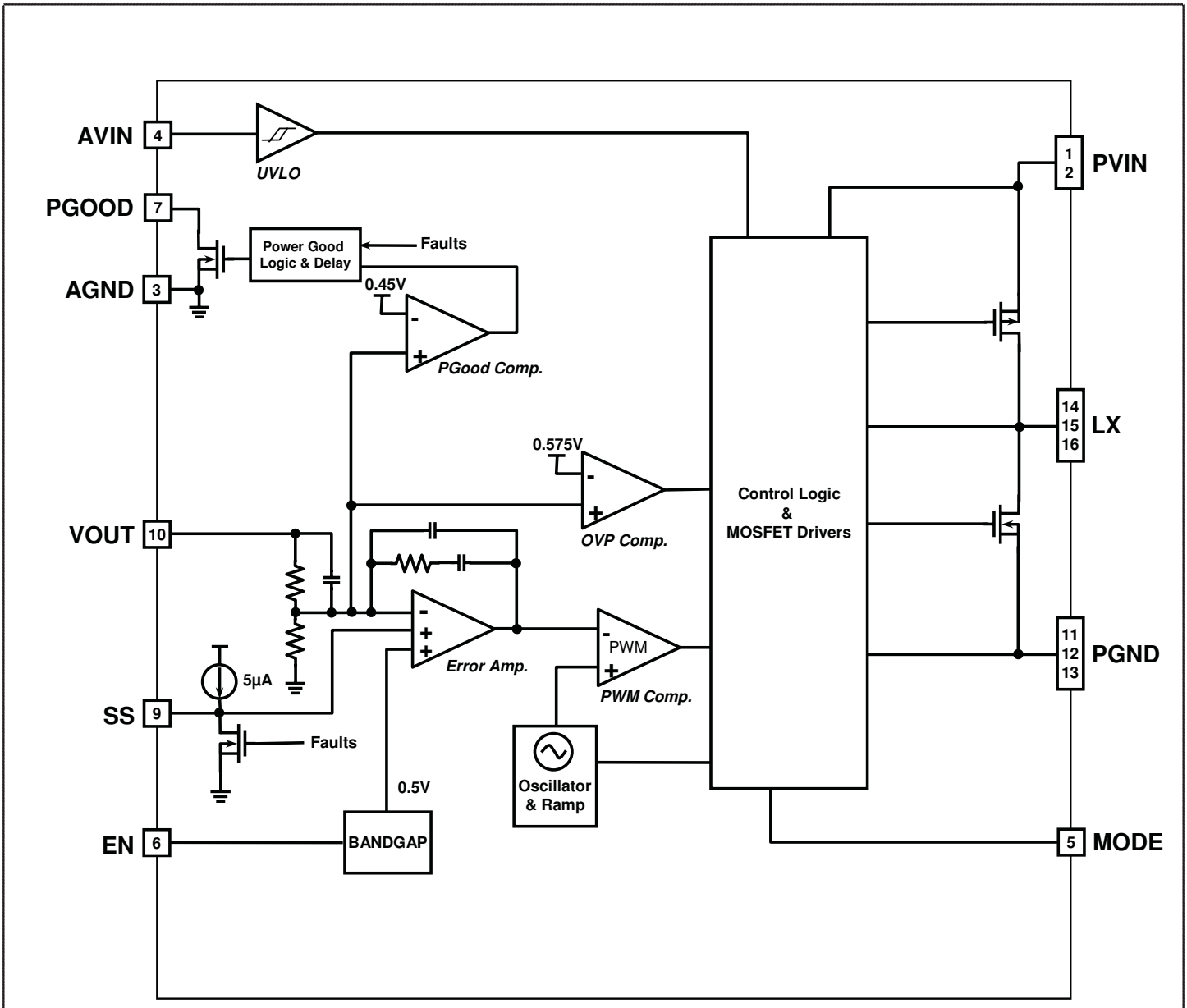
(10) The "Output Voltage Tolerance" includes output voltage accuracy, voltage drift over temperature and line regulation.

(11) A negative current means the current flows into the pin and a positive current means the current flows out from the pin.

Pin Descriptions

Pin #	Pin Name	Pin Function
1,2	PVIN	Input supply voltage for the converter power stage.
3	AGND	Ground connection for the internal circuitry. AGND needs to be connected to PGND directly.
4	AVIN	Power supply for the internal circuitry. AVIN is required to be connected to PVIN through an R-C filter of 1Ω and 100nF.
5	MODE	MODE select pin. When connected to logic high, the device operates in forced PWM mode. When connected to logic low, it operates in forced PSAVE mode at light load. The MODE pin has a 500kΩ internal pulldown resistor. This resistor is switched in circuit whenever the MODE pin is "Low" or when the part is in undervoltage lockout or disabled.
6	EN	Enable pin. When connected to logic high or tied to the AVIN pin, the SC3102 is on. When connected to logic low, the device enters shutdown and consumes less than 1µA current (typ.). The enable pin has a 500kΩ internal pulldown resistor. This resistor is switched in circuit whenever the EN pin is "Low" or when the part is in undervoltage lockout.
7	PGOOD	Power good indicator. When the output voltage reaches the PGOOD threshold, this pin will be open-drain (after the PGOOD delay), otherwise it is pulled low internally.
8	NC	No connection.
9	SS	Soft-Start. Connect a soft-start capacitor to program the soft-start time. There is a 5µA charging current flowing out of the pin.
10	VOUT	Output voltage sense pin.
11,12,13	PGND	Ground connection for converter power stage.
14,15,16	LX	Switching node - connect an inductor between this pin and the output capacitor.
T	Thermal Pad	Thermal pad for heatsinking purposes. Connection to PGND is recommended. It is not connected internally.

Block Diagram

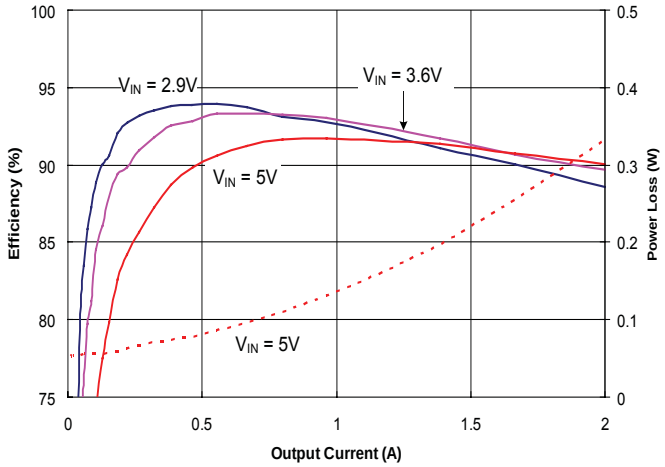


SEMTECH

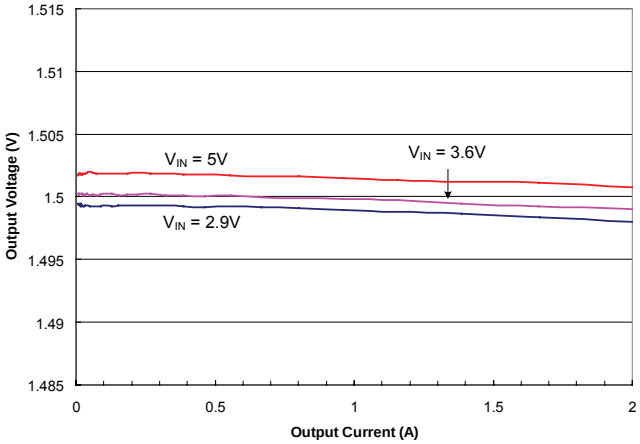
Typical Characteristics

Circuit Conditions: C_{IN}= 10µF/6.3V, C_{OUT}= 2 x 22µF/6.3V, C_{SS}= 2.2nF, L= 1.5µH.

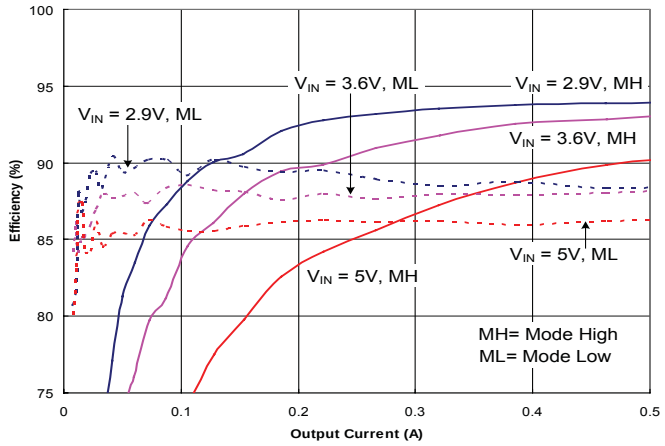
Efficiency and Power Loss: MODE = High



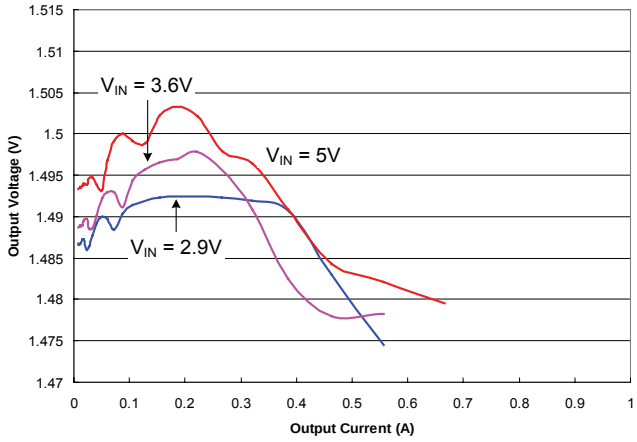
Load Regulation: MODE = High



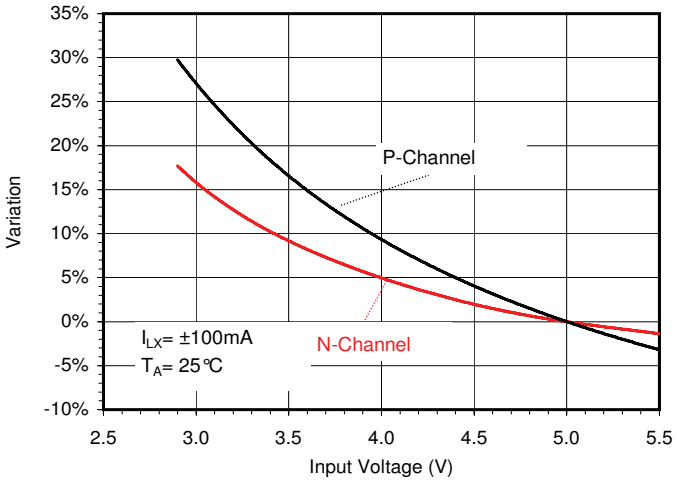
Efficiency Comparison: MODE - High vs Low



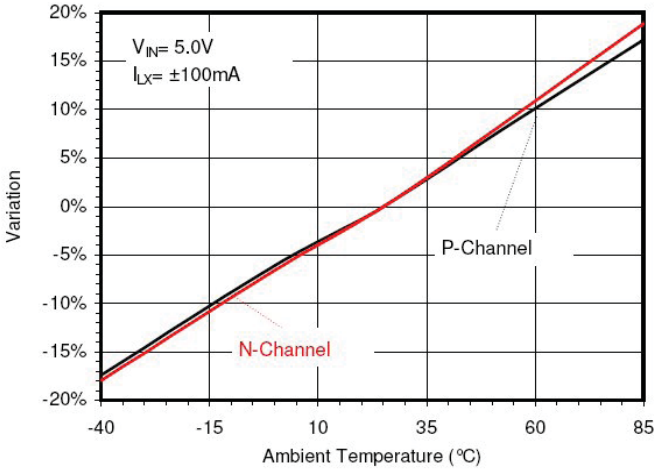
Load Regulation: MODE = Low



$R_{DS(ON)}$ Variation vs. Input Voltage



$R_{DS(ON)}$ Variation vs. Temperature

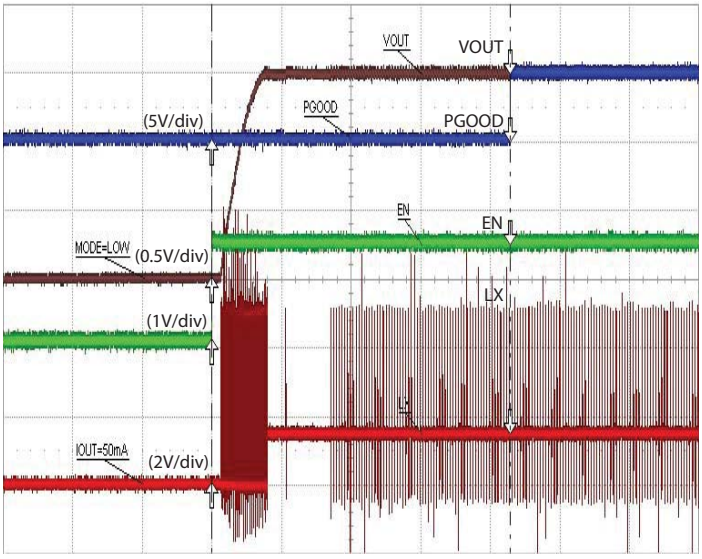


Typical Waveforms

Circuit Conditions: C_{IN}= 10µF/6.3V, C_{OUT}= 2 x 22µF/6.3V, C_{SS}= 2.2nF, L= 1.5µH.

Start Up: MODE = Low

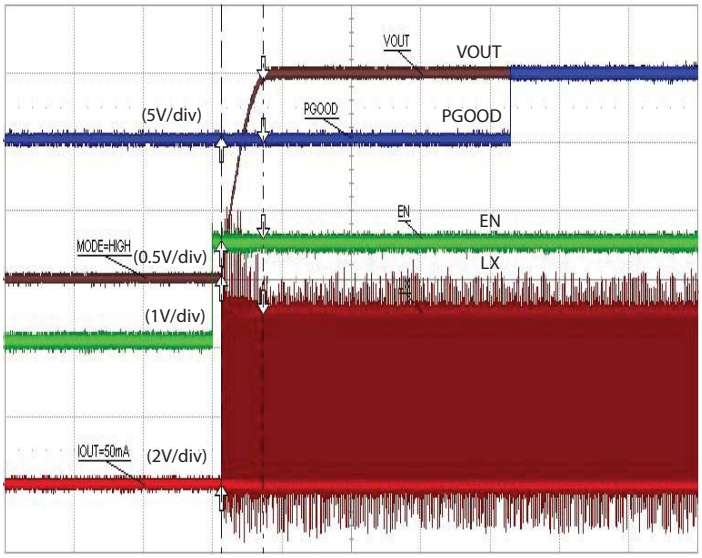
V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 50mA



Time (500µs/div)

Start Up: MODE = High

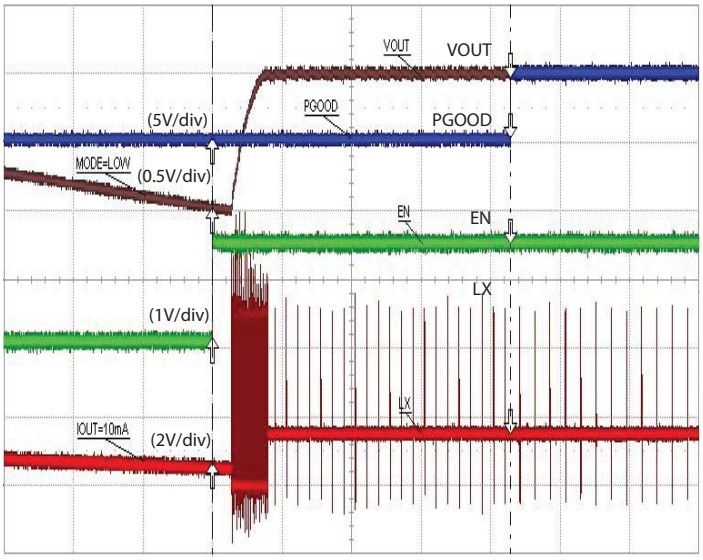
V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 50mA



Time (500µs/div)

Pre-bias Start Up: MODE = Low

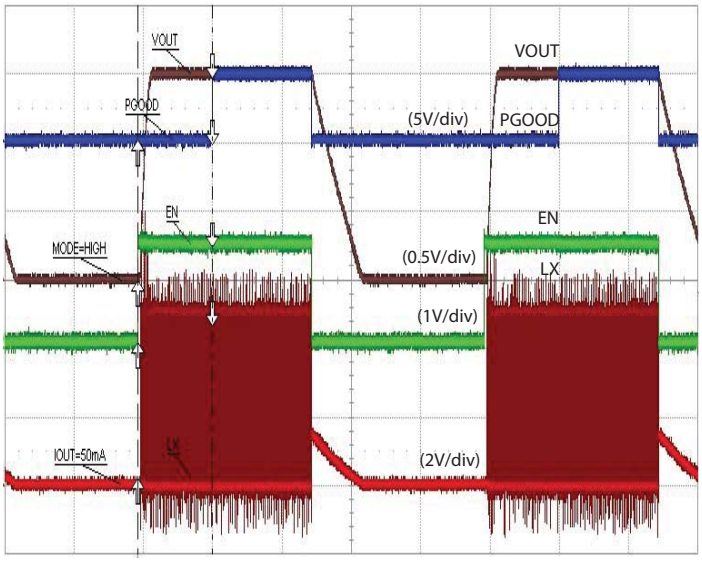
V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 10mA



Time (500µs/div)

Start Up and Shutdown: MODE = High

V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 50mA



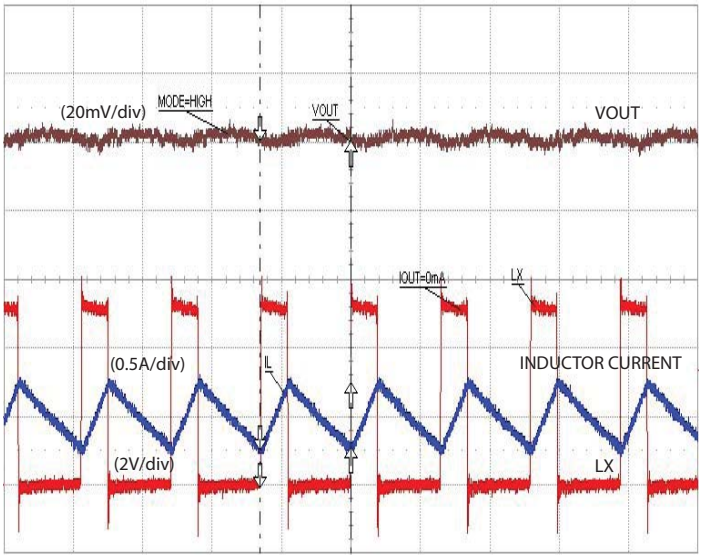
Time (500µs/div)

Typical Waveforms (continued)

Circuit Conditions: C_{IN}= 10µF/6.3V, C_{OUT}= 2 x 22µF/6.3V, C_{SS}= 2.2nF, L= 1.5µH.

Steady State: MODE = High

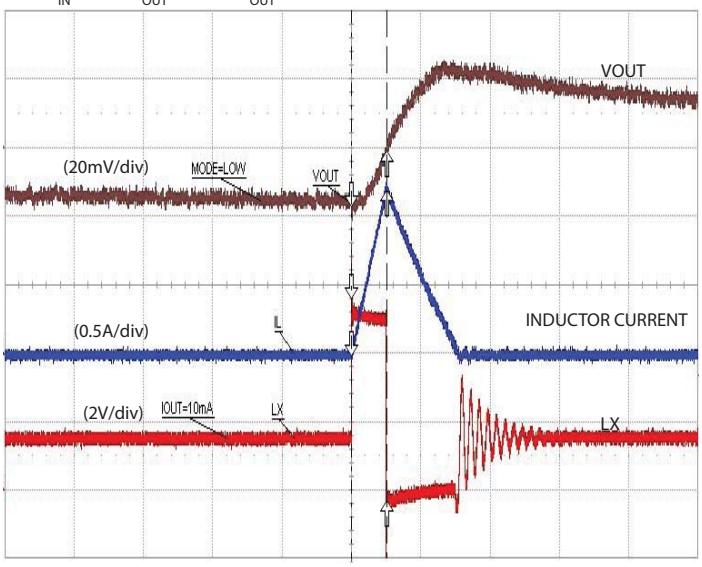
V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 0A



Time (500ns/div)

Steady State: MODE = Low

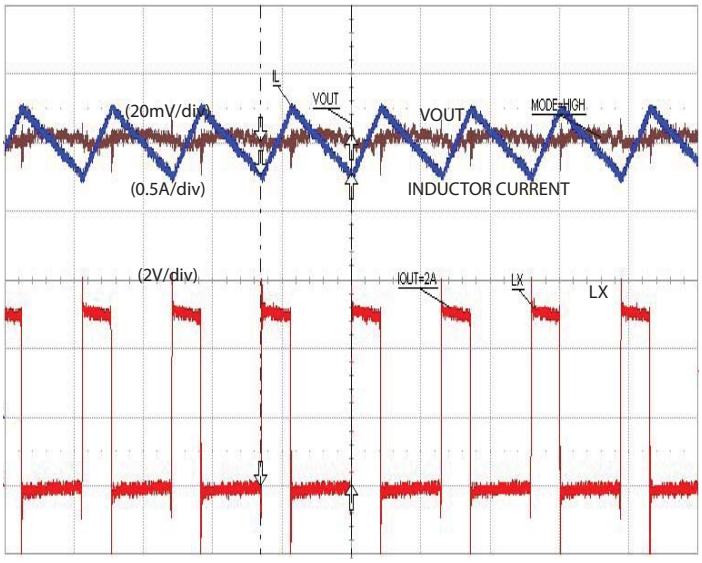
V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 10mA



Time (1µs/div)

Steady State: MODE = High

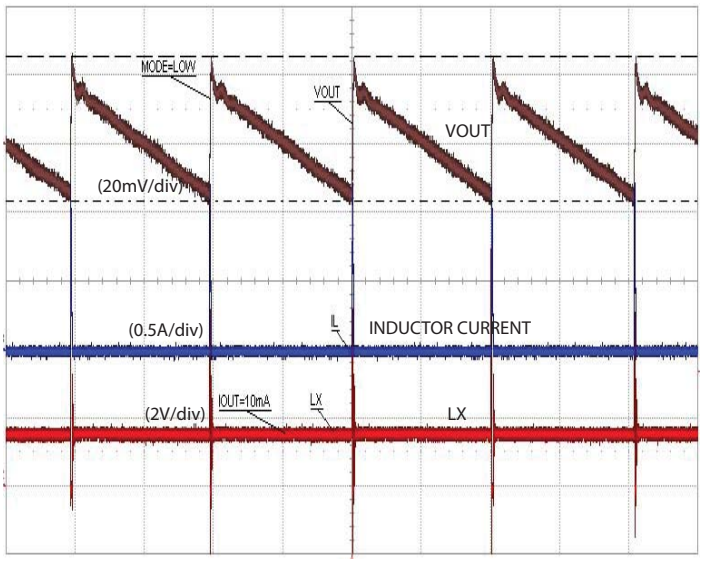
V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 2A



Time (500ns/div)

Steady State: MODE = Low

V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 10mA



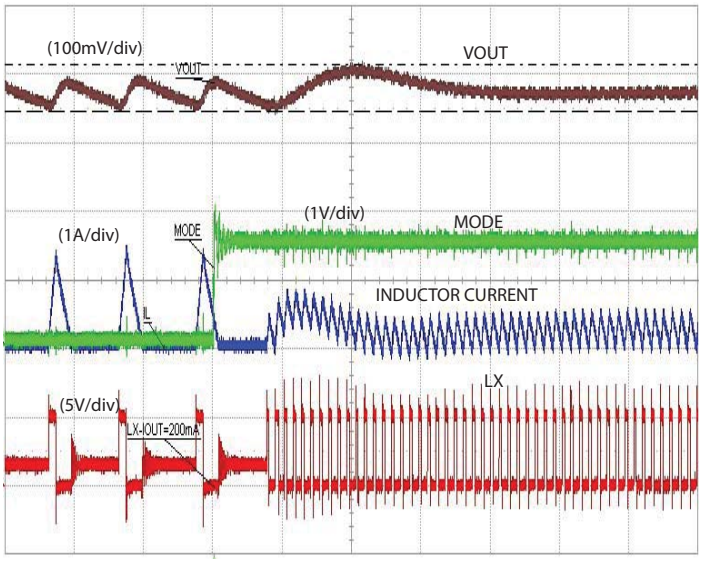
Time (50µs/div)

Typical Waveforms (continued)

Circuit Conditions: C_{IN}= 10µF/6.3V, C_{OUT}= 2 x 22µF/6.3V, C_{SS}= 2.2nF, L= 1.5µH.

MODE changing from Low to High

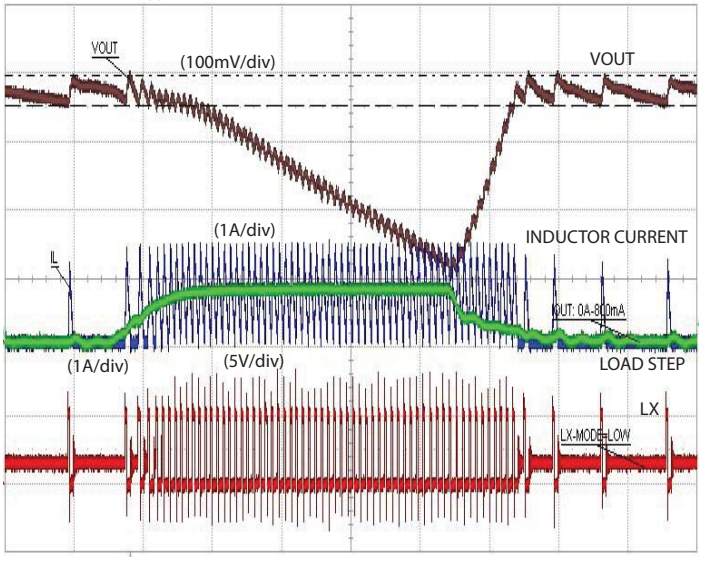
V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 200mA DC



Time (5µs/div)

Overload Recovery When MODE is Low

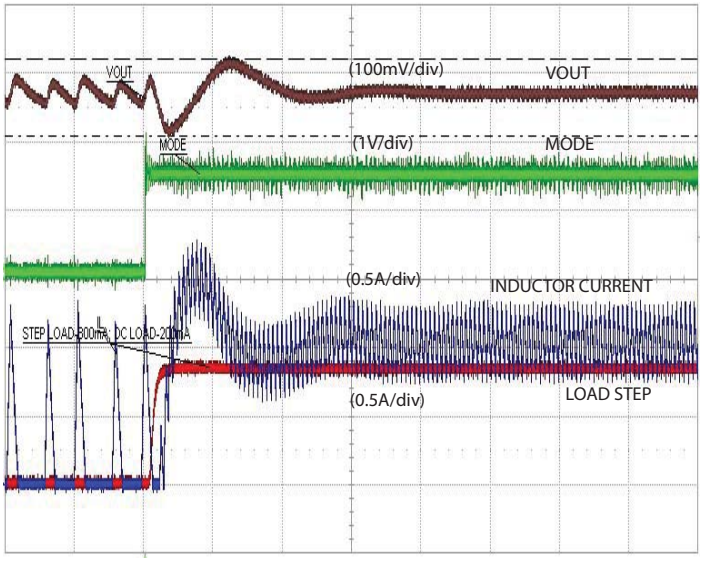
V_{IN} = 5V, V_{OUT} = 1.5V, Load Step = 0A to 800mA to 0A



Time (20µs/div)

MODE Change and Load Step

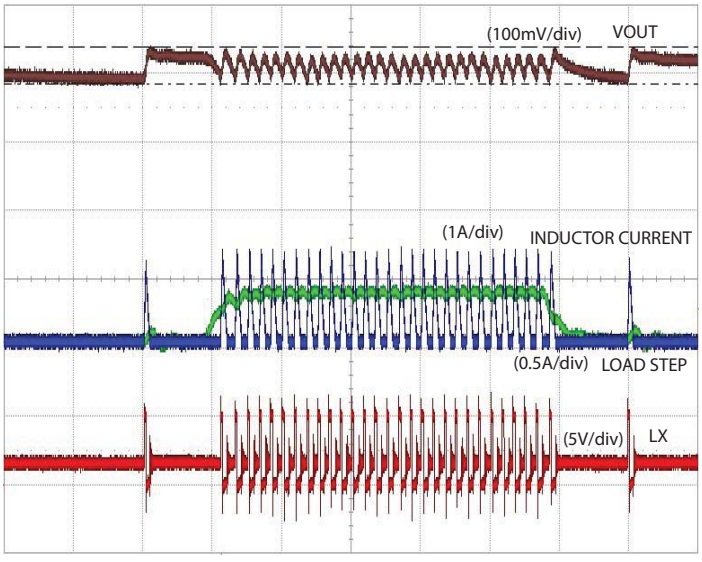
V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 200mA DC, Load Step = 800mA



Time (500µs/div)

Load Step during MODE = Low

V_{IN} = 5V, V_{OUT} = 1.5V, Load Step = 0A to 350mA to 0A



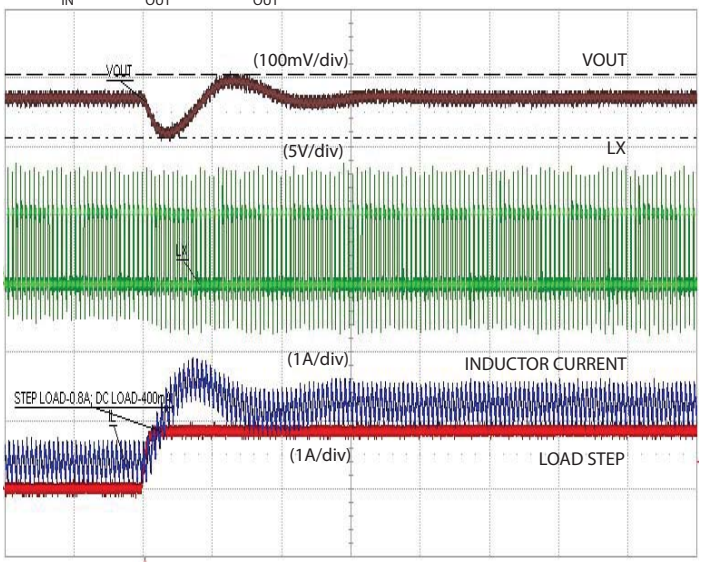
Time (20µs/div)

Typical Waveforms (continued)

Circuit Conditions: C_{IN}= 10µF/6.3V, C_{OUT}= 2 x 22µF/6.3V, C_{SS}= 2.2nF, L= 1.5µH.

Load Transient: MODE = High

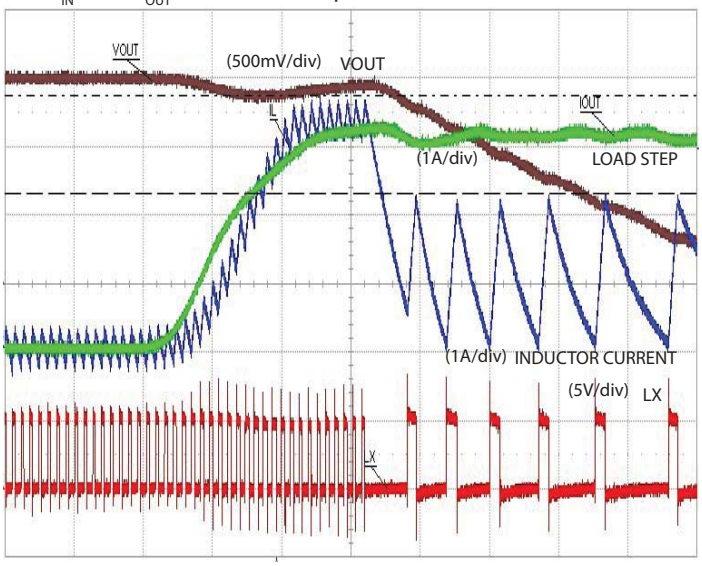
V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 400mA to 1.2A



Time (10µs/div)

Over-Current Protection: Fold Back

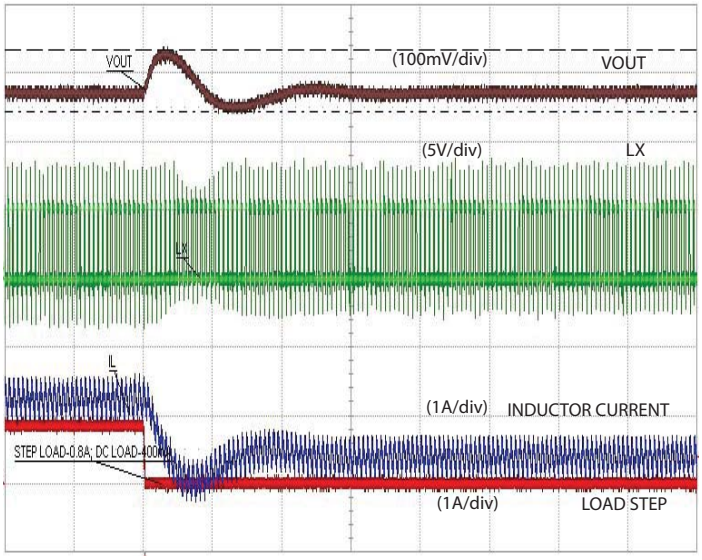
V_{IN} = 5V, V_{OUT} = 1.5V, Load Step = 0A to 3.2A



Time (5µs/div)

Load Transient: MODE = High

V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 1.2A to 400mA



Time (10µs/div)

Applications Information (continued)

Detailed Description

The SC3102 is a synchronous step-down Pulse Width Modulated (PWM), DC-DC converter utilizing a 1.5MHz fixed-frequency voltage mode architecture. The device is designed to operate in fixed-frequency PWM mode and has the option to enter forced power save mode (PSAVE) at light loads to improve efficiency. The switching frequency is chosen to minimize the size of the external inductor and capacitors while maintaining high efficiency.

Operation

During normal operation, the PMOS MOSFET is activated on each rising edge of the internal oscillator. The period is set by the onboard oscillator when in PWM mode. The device has an internal synchronous NMOS rectifier and does not require a Schottky diode on the LX pin. The device operates as a buck converter in PWM mode with a fixed frequency of 1.5MHz at medium to high loads. The MODE input is used to select between forced PWM and forced PSAVE modes. To improve the efficiency at light loads, the MODE pin can be set low to force PSAVE operation. When the MODE pin is held high, the device operates in forced continuous PWM mode regardless of the output load condition.

Forced Power Save Mode Operation

Connect the MODE pin to ground to force PSAVE mode. The maximum load current supported in forced PSAVE mode is 350mA.

Operation in PSAVE:

When the MODE pin toggles low, SC3102 operates in PSAVE mode after waiting for 64 switching cycles. Figure 1 shows the operating conditions in this mode. When the output current is less than 350mA, the switching frequency depends upon the load, and the output voltage does not fall below its regulation threshold. When the output current is higher than 350mA, the switching frequency depends upon the zero current crossing timing and the output voltage droops below its regulation threshold. The output voltage recovers when the load current is less than 350mA.

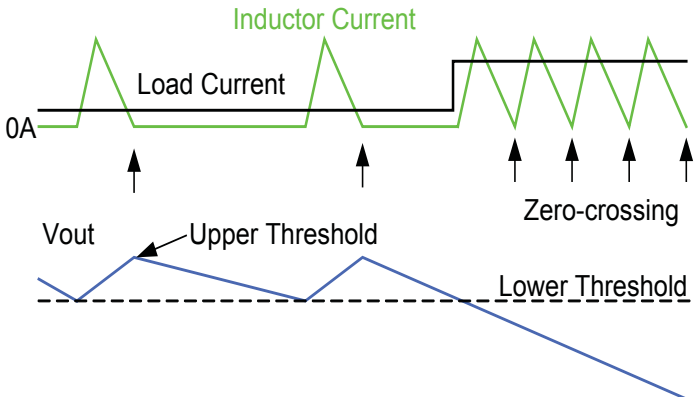


Figure 1 — Operation Conditions in PSAVE

Exiting from PSAVE:

Figure 2 shows the case of no change in the output current and the MODE pin toggling from low to high. SC3102 enters PWM mode at the end of the PSAVE cycle, where the output voltage crosses the lower PSAVE threshold.

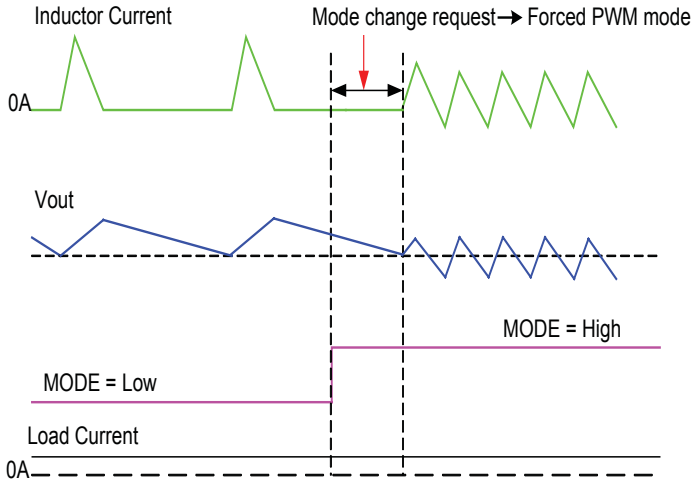


Figure 2 — Exiting PSAVE at Light Load

Figure 3 shows the behavior when there is a step increase in output current right after the MODE pin toggles high. The output voltage decreases initially due to the output capacitor supplying the load current. SC3102 changes the operation to PWM mode at t_1 and recovers the output voltage.

Applications Information (continued)

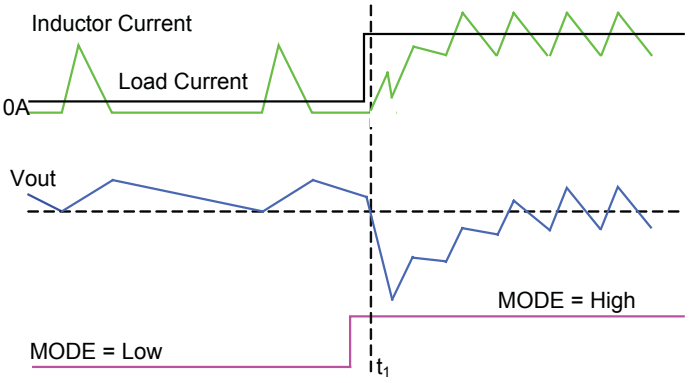


Figure 3 — Exiting PSAVE with Heavy Load

Protection Features

The SC3102 provides the following protection features:

- Current Limit
- Over-Voltage Protection
- Soft-Start Operation
- Thermal Shutdown
- UVLO

Current Limit & OCP

The internal PMOS power device in the switching stage is protected by a current limit feature. If the inductor current is above the PMOS current limit for 8 consecutive cycles, the part enters foldback current limit mode and the output current is limited to the current limit holding current (I_{CL_HOLD}) which is approximately 900mA. Under this condition, the output voltage will be the product of I_{CL_HOLD} and the load resistance. When the load presented falls below the current limit holding level, the output will charge to the upper PSAVE voltage threshold and return to normal operation. The SC3102 is capable of sustaining an indefinite short circuit without damage. During soft-start, if current limit has occurred before the SS voltage has reached 400mV, the part enters foldback current limit mode. Foldback current limit mode will be disabled during soft-start after the SS voltage is higher than 400mV.

Over-Voltage Protection

In the event of a 15% over-voltage on the output, the PWM drive is disabled with the LX pin floating. Switching does not resume until the output voltage falls below the nominal Vout regulation voltage.

Soft-Start

The soft-start mode is activated after AVIN reaches it's UVLO voltage threshold and EN is set high to enable the part. A thermal shutdown event will also activate the soft-start sequence. The soft-start mode controls the slew-rate of the output voltage during startup thus limiting in-rush current on the input supply. During start up, the reference voltage for the error amplifier is clamped by the voltage on the SS pin. The output voltage slew rate during soft-start is determined by the value of the external capacitor connected to the SS pin and the internal 5µA charging current. The SC3102 requires a minimum soft-start time from enable to final regulation in the order of 200µs, including the 50µs enable delay. As a result the soft-start capacitor, Css, should be higher than 1.5nF. During start up, the chip operates in forced PWM mode. The value of Css for the desired soft-start time, tss, can be determined by Equation 1.

$$t_{SS} = C_{SS} \times \frac{0.5V}{5\mu A} \quad (1)$$

The SC3102 is capable of starting up into a pre-biased output. When the output is pre-charged by another supply rail, the SC3102 will not discharge the output during the soft-start period.

Thermal Shutdown

The device has a thermal shutdown feature to protect the SC3102 if the junction temperature exceeds 160°C. During thermal shutdown, the on-chip power devices are disabled, floating the LX output. When the temperature drops by 10°C, it will initial a soft-start cycle to resume normal operation.

Under-Voltage Lockout

Under-Voltage Lockout (UVLO) is enabled when the input voltage drops below the UVLO threshold. This prevents the device from entering an ambiguous state in which regulation cannot be maintained. Hysteresis of approximately 300mV is included to prevent chattering near the threshold. When the AVIN voltage rises back to the turn-on threshold and EN is high, a soft-start sequence is initiated.

Power Good

The power good (PGOOD) is an open-drain output. When

Applications Information (continued)

the output voltage drops below 10% of nominal, the PGOOD pin is pulled low after a 20µs delay. During start-up, PGOOD will be asserted 2ms (typical) after the output voltage reaches 90% of the final regulation voltage. The faults of over voltage, fold-back current limit mode and thermal shutdown will force PGOOD low after a 20µs delay. When recovering from a fault, PGOOD will be asserted 2ms (typical) after Vout reaches 90% of the final regulation voltage.

Enable

The EN input is used to enable or disable the device when the device is not in UVLO. When EN is low (grounded), the device enters shutdown mode and consumes less than 1µA of current. In shutdown mode, the device tri-states the LX pin and pulls down the SS pin. The EN pin has a 500kΩ internal pull-down resistor. This resistor is switched in circuit whenever the EN pin is below its threshold, or when the device is in under voltage lockout and AVIN exceeds 0.8V. When the device is enabled, it takes about 50µs for the internal circuitry to wake up and begin the soft-start sequence.

100% Duty-Cycle Operation

The SC3102 is capable of operating at 100% duty-cycle. When the difference between the input voltage and output voltage is less than the minimum dropout voltage, the PMOS switch turns completely on, operating in 100% duty-cycle. The minimum dropout voltage is the output current multiplied by the on-resistance of the internal PMOS switch and the DC-resistance of the inductor when the PMOS switch is on continuously.

Output L-C filter Selection

The SC3102 has fixed internal loop-gain compensation. It is optimized for X5R or X7R ceramic output capacitors and an output L-C filter corner frequency of less than 34kHz. The output L-C corner frequency can be determined by Equation 2.

$$f_C = \frac{1}{2\pi\sqrt{L \cdot C_{OUT}}} \quad \text{(2)}$$

In general, the inductor is chosen to set the inductor ripple current to approximately 30% of the maximum output current. It is recommended to use a typical inductor value of 1µH to 2.2µH with output ceramic capacitors of 44µF or higher. Lower inductance should be considered in applications where faster transient response is required. More output capacitance will reduce the output deviation for a particular load transient. When using low inductance, the maximum peak inductor current at any condition (normal operation and start up) can not exceed 2.5A which is the guaranteed minimum current limit. The saturation current rating of the inductor needs to be at least larger than the peak inductor current which is the maximum output current plus half of the inductor ripple current.

Applications Information (continued)

PCB Layout Considerations

The layout diagram in Figure 4 shows a recommended top-layer PCB for the SC3102 and supporting components. Figure 5 shows the bottom layer for this PCB. Fundamental layout rules must be followed since the layout is critical for achieving the performance specified in the Electrical Characteristics table. Poor layout can degrade the performance of a DC-DC converter and can contribute to EMI problems, ground bounce, and resistive voltage losses. Poor regulation and instability can result.

The following guidelines are recommended when developing a PCB layout:

1. The input capacitor, C_{IN} should be placed as close to the PVIN and PGND pins as possible. This capacitor provides a low impedance loop for the pulsed currents present at the buck converter's input. Use short wide traces to connect as closely to the IC as possible. This will minimize EMI and input voltage ripple by localizing the high frequency current pulses.
2. Keep the LX pin traces as short as possible to minimize pickup of high frequency switching edges to other parts of the circuit. C_{OUT} and L should be connected as close as possible between the LX and PGND pins, with a direct return to the PGND pin from C_{OUT}.
3. Route the output voltage feedback/sense path away from the inductor and LX node to minimize noise and magnetic interference.
4. Use a ground plane referenced to the SC3102 PGND pin. Use several vias to connect to the component side ground to further reduce noise and interference on sensitive circuit nodes.
5. If possible, minimize the resistance from the VOUT and PGND pins to the load. This will reduce the voltage drop on the ground plane and improve the load regulation. And it will also improve the overall efficiency by reducing the copper losses on the output and ground planes.

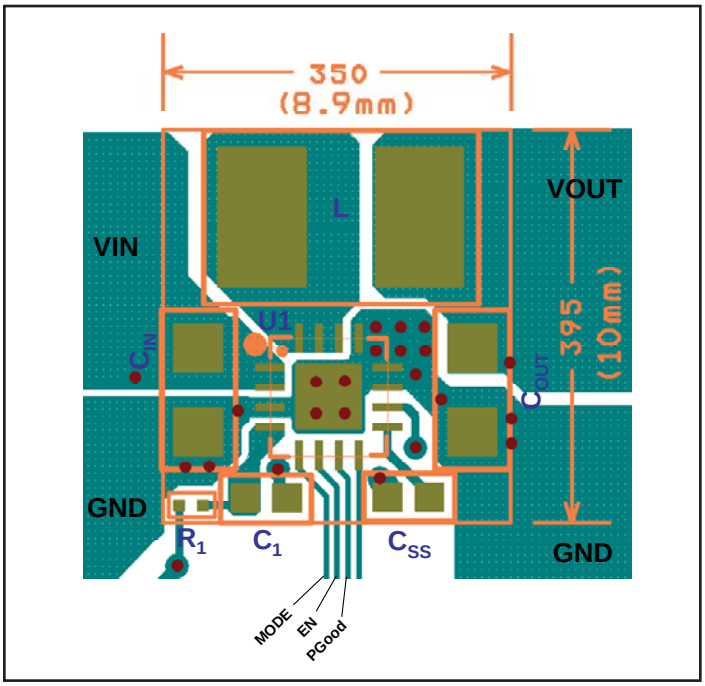


Figure 4 — Recommended PCB Layout (Top Layer)

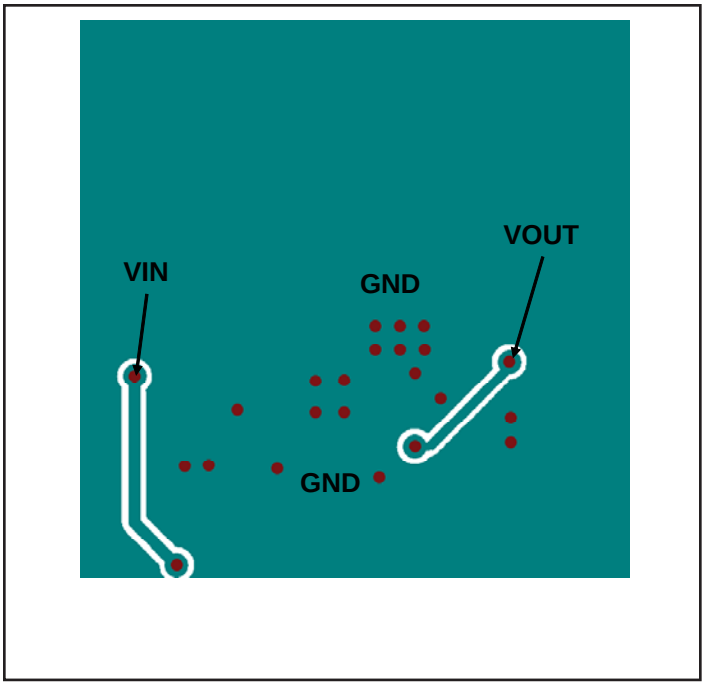
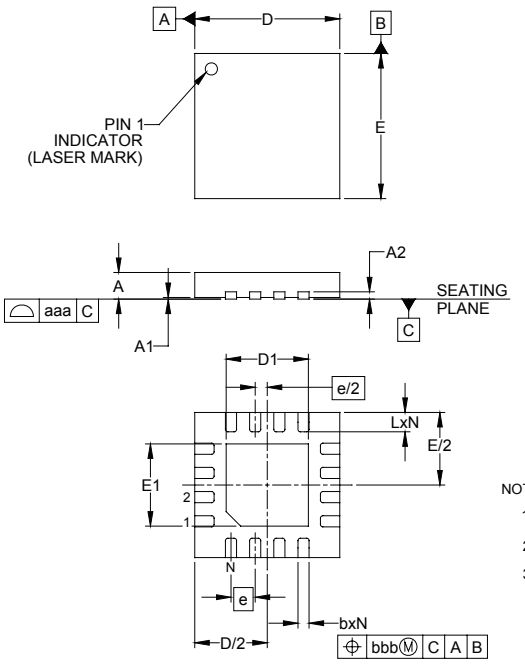


Figure 5 — Bottom Layer Detail

Outline Drawing – 3x3 MLPQ-UT16

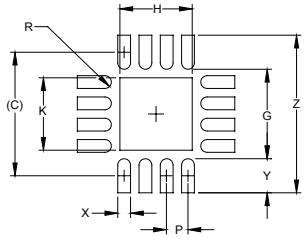


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.007	.009	.012	0.18	0.23	0.30
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.020 BSC			0.50 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		16			16	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.

Land Pattern – 3x3 MLPQ-UT16



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.020	0.50
R	.006	0.15
X	.012	0.30
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.