High Efficiency 65V/100mA Synchronous Bucks

FEATURES

- **High Efficiency Synchronous Operation**
  - **> 90% Efficiency at 30mA, 12V_{IN} to 3.3V_{OUT}**
- **Pin Selectable Forced Continuous or Burst Mode® Operation (LT8618C Only)**
- **Ultralow Quiescent Current Burst Mode Operation**
  - **< 2.5µA I_Q Regulating 48V_{IN} to 3.3V_{OUT}**
  - **Output Ripple < 10mV_{P-P}**
- **3.4V to 60V Input Operation Range (65V Max)**
- **Fast Minimum Switch-On Time: 35ns**
- **Adjustable (All) And Synchronizable (LT8618C Only) Switching Frequency: 200kHz to 2.2MHz**
- **Fixed 3.3V Output Voltage Version (LT8618-3.3)**
- Accurate 1V Enable Pin Threshold (All) with Adjustable Hysteresis (LT8618C Only)
- Internal Compensation
- Output Soft-Start and Tracking
- Small 12-Lead 2mm × 2mm LQFN (LT8618C) and 10-Lead 3mm × 2mm DFN Packages
- AEC-Q100 Qualified for Automotive Applications (LT8618/LT8618-3.3)

APPLICATIONS

- Industrial Sensors
- Industrial Internet of Things
- 4mA to 20mA Current Loops
- Flow Meters
- Automotive Housekeeping Supplies

DESCRIPTION

The LT®8618 family are compact, high speed synchronous monolithic step-down switching regulators that deliver up to 100mA to the output with high efficiency at a constant frequency, even up to 2.2MHz. They accept a wide input voltage range up to 65V (transients only, 60V for continuous operation), and consume only 2.5µA of quiescent current when operating in Burst Mode. Top and bottom power switches are included with all necessary circuitry to minimize the need for external components.

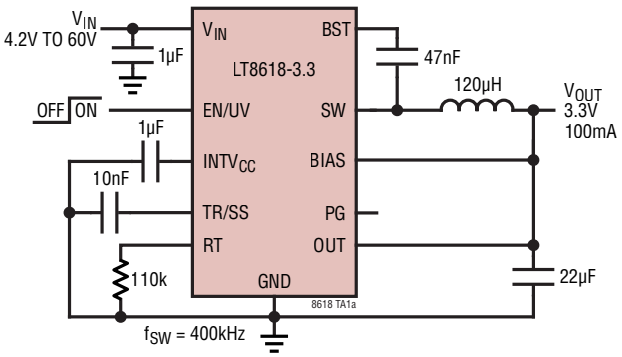
The LT8618C includes BST and $INTV_{CC}$ ceramic capacitors for a more compact solution while having SYNC/MODE and HYST pins. The SYNC/MODE pin selects the regulator's operation between forced continuous mode, for predictive interference in sampling systems, Burst Mode, for increased efficiency at light loads or spread spectrum for Low EMI. It also allows synchronization to an external clock to further increase signal to noise ratio in high-resolution acquisition systems.

A PG flag signals when V_{OUT} is within ±7.5% of the programmed output voltage and when in fault conditions. Thermal shutdown provides additional protection.

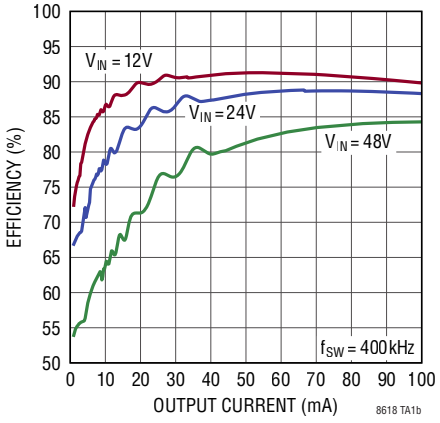
	PACKAGE	SYNC/ HYST	150°C GRADE	INTERNAL CAPS	FB RESISTORS
LT8618	DFN	No	Yes	No	External
LT8618-3.3	DFN	No	Yes	No	Internal
LT8618C	LQFN	Yes	No	Yes	External

TYPICAL APPLICATION

3.3V, Step-Down Converter



Efficiency at V_{OUT} = 3.3V



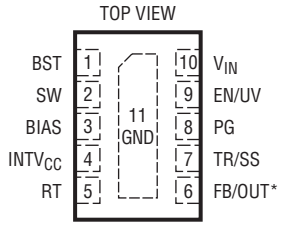
Rev. B

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, EN/UV Voltage (Note 4) ..... –0.3V to 65V
PG Voltage ..... –0.3V to 42V
BIAS Voltage ..... –0.3V to 25V
HYST Voltage (LT8618C Only) ..... –0.3V to 12V
FB (LT8618/LT8618C), TR/SS Voltages ..... –0.3V to 4V
OUT (LT8618-3.3) ..... –0.3V to 6V
SYNC/MODE Voltage (LT8618C Only) ..... –0.3V to 6V
Operating Junction Temperature Range (Note 2)
LT8618E/LT8618E-3.3/LT8618CA ..... –40°C to 125°C
LT8618I/LT8618I-3.3 ..... –40°C to 125°C
LT8618J/LT8618J-3.3 ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

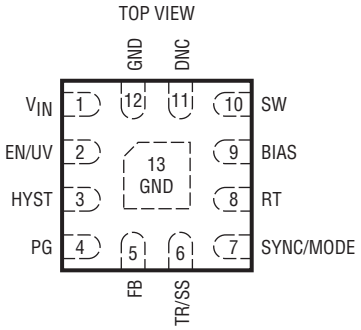
PIN CONFIGURATION

LT8618/LT8618-3.3



DDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC DFN
θ_{JA} = 76°C/W, θ_{JC} = 13.5°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB
* FB FOR LT8618, OUT FOR LT8618-3.3

LT8618C



LQFN PACKAGE
12-LEAD (2mm × 2mm × 0.74mm)
T_{JMAX} = 125°C, θ_{JA} = 51°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8618EDDB#TRMPBF	LT8618EDDB#TRPBF	LHHF	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8618IDDB#TRMPBF	LT8618IDDB#TRPBF	LHHF	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8618JDDB#TRMPBF	LT8618JDDB#TRPBF	LHHF	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C
LT8618EDDB-3.3#TRMPBF	LT8618EDDB-3.3#TRPBF	LHHW	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8618IDDB-3.3#TRMPBF	LT8618IDDB-3.3#TRPBF	LHHW	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8618JDDB-3.3#TRMPBF	LT8618JDDB-3.3#TRPBF	LHHW	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C
LT8618CAV#TRMPBF	LT8618CAV#TRPBF	LHNG	12-Lead (2mm × 2mm) LQFN (Laminate Package with QFN footprint)	–40°C to 125°C

ORDER INFORMATION

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
AUTOMOTIVE PRODUCTS**				
LT8618EDDB#WTRMPBF	LT8618EDDB#WTRPBF	LHHF	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8618IDDB#WTRMPBF	LT8618IDDB#WTRPBF	LHHF	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8618JDDB#WTRMPBF	LT8618JDDB#WTRPBF	LHHF	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C
LT8618EDDB-3.3#WTRMPBF	LT8618EDDB-3.3#WTRPBF	LHHW	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8618IDDB-3.3#WTRMPBF	LT8618IDDB-3.3#WTRPBF	LHHW	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8618JDDB-3.3#WTRMPBF	LT8618JDDB-3.3#WTRPBF	LHHW	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

For more information on lead free part marking, go to: http://www.adi.com/leadfree/
For more information on tape and reel specifications, go to: http://www.adi.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Input Voltage		●	3.4		60	V
Minimum Input Voltage	(Note 5)	●		2.9	3.4	V
V_{IN} Quiescent Current	$V_{EN/UV}$ = 0V $V_{EN/UV}$ = 2V, Not Switching	 ●		1 1.7	4 12	µA µA
V_{IN} Current in Regulation	V_{IN} = 12V, V_{OUT} = 3.3V, I_{LOAD} = 100µA V_{IN} = 12V, V_{OUT} = 3.3V, I_{LOAD} = 1mA			56 400		µA µA
LT8618/LT8618C Feedback Reference Voltage	V_{IN} = 12V, I_{LOAD} = 100µA	●	0.762	0.778	0.798	V
LT8618-3.3 Output Voltage	V_{IN} = 12V, I_{LOAD} = 100µA	●	3.2	3.3	3.4	V
FB/OUT Voltage Line Regulation	V_{IN} = 4V to 60V	●		±0.02	±0.06	%/V
LT8618/LT8618C FB Pin Input Current	V_{FB} = 0.8V	●			±20	nA
BIAS Pin Current Consumption	V_{BIAS} = 3.3V, I_{LOAD} = 30mA, 700kHz			0.8		mA
Minimum On-Time		●		35	65	ns
Minimum Off-Time		●		90	120	ns
Oscillator Frequency	R_T = 221k R_T = 18.2k	● ●	140 1.85	200 2.00	260 2.15	kHz MHz
Top Power NMOS On-Resistance				3		Ω
Top Power NMOS Current Limit		●	150	200	250	mA
Bottom Power NMOS On-Resistance				1.3		Ω
SW Leakage Current	V_{IN} = 48V	●			15	µA
EN/UV Pin Threshold	Pin Voltage Rising	●	0.98	1.05	1.11	V
EN/UV Pin Hysteresis				50		mV
EN/UV Pin Current	$V_{EN/UV}$ = 2V				±50	nA
HYST Pull-Down Resistance	V_{HYST} = 0.1V, $V_{EN/UV}$ < 0.9V, LT8618C Only			280	500	Ω
HYST Pin Leakage Current	V_{HYST} = 1V, $V_{EN/UV}$ > 1.2V, LT8618C Only				±200	nA
PG Upper Threshold Offset from $V_{FB/OUT}$	$V_{FB/OUT}$ Rising, LT8618/LT8618-3.3 $V_{FB/OUT}$ Rising, LT8618C	● ●	5.0 4.5	7.5 7.5	10.0 10.0	% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PG Lower Threshold Offset from $V_{FB/OUT}$	$V_{FB/OUT}$ Falling	●	–10.0	–7.5	–5.0	%
PG Hysteresis				0.5		%
PG Leakage	V_{PG} = 42V	●			±200	nA
PG Pull-Down Resistance	V_{PG} = 0.1V			550	1200	Ω
SYNC/MODE Threshold Voltage	LT8618C Only		0.4	0.9	1.5	V
TR/SS Source Current	$V_{TR/SS}$ = 0.1V, E- and I-Grades $V_{TR/SS}$ = 0.1V, J- and A-Grades	● ●	1 1	2 2	3.5 4	µA µA
TR/SS Pull-Down Resistance	Fault Condition, $V_{TR/SS}$ = 0.1V			300	900	Ω
V_{IN} to Disable Forced Continuous Mode	V_{IN} Rising, LT8618C Only	●	30	32	34	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8618E/LT8618E-3.3 is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8618I/LT8618I-3.3 is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT8618J/LT8618J-3.3 is guaranteed over the full –40°C to 150°C operating junction temperature range. The LT8618CA is specified over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

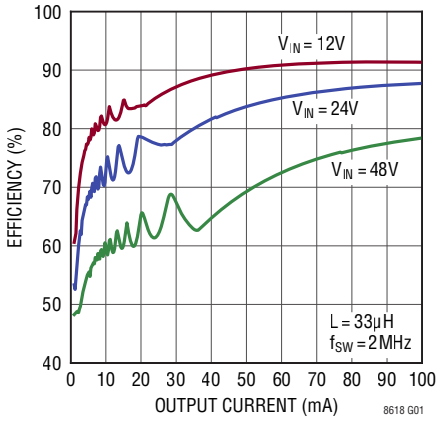
Note 3: This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

Note 4: Absolute maximum voltage at the V_{IN} and EN/UV pins is 65V for transients, and 60V for continuous operation.

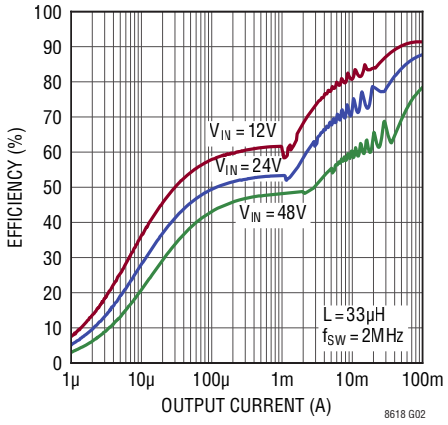
Note 5: For the LT8618-3.3, minimum input voltage will be limited by output voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

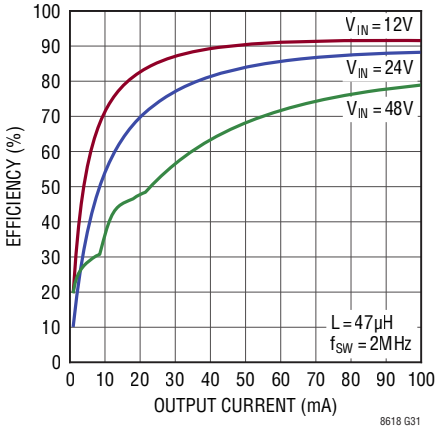
LT8618:
Burst Mode Efficiency (5V Output)



LT8618:
Burst Mode Efficiency (5V Output)

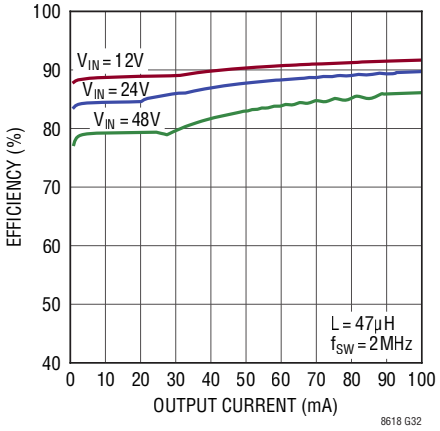


LT8618C: Forced Continuous
Mode Efficiency (5V Output)

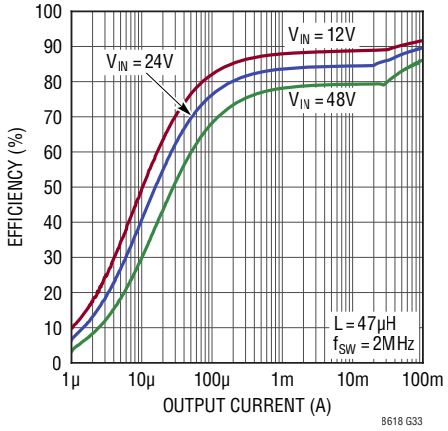


TYPICAL PERFORMANCE CHARACTERISTICS

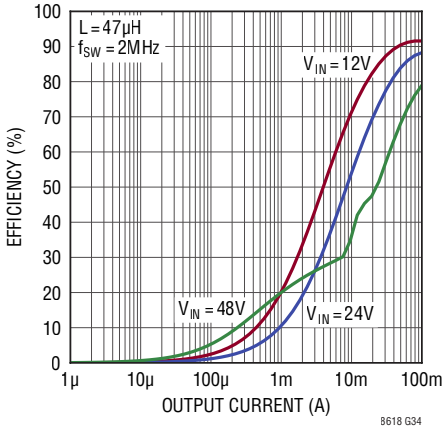
LT8618C:
Burst Mode Efficiency (5V Output)



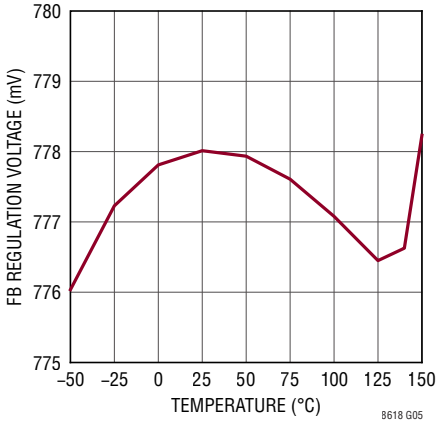
LT8618C:
Burst Mode Efficiency (5V Output)



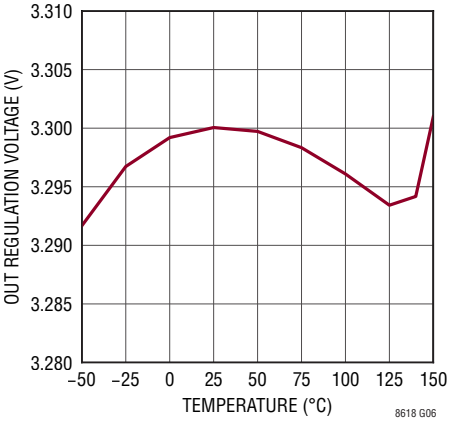
LT8618C: Forced Continuous
Mode Efficiency (5V Output)



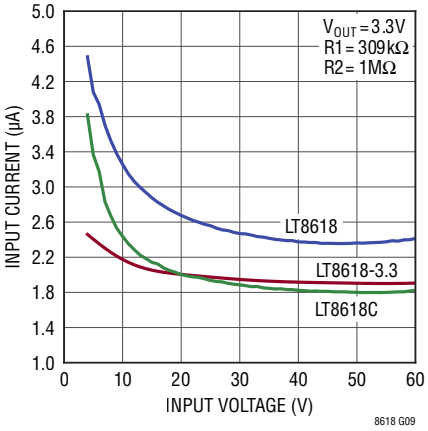
LT8618/LT8618C:
FB Voltage



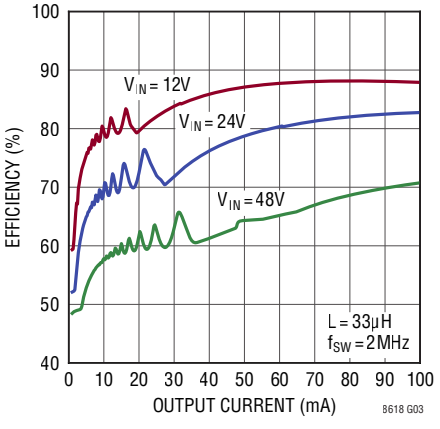
LT8618-3.3:
OUT Voltage



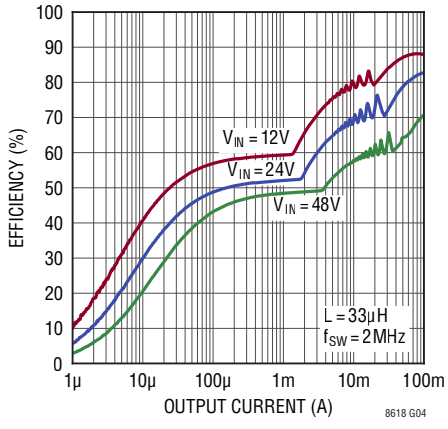
No-Load Supply Current
In Burst Mode (3.3V Output)



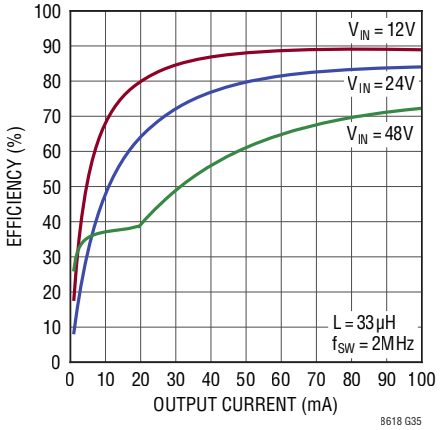
LT8618/LT8618-3.3:
Burst Mode Efficiency (3.3V Output)



LT8618/LT8618-3.3:
Burst Mode Efficiency (3.3V Output)

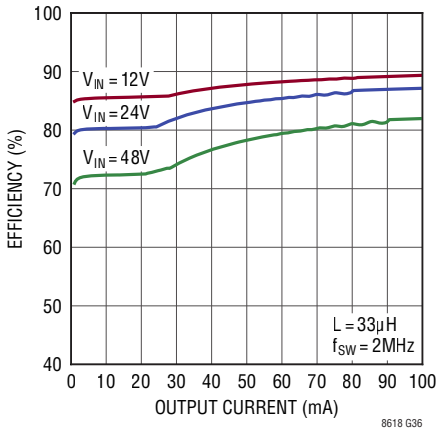


LT8618C: Forced Continuous
Mode Efficiency (3.3V Output)

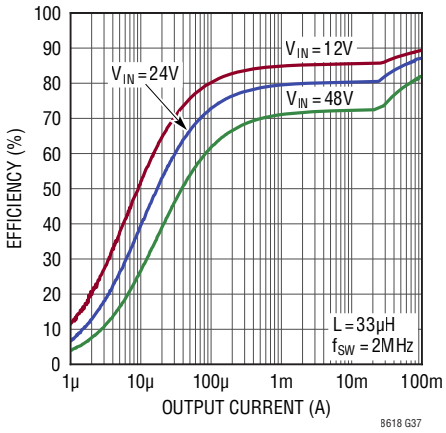


TYPICAL PERFORMANCE CHARACTERISTICS

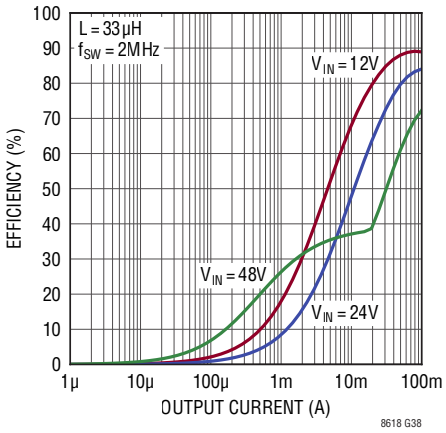
LT8618C: Burst Mode Efficiency (3.3V Output)



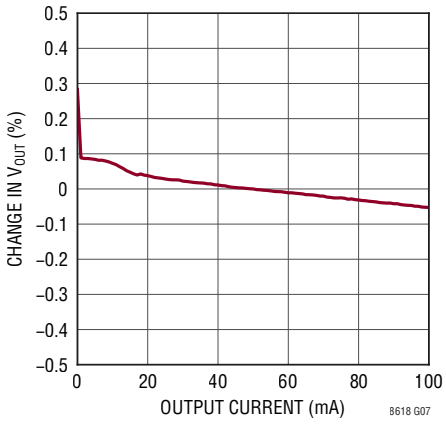
LT8618C: Burst Mode Efficiency (3.3V Output)



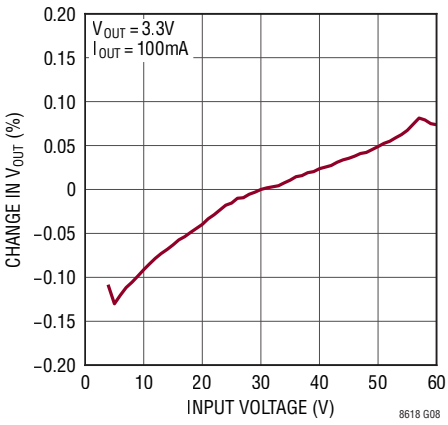
LT8618C: Forced Continuous Mode Efficiency (3.3V Output)



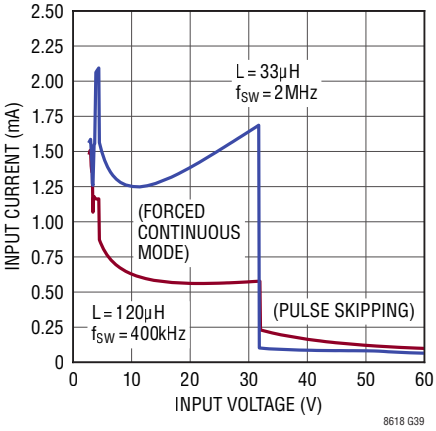
Load Regulation



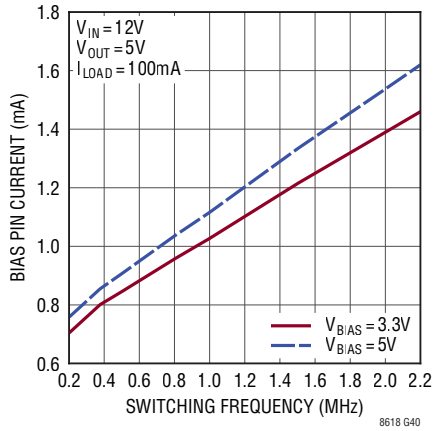
Line Regulation



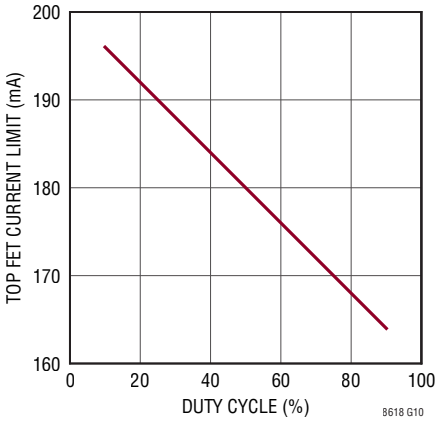
LT8618C: No-Load Supply Current In Forced Continuous Mode (3.3V Output)



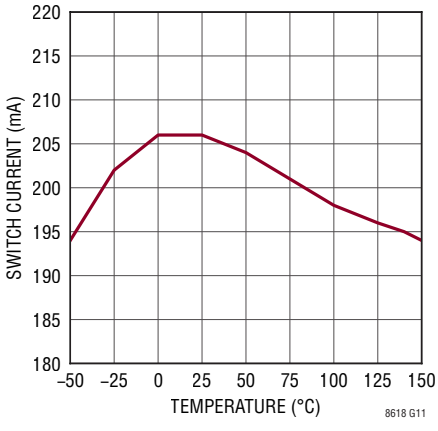
BIAS Current



Top FET Current Limit vs Duty Cycle

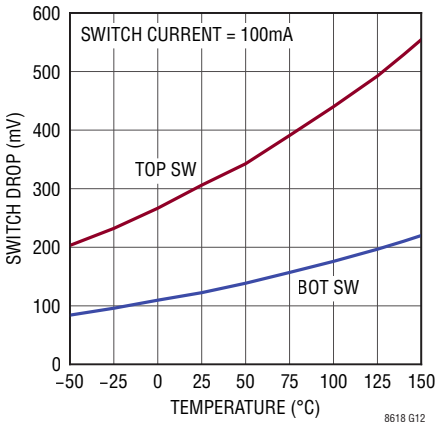


Top FET Current Limit vs Temperature

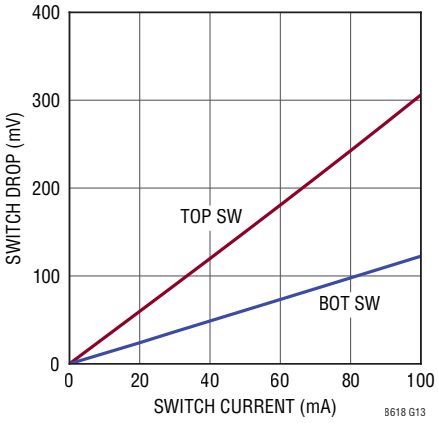


TYPICAL PERFORMANCE CHARACTERISTICS

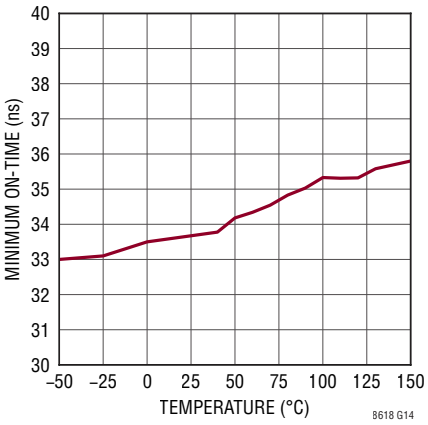
Switch Drop vs Temperature



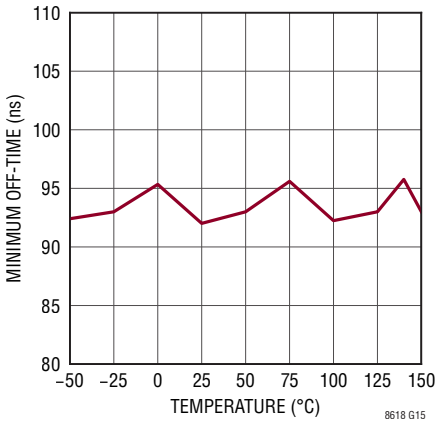
Switch Drop vs Switch Current



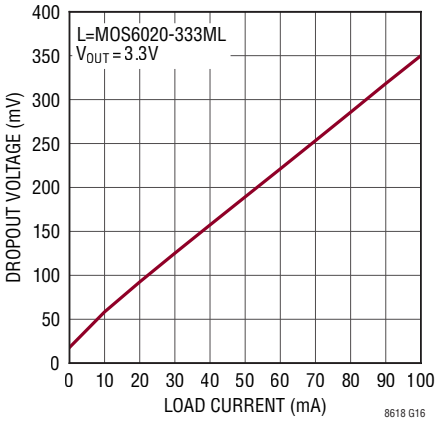
Minimum On-Time vs Temperature



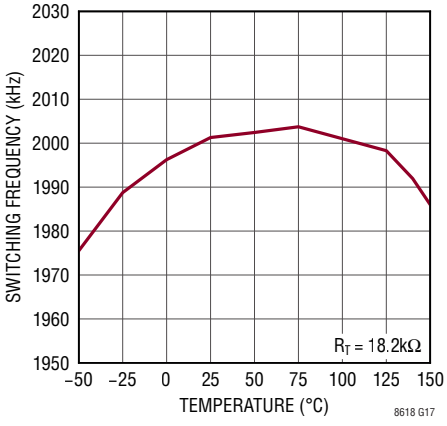
Minimum Off-Time vs Temperature



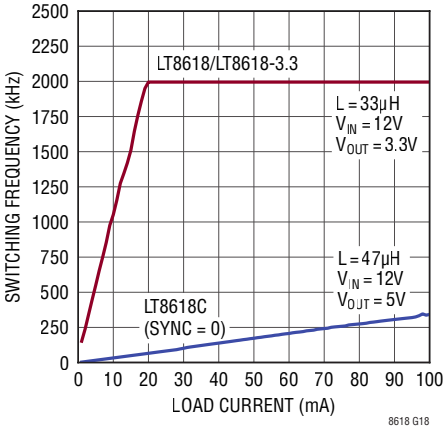
Dropout Voltage vs Load Current



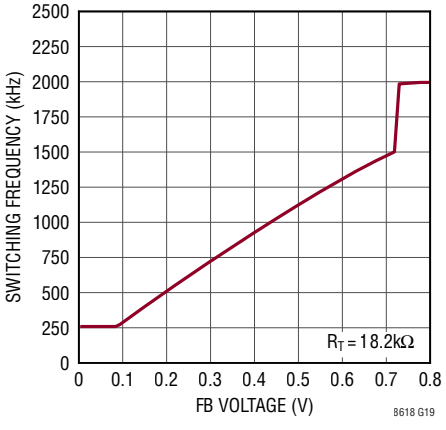
Switching Frequency vs Temperature



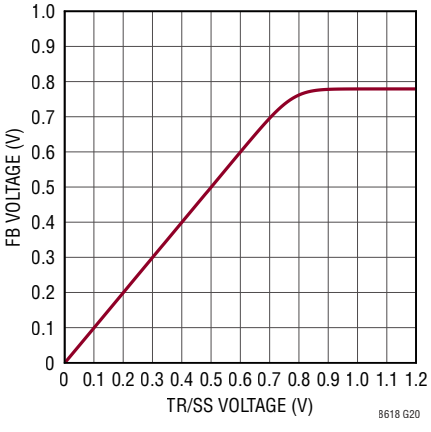
Burst Frequency vs Load Current



Frequency Foldback

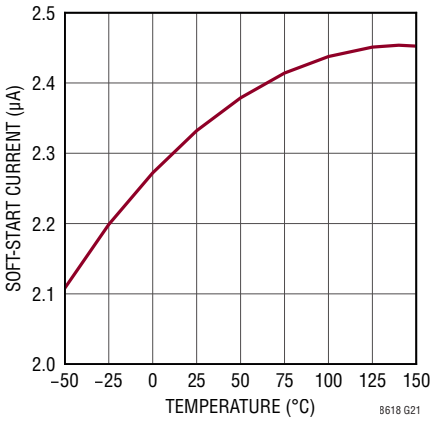


Soft-Start Tracking

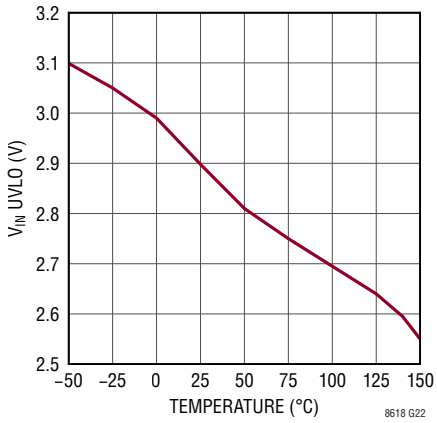


TYPICAL PERFORMANCE CHARACTERISTICS

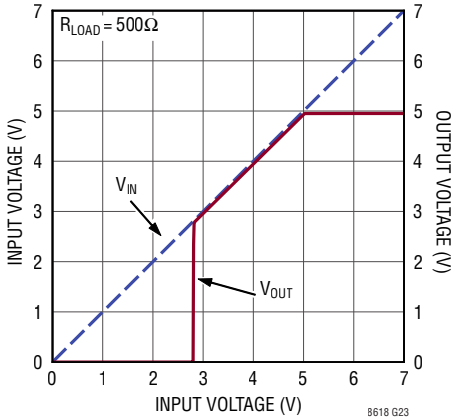
Soft-Start Current vs Temperature



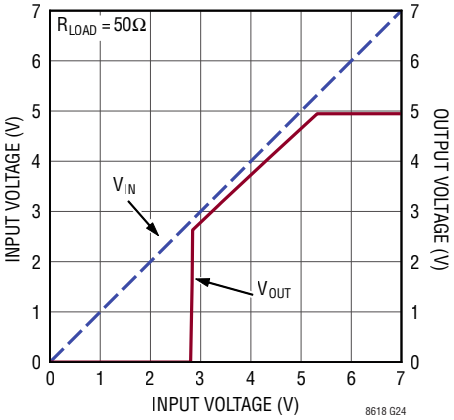
V_{IN} UVLO



Start-Up Dropout

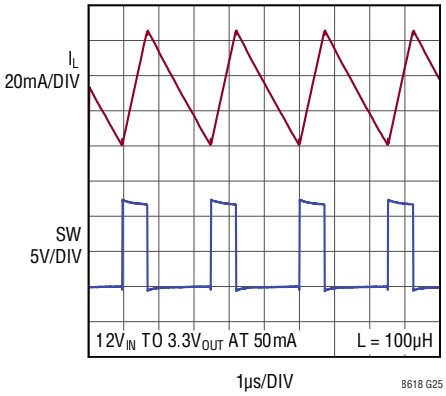


Start-Up Dropout

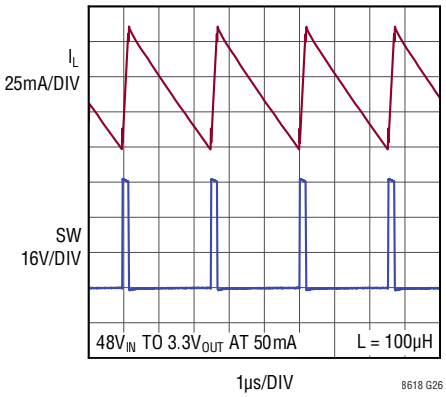


TYPICAL PERFORMANCE CHARACTERISTICS

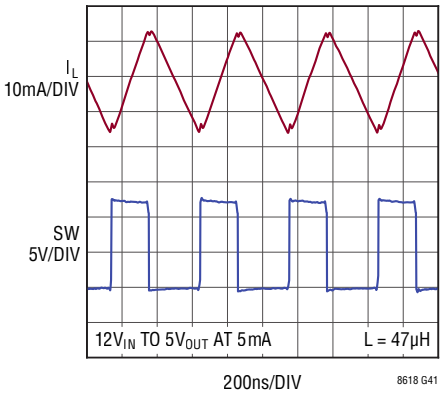
LT8618/LT8618-3.3: Switching Waveforms



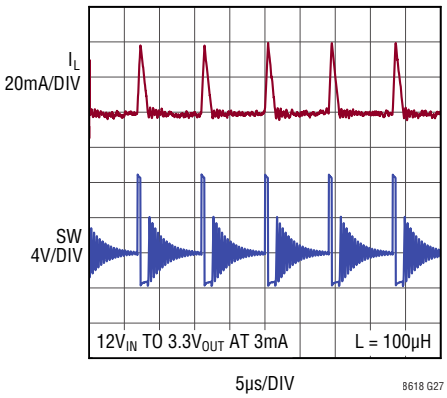
LT8618/LT8618-3.3: Switching Waveforms



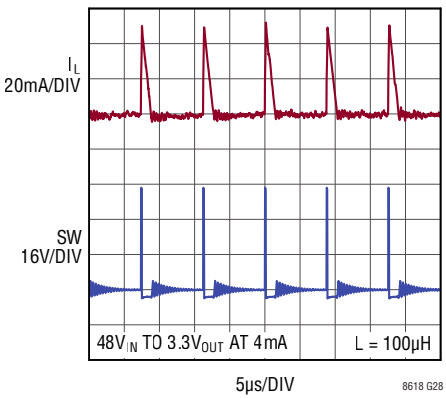
LT8618C: Forced Continuous Mode Switching Waveforms



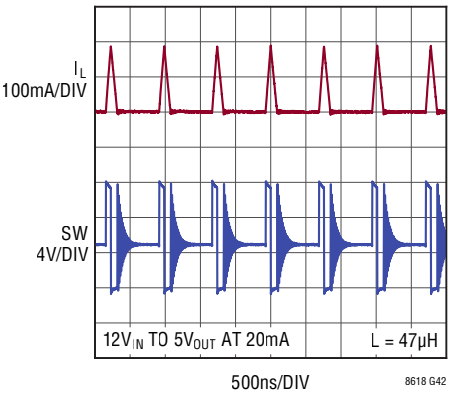
LT8618/LT8618-3.3: Switching Waveforms



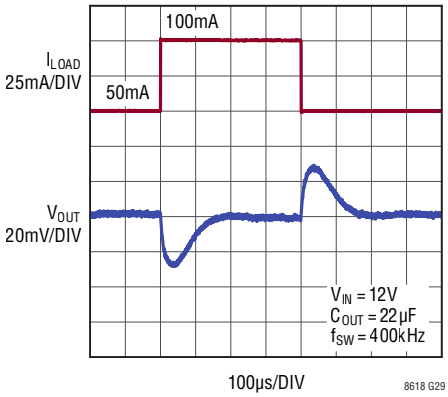
LT8618/LT8618-3.3: Switching Waveforms



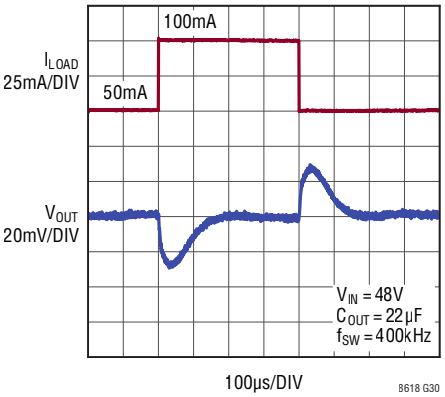
LT8618C: Burst Mode Switching Waveforms



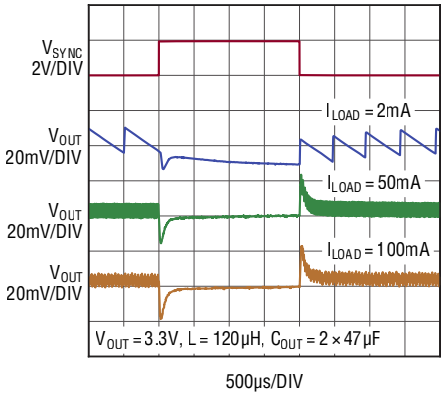
Transient Response



Transient Response



LT8618C: Transition Between Burst Mode And Forced Continuous Mode



PIN FUNCTIONS

LT8618/LT8618-3.3

BST (Pin 1): This pin is used to provide a drive voltage higher than the input voltage, to the topside power switch. Place a 47nF boost capacitor as close as possible to the IC. Do not put resistance in series with this pin.

SW (Pin 2): The SW pin is the output of the internal power switches. Connect this pin to the inductor. This node should be kept small on the PCB for good performance.

BIAS (Pin 3): The internal regulator will draw current from BIAS instead of V_{IN} when BIAS is tied to a voltage higher than 3.2V. For output voltages of 3.3V to 25V this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT}, use a 1µF local bypass capacitor on this pin. If no supply is available, tie this pin to GND.

$INTV_{CC}$ (Pin 4): Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. $INTV_{CC}$ maximum output current is 2mA. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ current will be supplied from BIAS if BIAS > 3.2V, otherwise current will be drawn from V_{IN}. Voltage on $INTV_{CC}$ will vary between 2.8V and 3.4V when V_{BIAS} is between 3.0V and 3.6V. Decouple this pin to power ground with a low ESR ceramic capacitor of at least 1µF placed close to the IC.

RT (Pin 5): Tie a resistor between RT and ground to set the switching frequency.

FB (Pin 6, LT8618 Only): The LT8618 regulates the FB pin to 0.778V. Connect the feedback resistor divider tap to this pin.

OUT (Pin 6, LT8618-3.3 Only): The LT8618-3.3 regulates the OUT pin to 3.3V. This pin connects to the internal feedback divider that programs the fixed output voltage. Tie the output to this pin.

TR/SS (Pin 7): Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A TR/SS voltage below 0.778V forces the LT8618 to regulate the FB pin to equal the TR/SS pin voltage. When TR/SS is above 0.778V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with a 300Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output.

PG (Pin 8): The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within ±7.5% of the final regulation voltage, and there are no fault conditions. PG is valid when V_{IN} is above 3.4V, regardless of EN/UV pin state.

EN/UV (Pin 9): The LT8618 is shut down when this pin is low and active when high. The hysteretic threshold voltage is 1.05V rising and 1.00V falling. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the LT8618 will shut down.

V_{IN} (Pin 10): The V_{IN} pin supplies current to the LT8618 internal circuitry and to the internal top side power switch. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN} pin, and the negative capacitor terminal as close as possible to the GND pin.

GND (Exposed Pad Pin 11): Ground. The exposed pad must be connected to the negative terminal of the input capacitor and soldered to the PCB in order to lower the thermal resistance.

PIN FUNCTIONS

LT8618C

V_{IN} (Pin 1): The V_{IN} pin supplies current to the LT8618C internal circuitry and the internal top side power switch. This pin must be locally bypassed. Place the positive terminal of the input capacitor as close as possible to the V_{IN} pin, and the negative capacitor terminal as close as possible to the GND pin.

EN/UV (Pin 2): The LT8618C is shut down when this pin is low and active when high. The hysteretic threshold voltage is 1.05V rising and 1.00V falling. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can program a V_{IN} threshold below which the LT8618C will shut down.

HYST (Pin 3): EN/UV Hysteresis Open-Drain Logic Output. This pin is pulled to ground when EN/UV (Pin 2) is below 1V. This pin can be used to adjust the EN/UV pin hysteresis. See applications information.

PG (Pin 4): The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within ±7.5% of the final regulation voltage, and there are no fault conditions. PG is valid when V_{IN} is above 3.4V, regardless of EN/UV pin state.

FB (Pin 5): The LT8618C regulates the FB pin to 0.778V. Connect the feedback resistor divider tap to this pin.

TR/SS (Pin 6): Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. A TR/SS voltage below 0.778V forces the LT8618C to regulate the FB pin to equal the TR/SS pin voltage. When TR/SS is above 0.778V, the tracking function is disabled, and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with a 300Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output.

SYNC/MODE (Pin 7): This pin programs four different operating modes: 1) Burst Mode operation. Tie this pin to ground for Burst Mode operation at low output loads—this will result in ultralow quiescent current. 2) Forced Continuous mode (FCM). This mode offers fast transient response and full frequency operation over a wide load range. Float this pin for FCM. When floating, the pin leakage current should be <1µA. 3) Spread Spectrum mode. Tie this pin high to a voltage >3V for forced continuous mode with spread-spectrum modulation. 4) Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization, the part will operate in forced continuous mode.

RT (Pin 8): Tie a resistor between RT and ground to set the switching frequency.

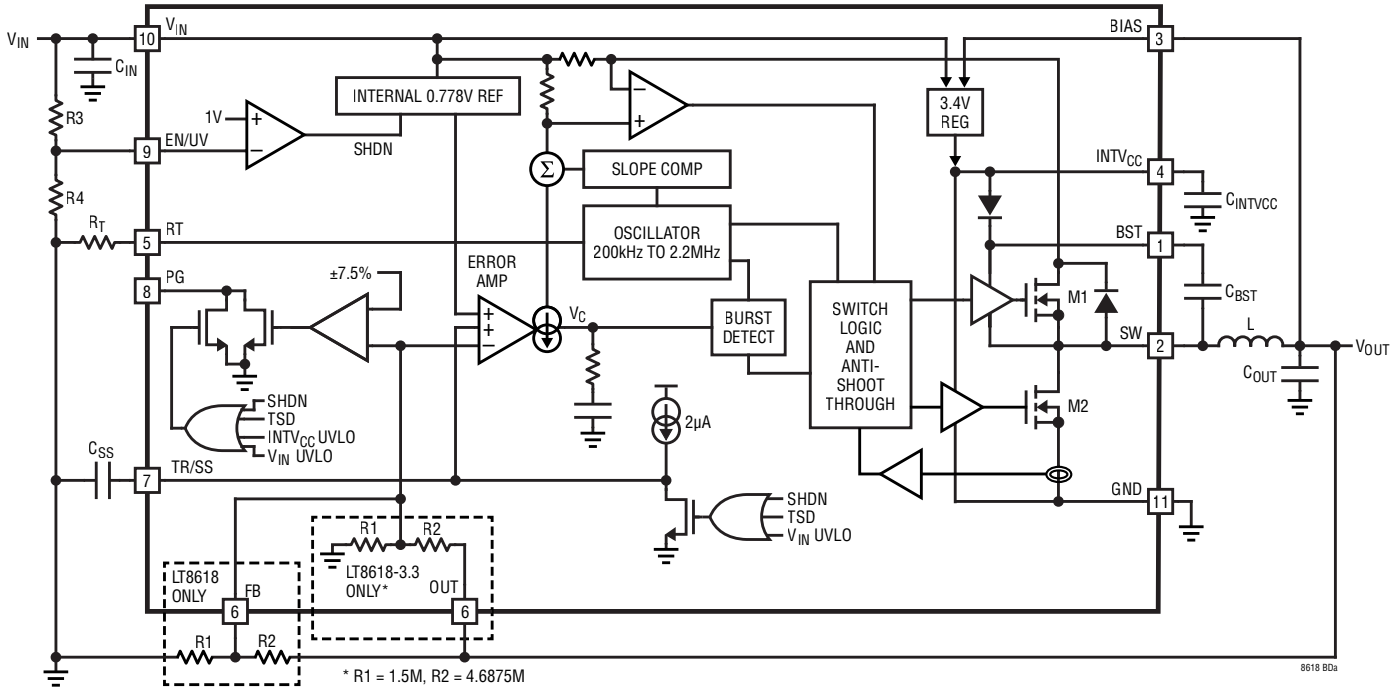
BIAS (Pin 9): The internal regulator will draw current from BIAS instead of V_{IN} when BIAS is tied to a voltage higher than 3.2V. For output voltages of 3.3V to 25V, this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT}, use a 1µF local bypass capacitor on this pin. If no supply is available, tie to GND.

SW (Pin 10): The SW pin is the output of the internal power switches. Connect this pin to the inductor. This node should be kept small on the PCB for good performance.

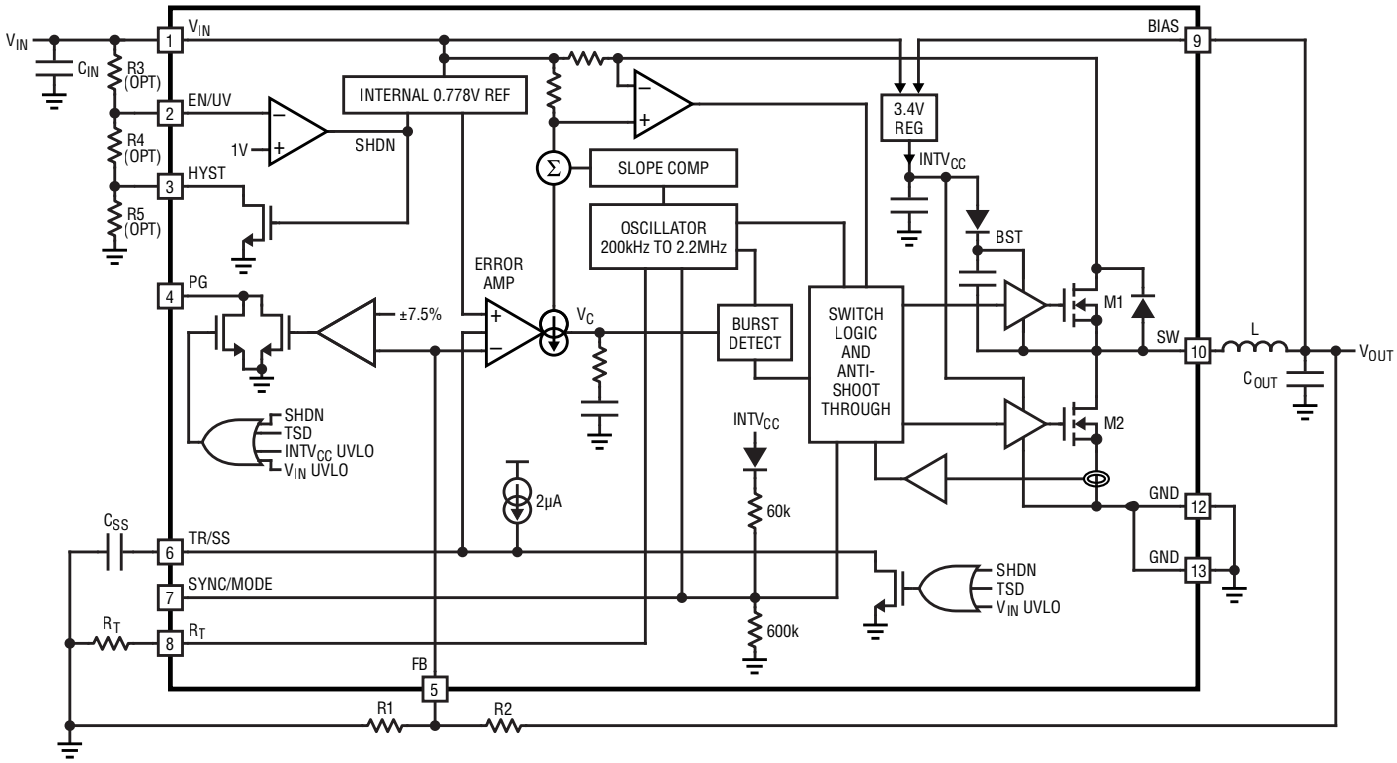
DNC (Pin 11): Do not connect pin. This pin should be left floating.

GND (Pin 12, Exposed Pad Pin 13): Ground. The exposed pad must be connected to the input capacitor's negative terminal and soldered to the PCB to lower the thermal resistance.

BLOCK DIAGRAM



LT8618/LT8618-3.3



LT8618C

OPERATION

The LT8618 family is monolithic constant frequency current mode step-down DC/DC converters. Operation is best understood by referring to the Block Diagrams. An internal oscillator turns on the integrated top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal V_C node. The error amplifier servos the V_C node by comparing the voltage on the FB pin with an internal reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or the inductor current falls to zero. If overload conditions result in excess current flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

To optimize efficiency, the LT8618 enters Burst Mode operation during light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1.7µA. In a typical application with a 48V input, 2.5µA will be consumed from the input supply when regulating with no load. The LT8618/LT8618-3.3 does not have a SYNC/MODE pin and always operates in Burst Mode. The SYNC/MODE pin (LT8618C only) is tied low to use Burst Mode operation with a fixed burst current limit of 180mA for improved efficiency at very light loads and can be floated to use forced continuous mode (FCM). If a clock is applied to the SYNC/MODE pin, the part will synchronize to an external clock frequency and operate in FCM. The SYNC/MODE pin may be tied high for spread spectrum modulation mode, and the LT8618C will operate like FCM but vary the clock frequency to reduce EMI.

The LT8618C can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is allowed. The LT8618C can sink current from the output and return it to the input in this mode, improving load step transient response.

To improve efficiency across all loads, supply current to internal circuitry is drawn from the BIAS pin when biased at 3.2V or above. Else, the internal circuitry will draw current from V_{IN}. The BIAS pin should be connected to V_{OUT} if the output is programmed to a voltage between 3.3V and 25V.

Comparators monitoring the FB (LT8618/LT8618C) or OUT (LT8618-3.3) pin voltage will pull the PG pin low if the output voltage varies more than ±7.5% (typical) from the set point or if a fault condition is present.

In the LT8618 family, the oscillator reduces its operating frequency when the voltage at the FB (LT8618/LT8618C) or OUT (LT8618-3.3) pin is low. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value, which occurs during start-up or overcurrent conditions. When a clock is applied to the SYNC/MODE pin (LT8618C only), the SYNC/MODE pin is floated or held DC high, the frequency foldback is disabled, and the switching frequency will slow down only during overcurrent conditions.

If the EN/UV pin is low, the LT8618 family is shut down and draws 1µA from the input. When the EN/UV pin is above 1.05V, the switching regulator becomes active.

The HYST pin (LT8618C only) provides an added degree of flexibility for the EN/UV pin operation. This open-drain output is pulled to ground whenever the EN/UV comparator is not tripped, signaling that the LT8618C is not in normal operation. In applications where the EN/UV pin is used to monitor the V_{IN} voltage through an external resistive divider, the HYST pin can be used to increase the effective EN/UV comparator hysteresis.

APPLICATIONS INFORMATION

Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT8618 family enters into low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. This is the default operation of LT8618/LT8618-3.3. For the LT8618C, the SYNC/MODE pin must be tied to ground. In Burst Mode operation, the LT8618 family delivers single small pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode the LT8618 family consumes 1.7µA.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT8618 family is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 2.5µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

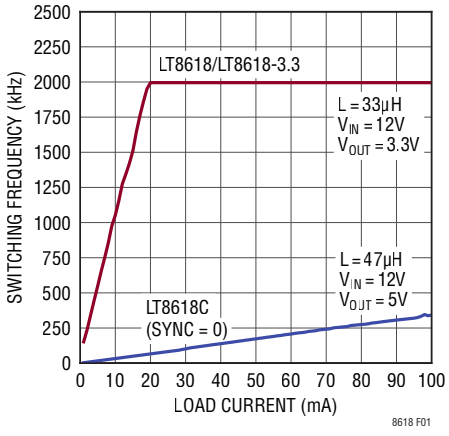


Figure 1. SW Burst Mode Frequency vs Load

While in Burst Mode operation, the current limit of the top switch is approximately 40mA in the LT8618/LT8618-3.3 and 180mA in the LT8618C, resulting in output voltage ripple shown in Figure 2 and Figure 3. As the load ramps upward from zero the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 1. The output

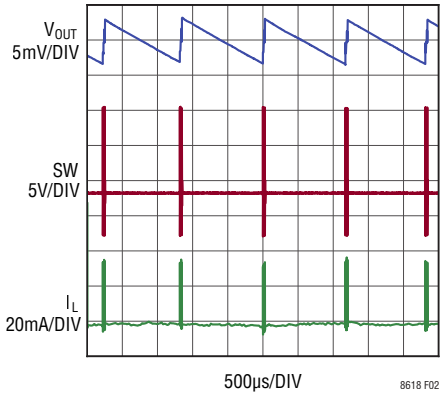


Figure 2. Burst Mode Operation (LT8618/LT8618-3.3)

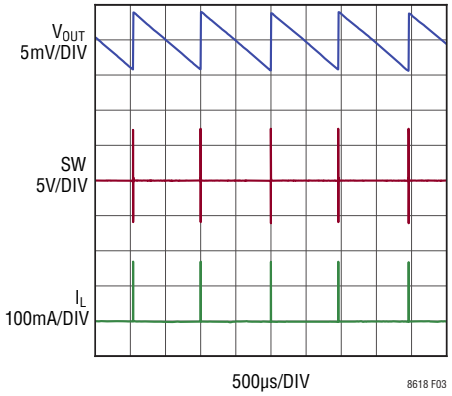


Figure 3. Burst Mode Operation (LT8618C)

load at which the LT8618 family reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice.

Since the higher Burst Mode current limit of the LT8618C leads to a higher inductor current ripple, its switching frequency is reduced accordingly and will usually never reach the frequency programmed by the resistor at the RT pin over the entire load range. Use forced continuous mode (see next section) for full frequency operation. The LT8618C applies slope compensation even in Burst Mode to ensure stable operation at higher load currents.

Forced Continuous Mode (LT8618C Only)

The LT8618C can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is allowed

APPLICATIONS INFORMATION

at light loads or under large transient conditions. The LT8618C can sink current from the output and return it to the input in this mode, improving load step transient response. At light loads, FCM operation is less efficient than Burst Mode operation or pulse-skipping mode. Still, it may be desirable in applications where it is necessary to keep switching harmonics out of the signal band. FCM must be used if the output is required to sink current. To enable FCM (LT8618C only), float the SYNC/MODE pin. Leakage current on this pin should be <1µA. See the Block Diagram for internal pull-up and pull-down resistance.

FCM is disabled if the voltage on the V_{IN} pin is above 32V or if the FB pin's voltage is above the internal reference voltage by more than 7.5%. FCM is also disabled during soft-start until the soft-start capacitor is fully charged. When FCM is disabled in these ways, negative inductor current is not allowed, and the LT8618C operates in pulse-skipping mode.

For robust operation over a wide V_{IN} and V_{OUT} range, use an inductor value larger than L_{MIN}:

$$L_{MIN} = \frac{V_{OUT}}{0.07 \bullet f_{SW}} \left(1 - \frac{V_{OUT}}{40}\right)$$

Spread Spectrum Mode (LT8618C only)

The LT8618C features spread-spectrum operation to further reduce EMI/EMC emissions. To enable spread-spectrum operation, tie the SYNC/MODE pin to a voltage >3V. In this mode, triangular frequency modulation is used to vary the switching frequency between 100% and approximately 120% of the value programmed by RT. The modulation frequency is approximately 3kHz. For example, when the LT8618C is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at a 3kHz rate. When spread-spectrum operation is selected, Burst Mode operation is disabled, and the part will run in forced continuous mode.

Synchronization (LT8618C only)

To synchronize the LT8618C oscillator to an external frequency, connect a square wave (with 20% to 80% duty cycle) to the SYNC/MODE pin. The square wave amplitude should have valleys below 0.4V and peaks above 1.5V (up to 6V).

The LT8618C will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will run in forced continuous mode to maintain regulation. The LT8618C may be synchronized over a 200kHz to 2.2MHz range. The R_T resistor should be chosen to set the LT8618C switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, RT should be selected for 500kHz. The slope compensation is set by the RT value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the inductor current waveform slopes, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by RT, then the slope compensation will be sufficient for all synchronization frequencies.

Switching between Burst Mode and FCM in LT8618C

The LT8618C achieves very high efficiency at very light loads when operating in Burst Mode due to its fixed top switch current limit of 180mA in this mode. The internal V_C node does not control peak inductor current but instead the period between current pulses. Thus it does not need to vary much to keep the output in regulation over the entire load current range. In Forced Continuous Mode, on the other hand, the V_C node controls the peak inductor current and thus varies widely with load current. For a given load current, the V_C node voltage required to keep the output in regulation may differ between Burst Mode and FCM. The error amplifier adjusts the VC node to the new required level when switching between these modes of operation. During this transition, the output may experience a load current dependent transient with worst-case amplitude happening at full load. Applications that transition between Burst Mode and FCM require a larger output capacitor to keep output voltage transients below acceptable limits at full load current.

APPLICATIONS INFORMATION

FB Resistor Network (LT8618)

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R2 = R1\left(\frac{V_{OUT}}{0.778V} - 1\right)$$

1% resistors are recommended to maintain output voltage accuracy.

The total resistance of the FB resistor divider should be selected to be as large as possible when good low load efficiency is desired: The resistor divider generates a small load on the output, which should be minimized to optimize the quiescent current at low loads.

Setting the Switching Frequency

The LT8618 family uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.2MHz by using a resistor tied from the RT pin to ground. Table 1 shows the necessary R_T value for a desired switching frequency.

Table 1. SW Frequency vs RT Value

f_{SW} (MHz)	R_T (kΩ)
0.2	221
0.3	143
0.4	110
0.5	86.6
0.6	71.5
0.7	60.4
0.8	52.3
0.9	46.4
1.0	40.2
1.2	33.2
1.4	27.4
1.6	23.7
1.8	20.5
2.0	18.2
2.2	16.2

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.13V, respectively at max load) and $t_{ON(MIN)}$ is the minimum top switch on-time (see Electrical Characteristics). This equation shows that slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation V_{IN} may go as high as the Abs Max rating regardless of the RT value, however the LT8618 family will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation.

The LT8618 family is capable of maximum duty cycle approaching 100%, and the V_{IN} to V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode the LT8618 family skips switch cycles, resulting in a lower switching frequency than programmed by R_T.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios, use the following formula to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)}$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.13V, respectively at max load), f_{SW} is the switching frequency (set by RT), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

APPLICATIONS INFORMATION

Inductor Selection and Maximum Output Current

The LT8618 family is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short circuit conditions the LT8618 family safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}} \bullet 19$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.13V) and L is the inductor value in µH. Using an inductor value more than two times this calculated size is not recommended.

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of the inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta_L$$

where ΔI_L is the inductor ripple current as calculated several paragraphs below and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 100mA output should use an inductor with an RMS rating of greater than 100mA and an I_{SAT} of greater than 160mA. To keep the efficiency high, the series resistance (DCR) should be less than 1Ω, and the core material should be intended for high frequency applications.

The LT8618 family limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is at least 150mA at low duty cycles and decreases linearly to 120mA at D = 0.8. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current:

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

The peak-to-peak ripple current in the inductor can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

where f_{SW} is the switching frequency, and L is the value of the inductor. Therefore, the maximum output current that the LT8618 family will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

For more information about maximum output current and discontinuous operation, see Analog Devices Application Note 44.

Finally, for duty cycles greater than 50%, a minimum inductance is required to avoid sub-harmonic oscillation:

$$L_{MIN} = \frac{V_{OUT} + V_{SW(BOT)}}{0.08 \bullet f_{SW}}$$

where f_{SW} is the switching frequency, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.13V) and L_{MIN} is the inductor value.

Input Capacitor

Bypass the input of the LT8618 family circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 1µF to 2.2µF ceramic capacitor is adequate to bypass the LT8618 family and will easily handle the ripple current. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

APPLICATIONS INFORMATION

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT8618 family and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 1µF capacitor is capable of this task, but only if it is placed close to the LT8618 family (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT8618 family. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8618 family circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8618 family's voltage rating. This situation is easily avoided (see Analog Devices Application Note 88).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT8618 family to produce the DC output. In this role it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT8618 family's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{50}{V_{OUT} \bullet f_{SW}}$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feedforward capacitor placed between V_{OUT} and FB. Increasing the output capacitance will also decrease the output voltage ripple. Due to its larger burst mode current limit, the LT8618C requires a larger C_{OUT} for low output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer and may cause loop instability. See the Typical Applications in this data sheet for suggested capacitor values. The LT8618-3.3 has an internal feedforward capacitor and therefore requires a minimum C_{OUT} of 22µF.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT8618 family due to their piezoelectric nature. When in Burst Mode operation, the LT8618 family's switching frequency depends on the load current, and at very light loads the LT8618 family can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT8618 family operates at a lower current limit during Burst Mode operation, the noise is typically very quiet. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT8618 family. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT8618 family circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT8618 family's rating. This situation is easily avoided (see Analog Devices Application Note 88).

EN/UV Pin and Programmable Hysteresis of LT8618C

The LT8618 family is in shutdown when the EN/UV pin is low and active when the pin is high. The rising threshold of the EN/UV comparator is 1.05V, with 50mV of hysteresis. The EN/UV pin can be tied to V_{IN} if the shutdown feature is not used, or tied to a logic level if shutdown control is required.

Adding a resistor divider from V_{IN} to EN/UV programs the LT8618 family to regulate the output only when V_{IN}

APPLICATIONS INFORMATION

is above a desired voltage (see Block Diagram). Typically, this threshold, $V_{IN(EN/UV)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN/UV)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$R3 = \left(\frac{V_{IN(EN/UV)}}{1.05V} - 1 \right) \bullet R4$$

where the LT8618 family will remain off until V_{IN} is above $V_{IN(EN/UV)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN/UV)}$.

Additional hysteresis may be added with the use of the HYST pin (LT8618C only). The HYST pin is an open-drain output that is pulled to ground whenever the EN/UV pin voltage is below the threshold that keeps the part in shutdown. As shown in the Block Diagram, a simple resistive divider can be used to meet specific operating V_{IN} voltage requirements.

Specific values for these UVLO thresholds can be computed from the following equations:

$$V_{IN(EN/UV)\uparrow} = 1.05V \left(1 + \frac{R3}{R4} \right)$$

$$V_{IN(EN/UV)\downarrow} = 1V \left(1 + \frac{R3}{R4+R5} \right)$$

where $V_{IN(EN/UV)\uparrow}$ is the rising V_{IN} UVLO threshold and $V_{IN(EN/UV)\downarrow}$ is the falling V_{IN} UVLO threshold. The hysteresis $V_{IN(EN/UV)H} = V_{IN(EN/UV)\uparrow} - V_{IN(EN/UV)\downarrow}$ is set by R5:

$$R5 = \frac{R3}{1.05\frac{R3}{R4} + 0.05 - \frac{V_{IN(EN/UV)H}}{1V}} - R4$$

The minimum value of these UVLO thresholds is limited to the internal minimum V_{IN} Voltage shown in the Electrical Characteristics table. Be aware that the HYST pin cannot be allowed to exceed its absolute maximum rating of 12V. To keep the voltage on the HYST pin from exceeding 12V, the following relation should be satisfied:

$$V_{IN(MAX)} \bullet \left(\frac{R5}{R3+R4+R5} \right) \leq 12V$$

When in Burst Mode operation for light-load currents, the current through the $V_{IN(EN/UV)}$ resistor network can easily be greater than the supply current consumed by the LT8618 family. Therefore, the $V_{IN(EN/UV)}$ resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN} that powers the drivers and the internal bias circuitry. $INTV_{CC}$ can supply enough current for the LT8618 family's circuitry. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Therefore, the $INTV_{CC}$ pin of the LT8618/LT8618-3.3 must be bypassed to ground with a ceramic capacitor of at least 1µF. The LT8618C does not have an $INTV_{CC}$ pin but provides an on-package capacitor as an internal bypass. To improve efficiency, the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.2V or higher. Typically, the BIAS pin can be tied to the output of the LT8618 or can be tied to an external supply of 3.3V or above. If BIAS is connected to a supply other than V_{OUT}, be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO will consume current from V_{IN}. Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the $INTV_{CC}$ pin.

Output Voltage Tracking and Soft-Start

The LT8618 family allows the user to program its output voltage ramp rate by means of the TR/SS pin. An internal

APPLICATIONS INFORMATION

2µA pulls up the TR/SS pin to $INTV_{CC}$. Putting an external capacitor on TR/SS enables soft-starting the output to prevent current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage. For output tracking applications, TR/SS can be externally driven by another voltage source. From 0V to 0.778V, the TR/SS voltage will override the internal 0.778V reference input to the error amplifier, thus regulating the FB pin voltage to that of TR/SS pin. When TR/SS is above 0.778V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good

When the LT8618 family's output voltage is within the ±7.5% window of the regulation point, which is a V_{FB} voltage in the range of 0.720V to 0.836V (typical), the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal drain pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 0.5% of hysteresis.

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ has fallen too low, or thermal shutdown.

Shorted and Reversed Input Protection

The LT8618 family will tolerate a shorted output. Several features are used for protection during output short-circuit and brownout conditions. The first is the switching frequency will be folded back while the output is lower than the set point to maintain inductor current control. Second, the bottom switch current is monitored such that if inductor current is beyond safe levels switching of the top switch will be delayed until such time as the inductor current falls to safe levels. This allows for tailoring the LT8618 family to individual applications and limiting thermal dissipation during short circuit conditions.

There is another situation to consider in systems where the output will be held high when the input to the LT8618 family is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LT8618 family's output. If the V_{IN} pin is allowed to float and the EN/UV pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8618 family's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate several µA in this state. If the EN/UV pin is grounded the SW pin current will drop to near 0.7µA. However, if the V_{IN} pin is grounded while the

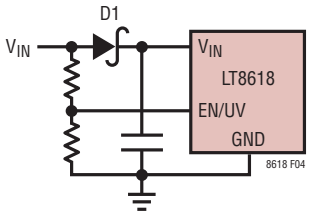


Figure 4. Reverse V_{IN} Protection

output is held high, regardless of EN/UV, parasitic body diodes inside the LT8618 family can pull current from the output through the SW pin and the V_{IN} pin. Figure 4 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8618 family to run only when the input voltage is present and that protects against a shorted or reversed input.

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 5 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT8618 family's V_{IN} pins, GND pins, and the input capacitor (C_{IN}). The loop formed by the input capacitor should be as small as possible by placing the capacitor adjacent to the V_{IN} and GND pins. When using a physically large input capacitor the resulting loop may become too large in which case using a small case/value capacitor placed close to the V_{IN} and GND pins plus a larger capacitor further away is preferred. These components, along with the inductor and output capacitor,

APPLICATIONS INFORMATION

should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible. In addition, keep the FB and RT nodes small so that the ground traces will shield them from the SW and BOOST nodes. Finally, route the LT8618C's SYNC node below the ground plane in order to minimize capacitive coupling to the FB and TR/SS nodes. The exposed pad on the bottom of the package must be soldered to ground so that the pad is connected to ground electrically and also acts as a heat sink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias near the LT8618 family to additional ground planes within the circuit board and on the bottom side. Figure 5 and Figure 6 show basic guidelines for layout examples that can pass the CISPR25 radiated emission test with class 5 limits.

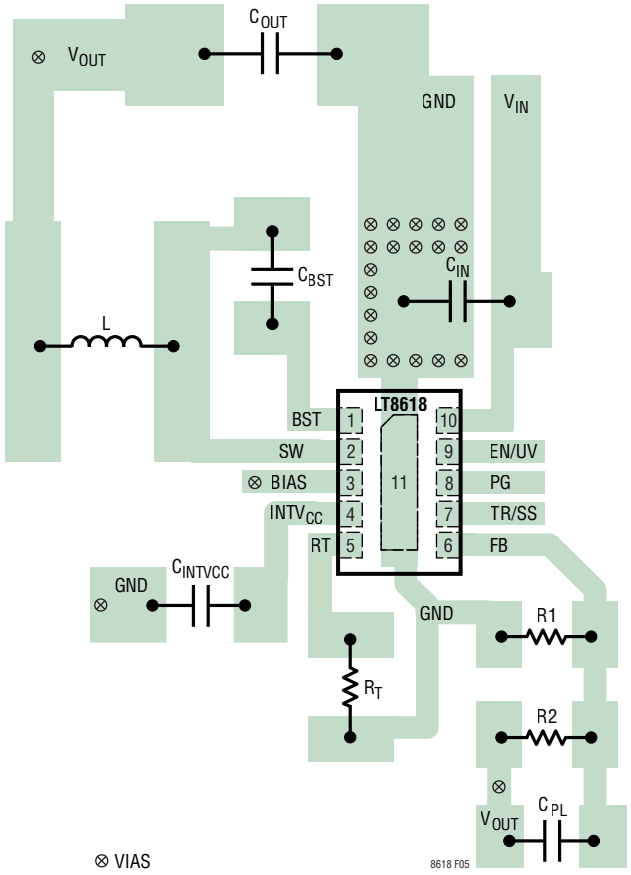


Figure 5. LT8618/LT8618-3.3, Recommended PCB Layout

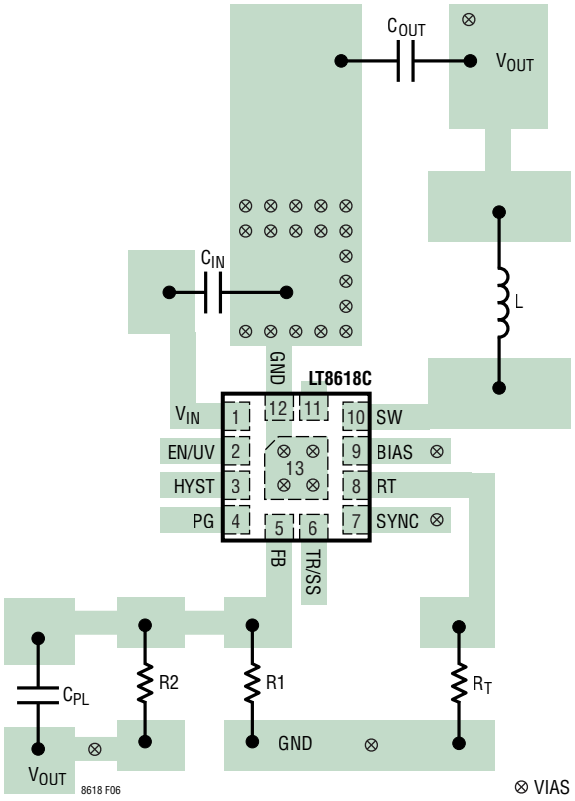
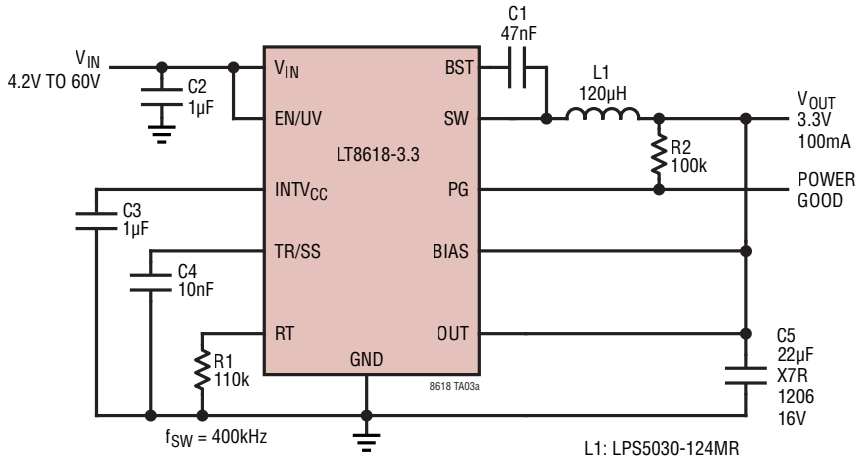


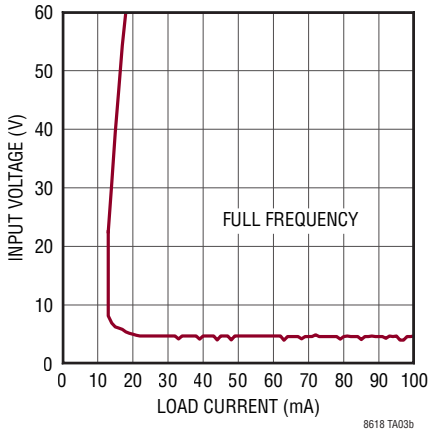
Figure 6. LT8618C, Recommended PCB Layout

TYPICAL APPLICATIONS

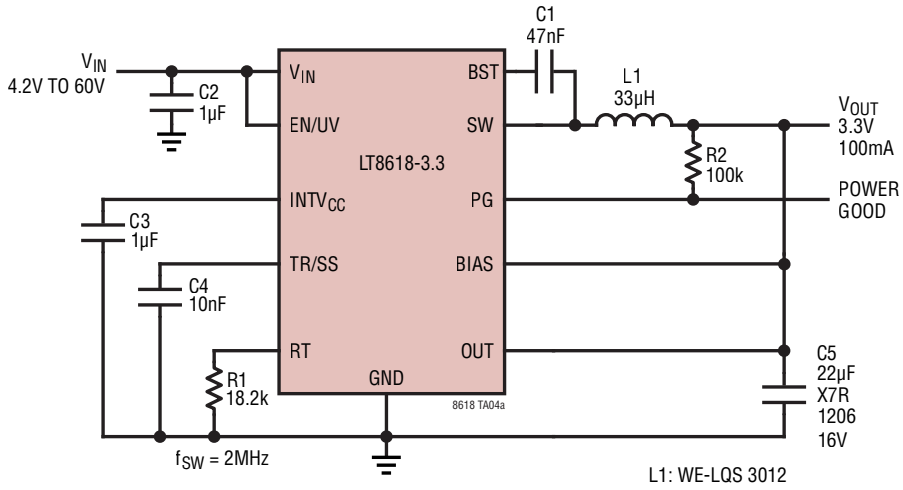
3.3V Step-Down Converter



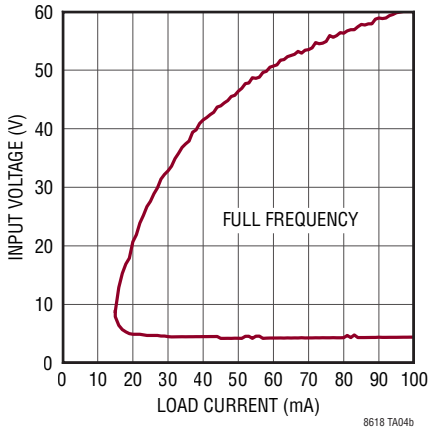
Typical Performance Minimum Load to Full Frequency



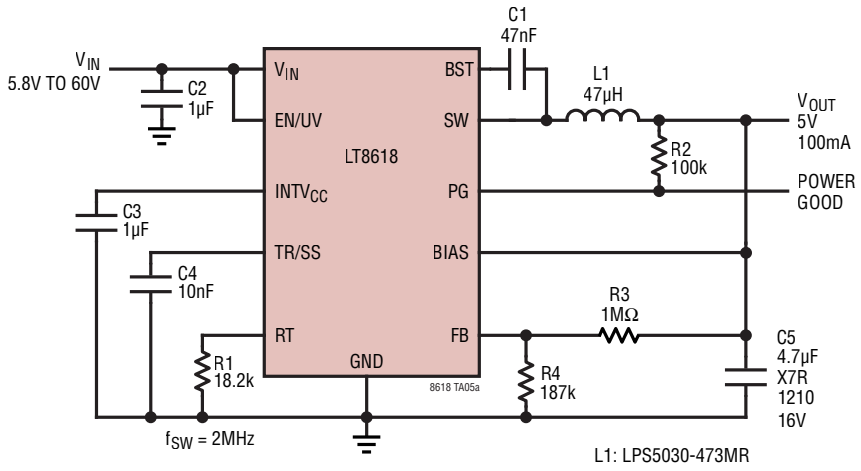
3.3V, 2MHz Step-Down Converter



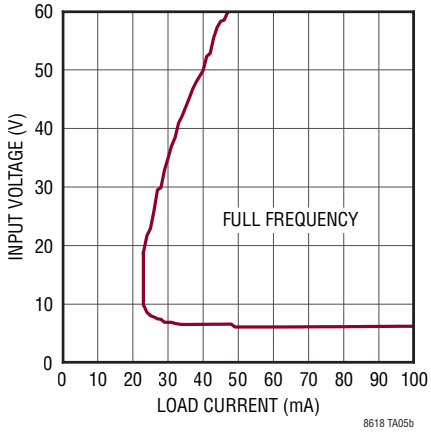
Typical Performance Minimum Load to Full Frequency



5V, 2MHz Step-Down Converter



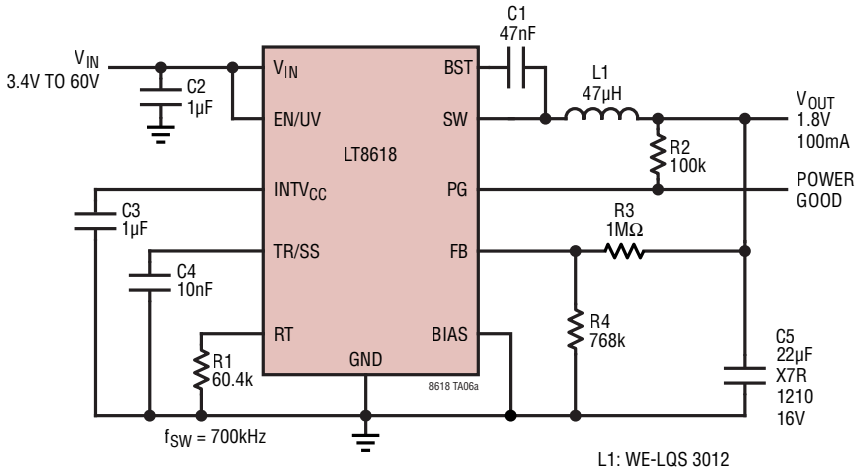
Typical Performance Minimum Load to Full Frequency



Rev. B

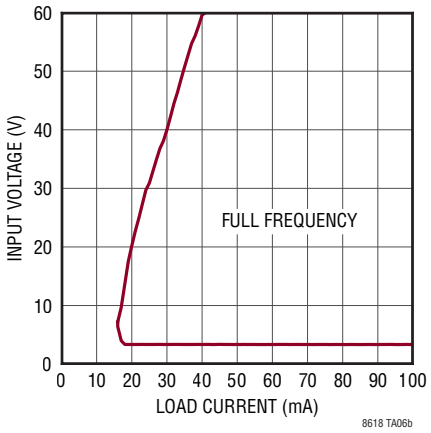
TYPICAL APPLICATIONS

1.8V Step-Down Converter

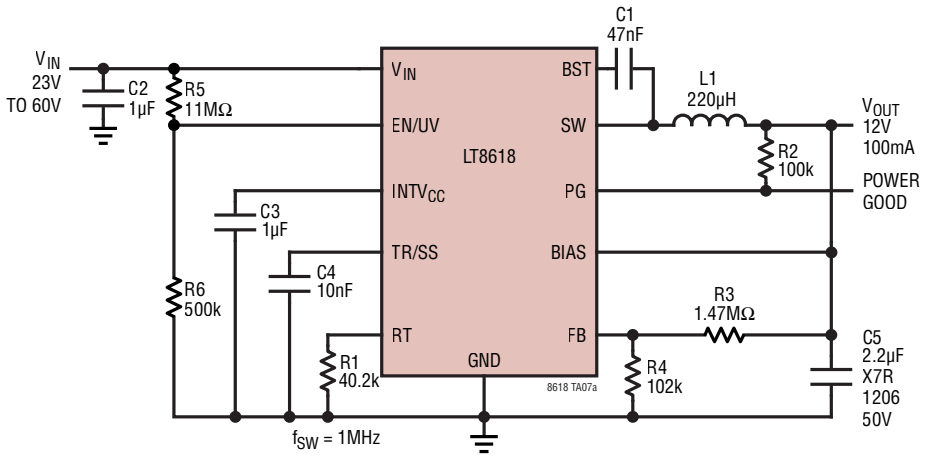


L1: WE-LQS 3012

Typical Performance Minimum Load to Full Frequency

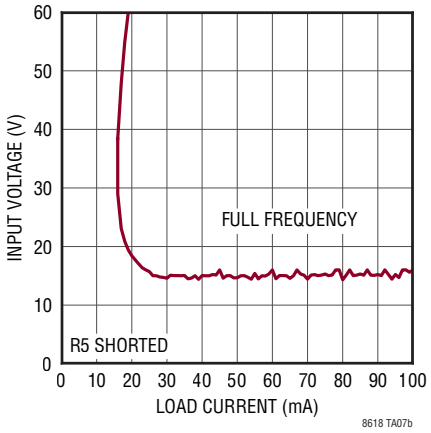


12V Step-Down Converter with Undervoltage Lockout

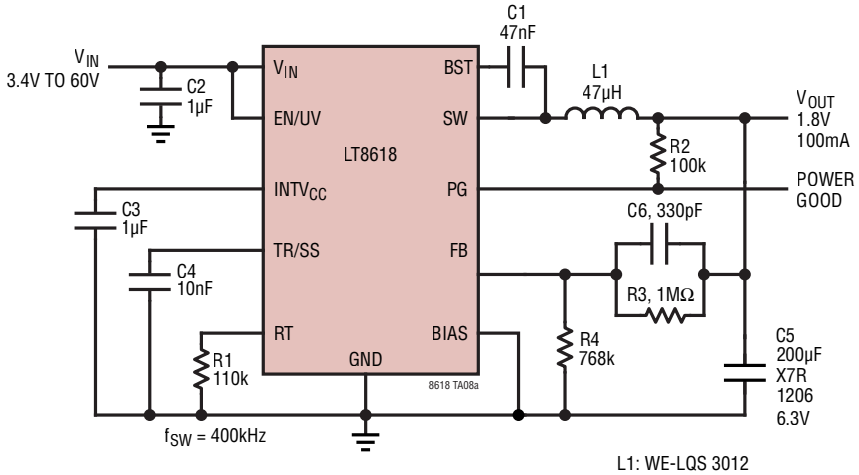


L1: WE-LQS 4025

Typical Performance Minimum Load to Full Frequency

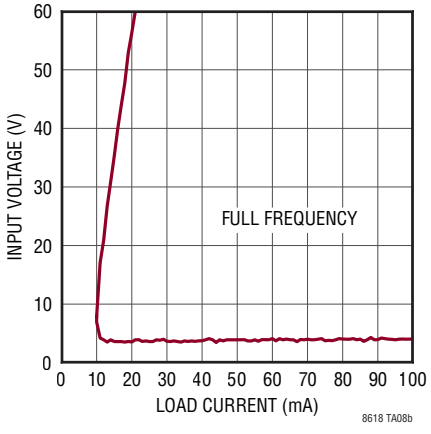


1.8V Step-Down Converter with Large Output Capacitor



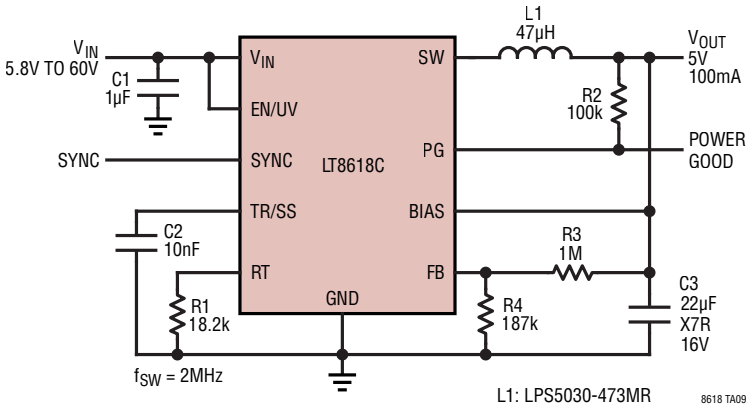
L1: WE-LQS 3012

Typical Performance Minimum Load to Full Frequency

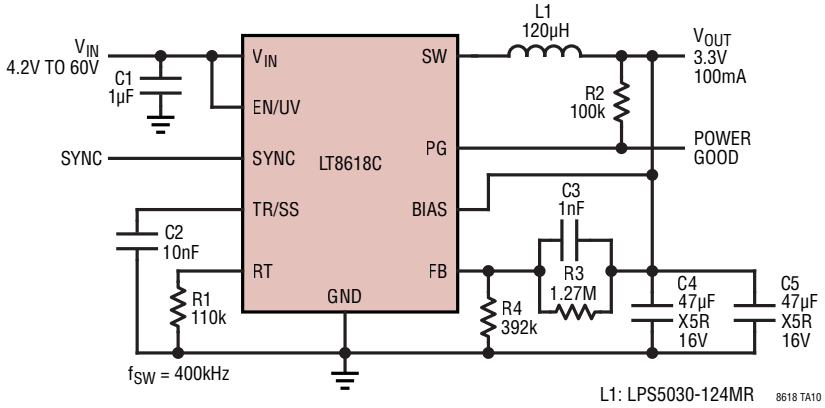


TYPICAL APPLICATIONS

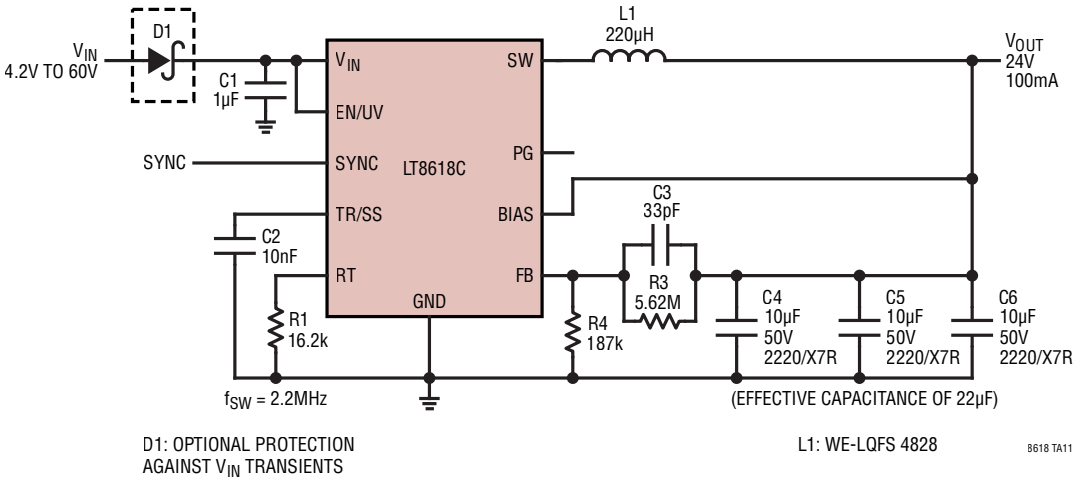
5V, 2MHz Step-Down Converter



3.3V, 400kHz Step-Down Converter

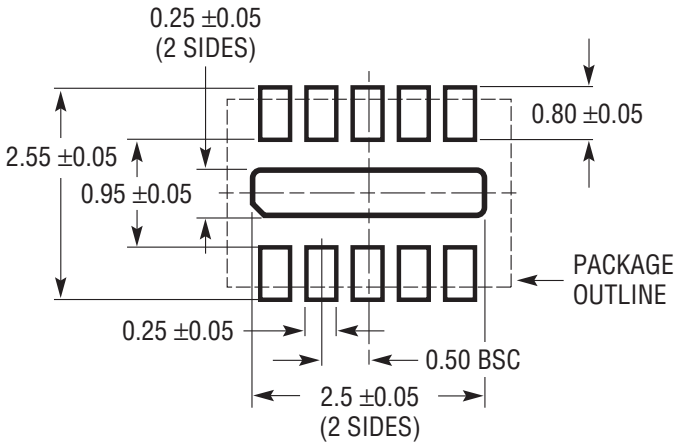


24V, 2.2MHz Step-Down Converter

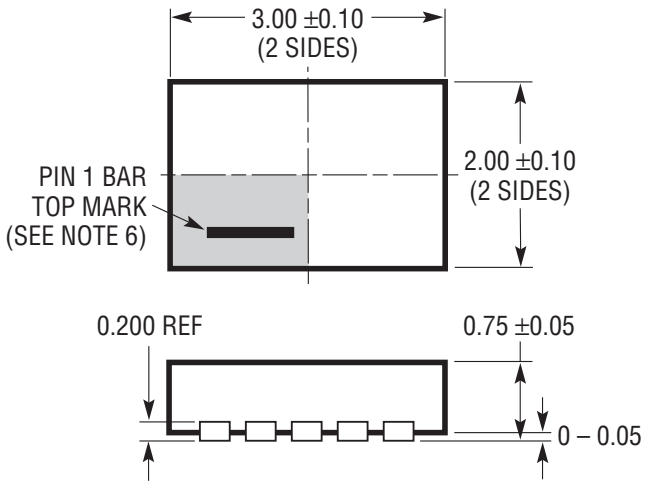


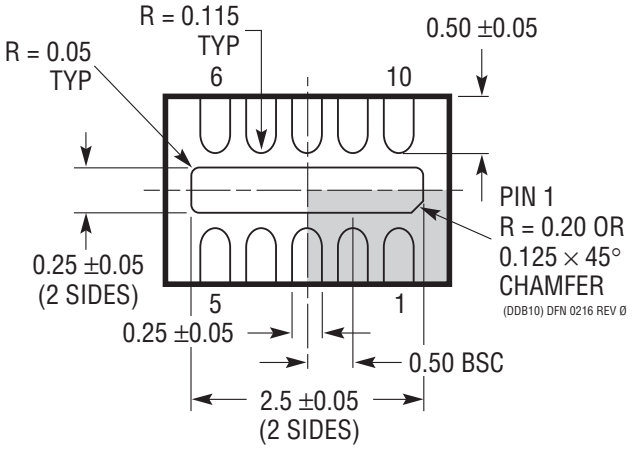
PACKAGE DESCRIPTION

DDB Package
10-Lead Plastic DFN (3mm × 2mm) COL
(Reference LTC DWG # 05-08-1531 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



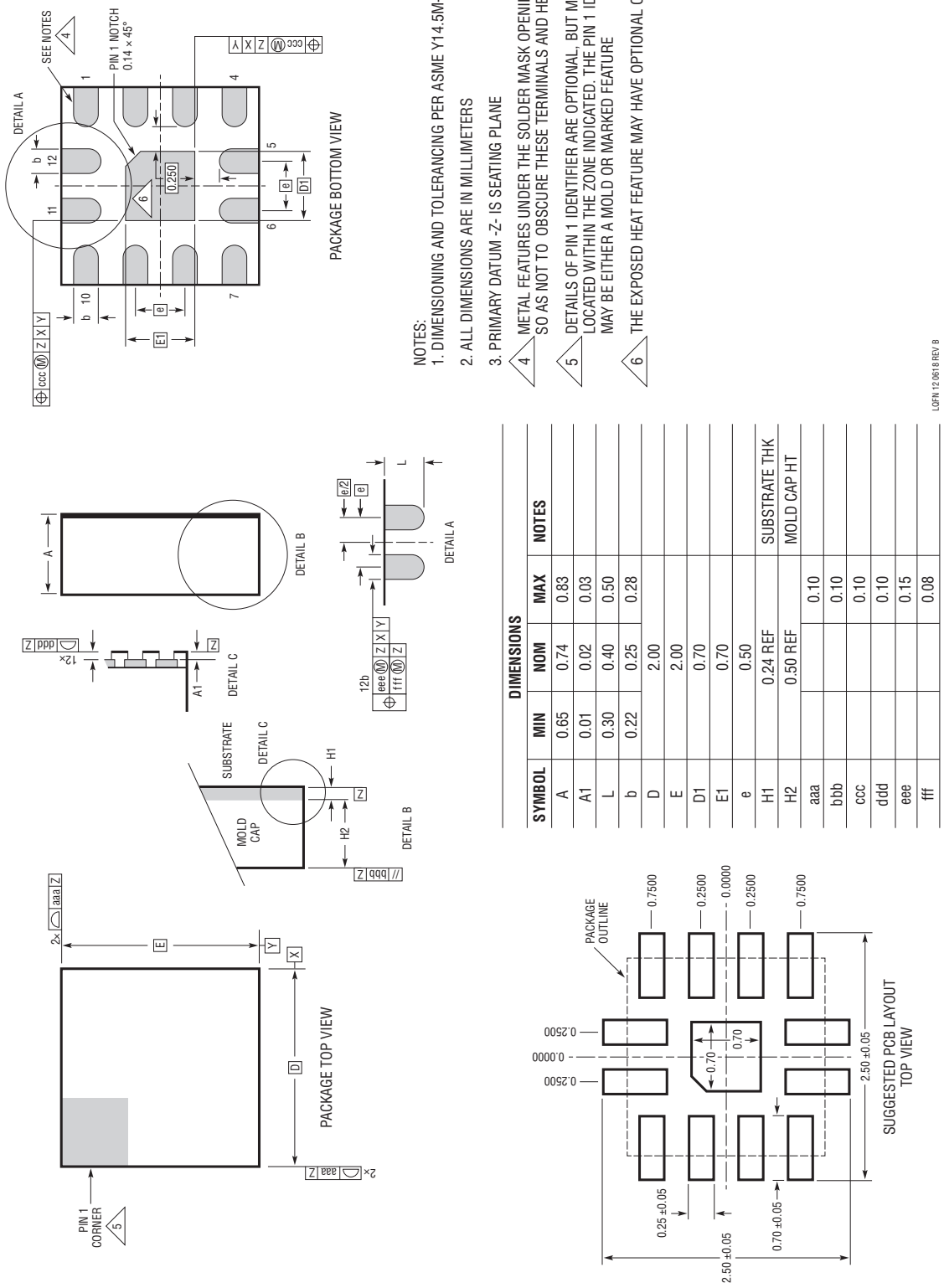


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

LQFN Package
12-Lead (2mm × 2mm × 0.74mm)
(Reference LTC DWG # 05-08-1530 Rev B)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.65	0.74	0.83	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		2.00		
E		2.00		
D1		0.70		
E1		0.70		
e		0.50		
H1		0.24 REF		SUBSTRATE THK
H2		0.50 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/21	Update to Features and Description.	1
		Addition of LQFN package option and grade option for DFN package.	2
		Addition of electrical characteristics for LQFN package.	4
		Addition of performance characteristics for LQFN package.	4-9
		Addition of block diagram for LQFN package.	12
		Addition of PCB layout for LQFN package.	21
		Addition of typical applications for LQFN package.	24
		Updates to text.	10, 13-22
B	11/22	Correction of Typos in Block Diagram of LT8618C.	12
		Correction of Typo in L_{MIN} expression.	15
		DDB Package Outline Drawing Version Updated.	25