

Product Summary

Part Number	$V_{(BR)DS}$ Min (V)	$V_{GS(th)}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD5000I	20	1.5	70 @ $V_{GS} = 5$ V	0.5	2
SD5000N	20	1.5	70 @ $V_{GS} = 5$ V	0.5	2
SD5001N	10	1.5	70 @ $V_{GS} = 5$ V	0.5	2
SD5400CY	20	1.5	75 @ $V_{GS} = 5$ V	0.5	2
SD5401CY	10	1.5	75 @ $V_{GS} = 5$ V	0.5	2

Features

- Quad SPST Switch with Zener Input Protection
- Low Interelectrode Capacitance and Leakage
- Ultra-High Speed Switching— t_{ON} : 1 ns
- Ultra-Low Reverse Capacitance: 0.2 pF
- Low Guaranteed r_{DS} @5 V
- Low Turn-On Threshold Voltage

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- Video Switch
- Multiplexer
- DAC Deglitchers
- High-Speed Driver

Description

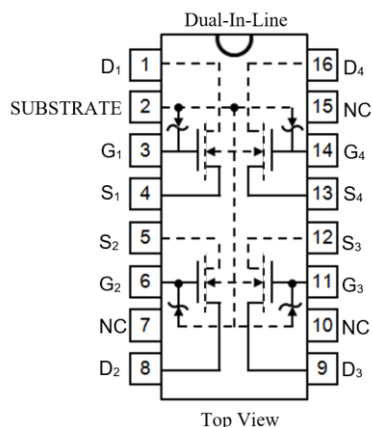
The SD5000/5400 series of monolithic switches features four individual double-diffused enhancement-mode MOSFETs built on a common substrate. These bidirectional devices provide low on-resistance and low interelectrode capacitances to minimize insertion loss and crosstalk.

Built on Siliconix' proprietary DMOS process, the SD5000/5400 series utilizes lateral construction to achieve low capacitance and

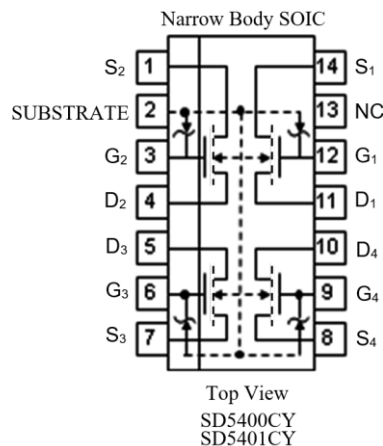
ultra-fast switching speeds. For manufacturing reliability, these devices feature poly-silicon gates protected by Zener diodes

The SD 5000/5400 are rated to handle ± 10 -V analog signals, while the SD5001/5401 are rated for ± 5 -V signals.

For similar products packaged in TO-206AF (TO-72) and TO-253 (SOT-143) see the SD211DE/SST211 series.



Plastic: SD5000N
SD5001N
Sidebrazed: SD5000I



SD5000/5001/5400/5401

Quad N-Channel Lateral DMOS Switch, Zener Protected

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Gate-Drain, Gate-Source Voltage (SD5000, SD5400).....	+30V/-25V
(SD5001, SD5401).....	+25V/-15V
Gate-Substrate Voltage (SD5000, SD5400).....	+30V/-0.3V
(SD5001I, SD5401).....	+25V/-0.3V
Drain-Source Voltage (SD5000, SD5400).....	20V
(SD5001I, SD5401).....	10V
Drain-Source-Substrate Voltage (SD5000, SD5400).....	25V
(SD5001I, SD5401).....	15V

Drain Current.....	50 mA
Lead Temperature (1/16" from case for 10 seconds).....	300°C
Storage Temperature.....	-65 to 150°C
Operating Junction Temperature.....	-55 to 150°C
Power Dissipation": (Package).....	500 mW
(each Device).....	300 mW

Notes:

- a. SD5000/SD5001I derate 5 mW/C above 25°C
- b. SD5400/SD5401 derate 4 mW/C above 25°C

Specifications^a

Parameter	Symbol ^b	Test Conditions ^b	Typ ^c	Limits				Unit
				SD5000 SD5400		SD5001 SD5401		
				Min	Max	Min	Max	
Static								
Drain-Source Breakdown Voltage	V _{(BR)DS}	V _{GS} =V _{BS} =-5V, I _D =10nA	30	20		10		V
Source-Drain Breakdown Voltage	V _{(BR)SD}	V _{GD} =V _{BD} =-5V, I _S =10nA	22	20		10		
Drain-Substrate Breakdown Voltage	V _{(BR)DBO}	V _{GB} =0 V, I _D =10μA, Source Open	35	25		15		
Source-Substrate Breakdown Voltage	V _{(BR)SBO}	V _{GB} =0 V, I _S =10μA, Drain Open	35	25		15		
Drain-Source Leakage	I _{DS(off)}	V _{GS} = V _{BS} =-5 V	V _{DS} = 10 V	0.4			10	nA
			V _{DS} = 15 V	0.7				
			V _{DS} = 20 V	0.9		10		
Source-Drain Leakage	I _{SD(off)}	V _{GD} = V _{BD} =-5 V	V _{SD} = 10 V	0.5			10	
			V _{SD} = 15 V	0.8				
			V _{SD} = 20 V	1		10		
Gate Leakage	I _{GBS}	V _{DB} = V _{SB} = 0 V, V _{GB} =30V	0.01		100	100		
Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 μA, V _{SB} =0V	0.8		1.5	1.5	V	
Drain-Source On-Resistance	r _{DS(on)}	V _{SB} = 0 V I _D = 1 mA	SD5000 Series V _{GS} = 5 V	58		70	70	Ω
			SD5400 Series V _{GS} = 5 V	60		75	75	
			V _{GS} = 10 V	38				
			V _{GS} = 15 V	30				
			V _{GS} = 20 V	26				
Resistance Match	Δr _{DS(on)}	V _{GS} = 5 V	1		5	5		
Dynamic								
Forward Transconductance	g _{fs}	V _{DS} = 10 V V _{SB} = 0 V I _D = 20 mA f = 1 kHz	SD5000 Series	12	10		10	mS
			SD5400 Series	11	9		9	
Gate Node Capacitance	C _(GS+GD+GB)	V _{DS} = 10 V f = 1 MHz V _{GS} = V _{BS} = -15V	SD5000 Series	2.5		3.5	3.5	pF
Drain Node Capacitance	C _(GD+DB)			2.0		3	3	
Source Node Capacitance	C _(GS+SB)			3.7		5	5	
Reverse Transfer Capacitance	C _{rSS}			0.2		0.5	0.5	
Crosstalk		f = 3 kHz		-107				dB

SD5000/5001/5400/5401

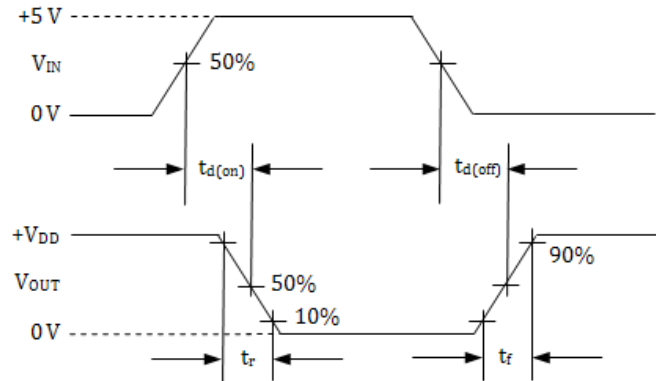
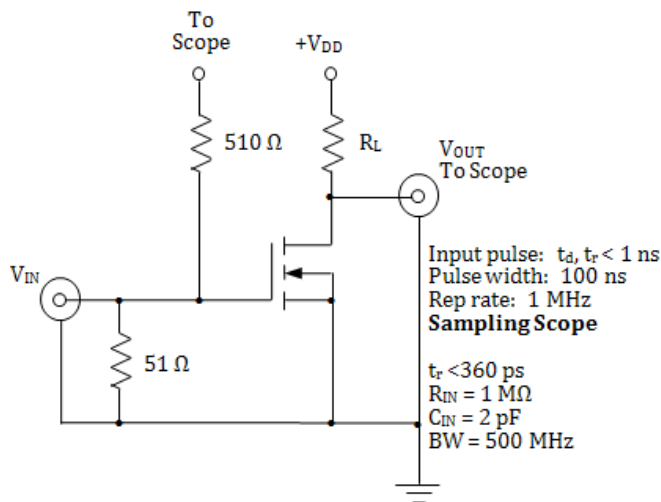
Quad N-Channel Lateral DMOS Switch, Zener Protected

Specifications^a

Parameter	Symbol ^b	Test Conditions ^b	Typ ^c	Limits				Unit
				SD5000 SD5400		SD5001 SD5401		
				Min	Max	Min	Max	
Switching								
Turn-On Time	$t_{d(on)}$	$V_{SB} = 1-5 V_{in}, V_{GN} 0 \text{ to } 5 V, R_G = 25 \Omega$ $V_{DD} = 5 V, R_L = 680 \Omega$	0.5		1		1	ns
	t_r		0.6		1		1	
Turn-Off Time	$t_{d(off)}$		2					
	t_f		6					

DMCA

Switching Time Test Circuit



V_{IN}	Switch (On/Off)	V_{OUT}
High	On	GND
Low	Off	VDD

Notes:

- $T_A = 25^\circ\text{C}$ unless otherwise noted.
- B is the body (substrate) and $V_{(BR)}$ is breakdown.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
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