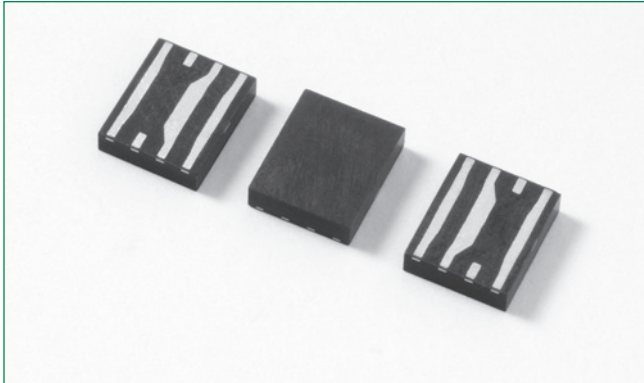


**SDPXXX0Q38CX -SDP Biased Series - 5x6 QFN for DSL Protection**



**Description**

This new SDP (SIDActo<sup>®</sup>r DSL Protector) Biased series provides overvoltage protection for applications such as VDSL2, ADSL2, and ADSL2+ with minimal effect on data signals. This latest silicon design innovation results in a capacitive loading characteristic that is compatible with these high bandwidth applications. This surface mount QFN package provides a surge capability that exceeds most worldwide standards and recommendations for lightning surge withstand capability of secondary protectors.

**Features & Benefits**

- Compatible with VDSL2 (30MHz)
- Balanced overvoltage protection
- Low distortion
- Low insertion loss
- Low profile
- SO-8 footprint compatible
- Fails short circuit when surged in excess of ratings
- 2nd level interconnect is Pb-free per IPC/JEDEC J-STD-609A.01
- Recognized to UL 497B as an Isolated Loop Circuit Protector
- Halogen-free and RoHS compliant

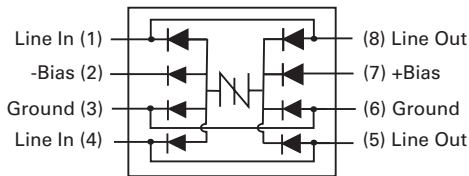
**Agency Approvals**

Agency	Agency File Number
	E133083

**Pinout Designation**

Tip in	1	8	Tip out
- Bias	2	7	+ Bias
Ground	3	6	Ground
Ring in	4	5	Ring out

**Schematic Symbol**



**Applicable Global Standards**

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- IEC 61000-4-5, 2nd Edition
- GR 1089 Inter-building
- GR 1089 Intra-building
- YD/T 1082
- YD/T 993
- YD/T 950

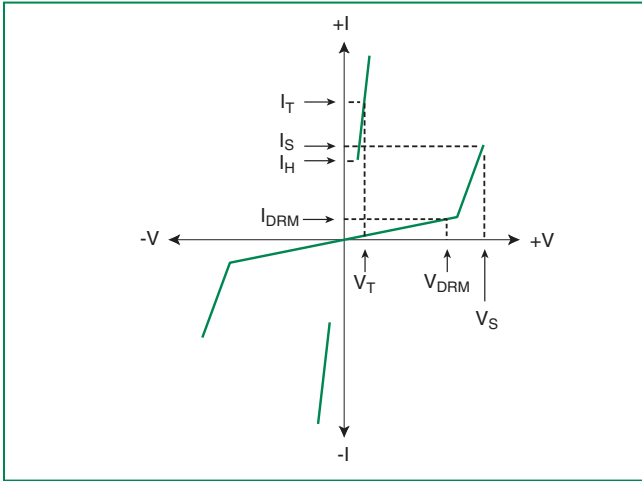
**Electrical Characteristics**

Part Number	Marking	$V_{DRM}@I_{DRM}=5\mu A$	$V_s@100V/\mu s$	$I_H$	$I_s$	$I_T$	$V_T@I_T=2.2$ Amps	Capacitance
		V min	V max	mA min	mA max	A max	V max	
SDP0080Q38CB	SDP-8C	6	25	50	800	2.2	8	See Capacitance vs Voltage Chart
SDP0220Q38CB	SDP02C	16	30	50	800	2.2	8	
SDP0640Q38CB	SDP06C	58	77	150	800	2.2	8	
SDP0720Q38CB	SDP07C	65	88	150	800	2.2	8	
SDP0900Q38CB	SDP09C	75	98	150	800	2.2	8	
SDP1100Q38CB	SDP11C	90	130	150	800	2.2	8	
SDP1300Q38CB	SDP13C	120	160	150	800	2.2	8	
SDP1800Q38CB	SDP18C	170	220	150	800	2.2	8	
SDP2600Q38CB	SDP26C	220	300	150	800	2.2	8	
SDP3100Q38CB	SDP31C	275	350	150	800	2.2	8	
SDP3500Q38CB	SDP35C	320	400	150	800	2.2	8	

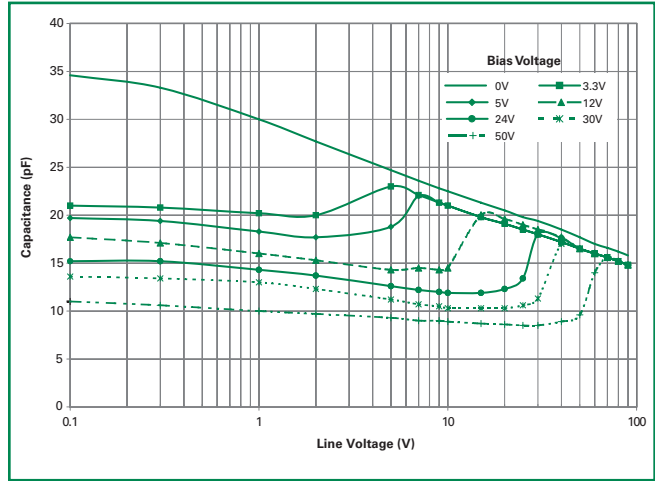
**Notes:**

- Absolute maximum ratings measured at  $T_A=25^\circ C$  (unless otherwise noted).
- Devices are bi-directional (unless otherwise noted).

**V-I: Characteristics**



**Capacitance vs. Voltage\***



\* Bias voltage must be lower than  $V_{DRM}$

**50/60Hz Ratings**

Parameter Name	Test Conditions	Value	Units
$I_{TSM}$ Maximum non-repetitive on-state current, 50/60Hz	0.5s	6.5	A
	1s	4.6	
	2s	3.4	
	5s	2.3	
	30s	1.3	
	900s	0.73	

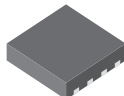
**Surge Ratings**

Series	$I_{PP}$				$I_{TSM}$
	2x10 $\mu$ s	1.2x50 $\mu$ s/8x20 $\mu$ s	10x700/5x310 $\mu$ s	10x1000 $\mu$ s	600V <sub>RMS</sub> 1 cycle
	A min	A min	A min	A min	A <sub>RMS</sub>
C	500	400	200	100	30

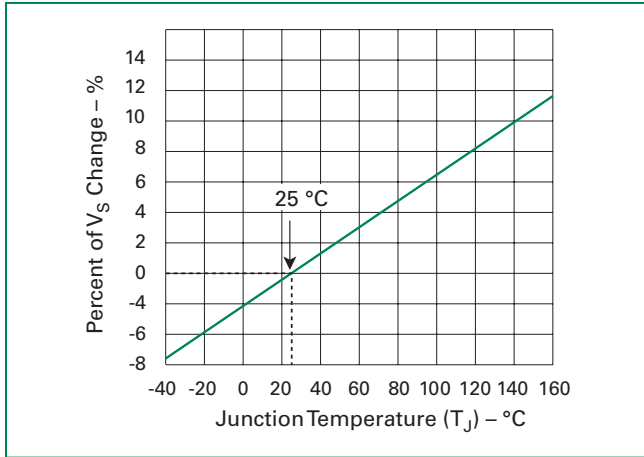
**Notes:**

- Peak pulse current rating ( $I_{pp}$ ) is repetitive and guaranteed for the life of the product.
- $I_{pp}$  ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C  $\leq$   $T_J$   $\leq$  +150°C

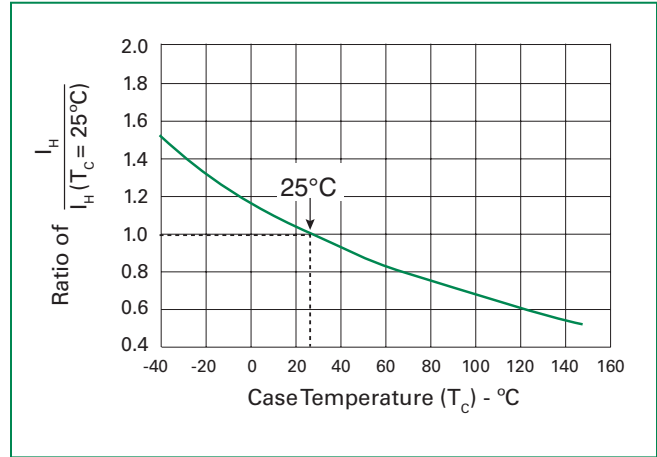
**Thermal Considerations**

Package	Symbol	Parameter	Value	Unit
 5x6 QFN	$T_J$	Junction Temperature	-40 to +150	°C
	$T_{STG}$	Storage Temperature Range	-40 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	100	°C/W

**Normalized  $V_s$  Change vs. Junction Temperature**

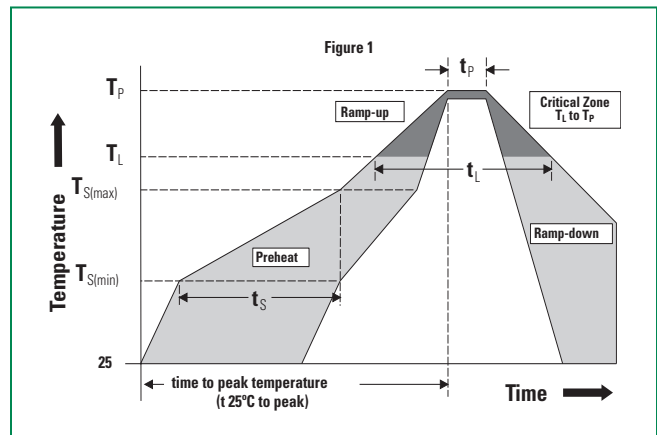


**Normalized DC Holding Current vs. Case Temperature**



**Soldering Parameters**

<b>Reflow Condition</b>	Pb-Free assembly (see Fig. 1)	
<b>Pre Heat</b>	- Temperature Min ( $T_{s(\text{min})}$ )	+150°C
	- Temperature Max ( $T_{s(\text{max})}$ )	+200°C
	- Time (Min to Max) ( $t_s$ )	60-180 secs.
<b>Average ramp up rate (Liquidus Temp (<math>T_L</math>) to peak)</b>	3°C/sec. Max.	
<b><math>T_{s(\text{max})}</math> to <math>T_L</math> - Ramp-up Rate</b>	3°C/sec. Max.	
<b>Reflow</b>	- Temperature ( $T_L$ ) (Liquidus)	+217°C
	- Temperature ( $t_L$ )	60-150 secs.
<b>Peak Temp (<math>T_p</math>)</b>	+260(+0/-5)°C	
<b>Time within 5°C of actual Peak Temp (<math>t_p</math>)</b>	30 secs. Max.	
<b>Ramp-down Rate</b>	6°C/sec. Max.	
<b>Time 25°C to Peak Temp (<math>T_p</math>)</b>	8 min. Max.	
<b>Do not exceed</b>	+260°C	



**Physical Specifications**

<b>Lead Material</b>	Copper Alloy
<b>Terminal Finish</b>	100% Matte-Tin Plated
<b>Body Material</b>	UL Recognized epoxy meeting flammability classification 94V-0

**Additional Information**



Datasheet



Resources

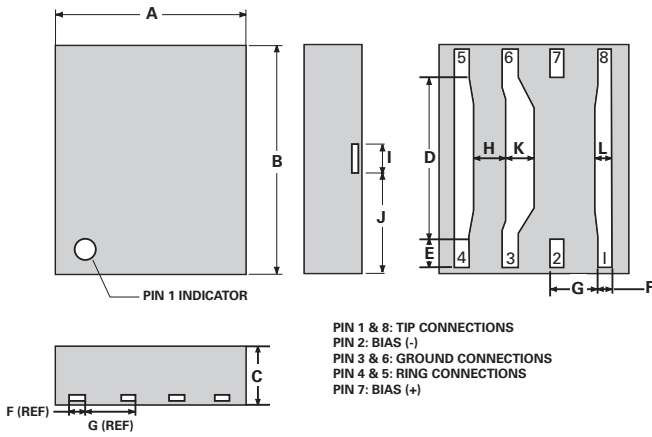


Samples

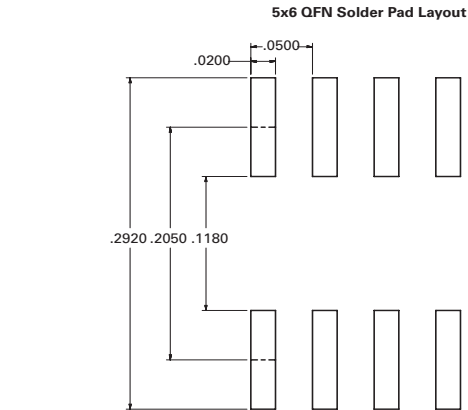
**Environmental Specifications**

<b>High Temp Voltage Blocking</b>	80% Rated $V_{\text{DRM}}$ ( $V_{\text{AC Peak}}$ ) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
<b>Temp Cycling</b>	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
<b>Biased Temp &amp; Humidity</b>	52 $V_{\text{DC}}$ (+85°C) 85% RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
<b>High Temp Storage</b>	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
<b>Low Temp Storage</b>	-65°C, 1008 hrs.
<b>Thermal Shock</b>	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
<b>Resistance to Solder Heat</b>	+260°C, 30 secs. MIL-STD-750 (Method 2031)
<b>Moisture Sensitivity Level</b>	85% RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

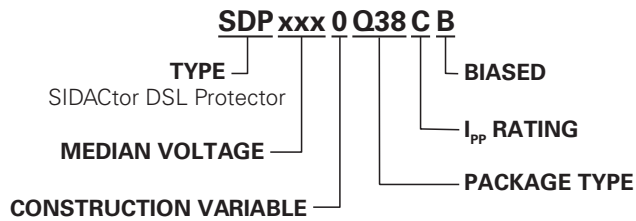
**Dimensions — 5x6 QFN**



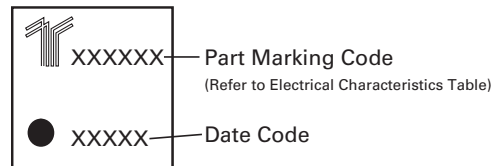
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.187	0.207	4.745	5.253
B	0.226	0.246	5.745	6.253
C	0.054	0.064	1.374	1.628
D	0.165	0.171	4.199	4.351
E	0.027	0.033	0.686	0.838
F	0.011	0.017	0.279	0.432
G	0.047	0.053	1.194	1.346
H	0.032	0.038	0.800	0.953
I	0.027	0.033	0.686	0.838
J	0.100	0.106	2.540	2.692
K	0.027	0.033	0.686	0.838
L	0.015	0.021	0.381	0.533



**Part Numbering**



**Part Marking**



**Packing Options**

Package Type	Description	Quantity	Added Suffix	Industry Standard
Q38	5x6x1.5 QFN Tape and Reel Pack	4000	N/A	EIA-481-D