BURST[1:0]	FUNCTION
00	no
01	READ
10	no
11	READ/COMP

16.2.6 PARALLEL ACCESS TO TEST PORT INTERFACE

Parallel access for the 8051 CPU. This enables parallel writes to the OTP Data and Mode registers.

16.2.6.1 OTP CPU Test Port Command Instruction Register

TABLE 16-9: CPU TEST PORT COMMAND INSTRUCTION REGISTER

CPU_TCMD_REG (0X36 - RESET = 0X10)			OTP TEST PORT COMMAND REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7:5	Reserved	R	Always read as 0
4	TRSTN	R/W	OTP Test Port reset of TMODE, CMD, SHIFT registers.
3	TCLRN	R/W	OTP Test Port clear of the command register.
2:0	TCMD[2:0]	R/W	OTP Test Port Command instruction

16.2.6.2 OTP CPU Test Port Control Register

TABLE 16-10: CPU TEST PORT CONTROL REGISTER

CPU_TCTL_REG (0X37 - RESET = 0X00)			OTP TEST PORT CONTROL REGISTER
BIT	**NAME**	**R/W**	**DESCRIPTION**
7	COUNT_EN	R/W	Generate clocks in TSCK, COUNT times. If this bit is set, TSCK is generated every CPU clock and COUNT field is decrement by one; until COUNT field becomes zero.
6:0	COUNT[5:0]	R/W	Indicated number of TSCK clocks to generate

16.2.6.3 OTP CPU Test Port Shift Register

TABLE 16-11: CPU TEST PORT SHIFT REGISTER

CPU_SHIFT_REG (0X38 ~ 0X3B- RESET = 0X00)			OTP TEST PORT SHIFT REGISTER
BYTE	**NAME**	**R/W**	**DESCRIPTION**
0	SHIFT[7:0]	R/W	OTP Test Port Shift register. The mapping of shift register bits to TMODE, CMD, ADDRESS registers of OTP is shown in Table 16-7.
1	SHIFT[15:8]	R/W	
2	SHIFT[23:16]	R/W	
3	SHIFT[31:24]	R/W	