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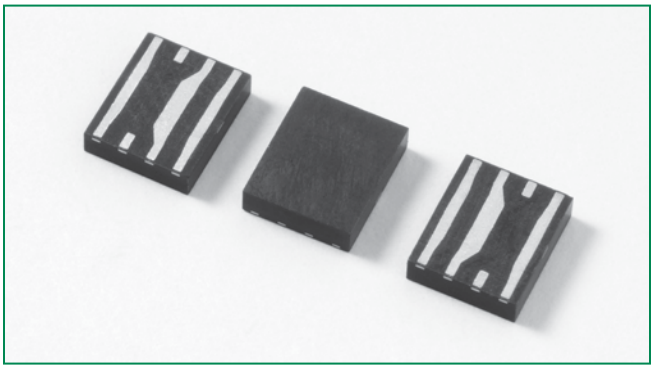
SIDACtor® Protection Thyristors
Broadband Optimized™ Protection

SEP Biased Series - 5x6 QFN

HF RoHS



Description

The new SEP (SIDACtor Thyristor Ethernet/PoE Protector) series has a surge rating compatible with GR1089 inter-building and ITU K.20/21 Enhanced protection requirements. Targeted for high-speed applications such as 10BaseT, 100BaseT, and 1000BaseT, the SEP series maintains signal quality while providing robust protection for Ethernet and PoE applications. This latest silicon design innovation results in a capacitive loading characteristic that is constant with respect to the voltage across the component. This reduces distortion caused by typical solid-state protection solutions. Offered in a surface-mount, QFN package, the SEP provides small package size without sacrificing power and surge handling capabilities.

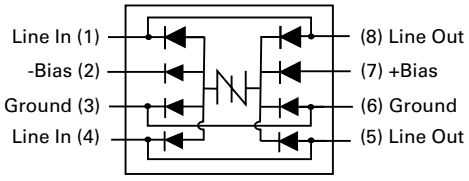
Agency Approvals

Agency	Agency File Number
	E133083

Pinout Designation

Line in	1	8	Line out
- Bias	2	7	+ Bias
Ground	3	6	Ground
Line in	4	5	Line out

Schematic Symbol



Features & Benefits

- Compatible with 1000Base-T
- Balanced overvoltage protection
- Low distortion
- Low insertion loss
- Low profile
- SO-8 footprint compatible
- Fails short circuit when surged in excess of ratings
- RoHS Compliant and Halogen-Free
- Pb-free E3 means 2nd level interconnect is Pb-free and the terminal finish material is tin(Sn) (IPC/JEDEC J-STD-609A.01)

Applicable Global Standards

- TIA-968-A
- TIA-968-B
- ITU K.20/21 Enhanced Level
- ITU K.20/21 Basic Level
- IEC 61000-4-5 2nd edition
- GR 1089 Inter-building
- GR 1089 Intra-building
- YD/T 1082
- YD/T 993
- YD/T 950
- Class 4/5 compliance of IEC 61000--4-5

Additional Information

Datasheet | **Resources** | **Samples**

Electrical Characteristics

Part Number	Marking	V_{DRM} @ I_{DRM}=5µA	V_S @ 100V/µs	I_H	I_S	I_T @ V_T	V_T @ I_T= 2.2Amps	Capacitance
		V min	V max	mA min	mA max	A max	V max	
SEP0080Q38CB	SEP-8C	6	25	50	800	2.2	8	See Capacitance vs. Bias Voltage Graph
SEP0640Q38CB	SEP06C	58	77	150	800	2.2	8	
SEP0720Q38CB	SEP07C	65	88	150	800	2.2	8	
SEP0900Q38CB	SEP09C	75	98	150	800	2.2	8	
SEP0080Q38BB	SEP-8B	6	25	50	800	2.2	8	
SEP0640Q38BB	SEP06B	58	77	150	800	2.2	8	
SEP0720Q38BB	SEP07B	65	88	150	800	2.2	8	
SEP0900Q38BB	SEP09B	75	98	150	800	2.2	8	

Notes:
- Absolute maximum ratings measured at T_A= 25°C (unless otherwise noted).
- Components are bidirectional (unless otherwise noted).

Revised: 08/29/18

50/60 Hz Ratings

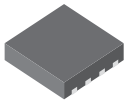
Parameter Name	Test Conditions	Value	Units
I_{TSM} Maximum non-repetitive on-state current, 50/60 Hz	0.5s	6.5	A
	1s	4.6	
	2s	3.4	
	5s	2.3	
	30s	1.3	
	900s	0.73	

Surge Ratings

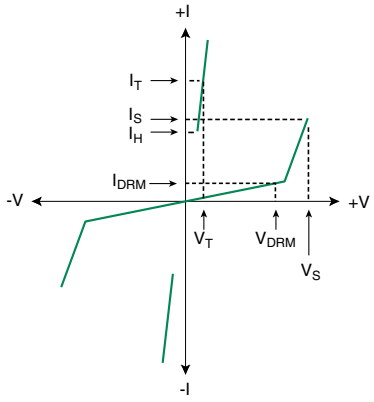
Series	I_{PP}				I_{TSM}
	2x10µs	1.2/50µs-8/20µs	10/700-5/310µs	10x1000µs	$600V_{RMS}$ 1 cycle
	A min	A min	A min	A min	A_{RMS}
B	250	250	100	80	30
C	500	430	200	100	30

Notes:
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product as long as it returns to 25C° between surges
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The components must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C

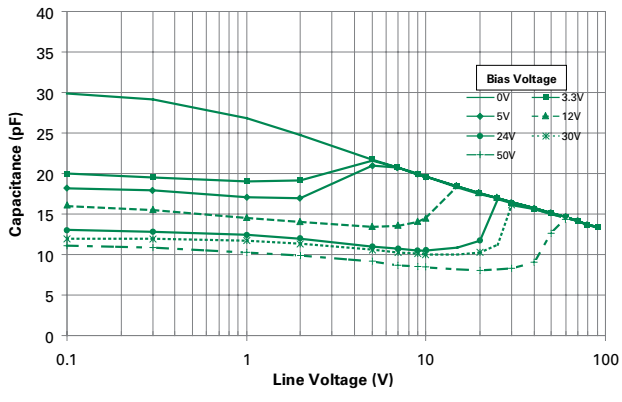
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
 5x6 QFN	T_J	Junction Temperature	-40 to +150	°C
	T_{STG}	Storage Temperature Range	-40 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	100	°C/W

V-I Characteristics



Capacitance vs. Bias Voltage*



* Bias voltage must be lower than V_{DRM}

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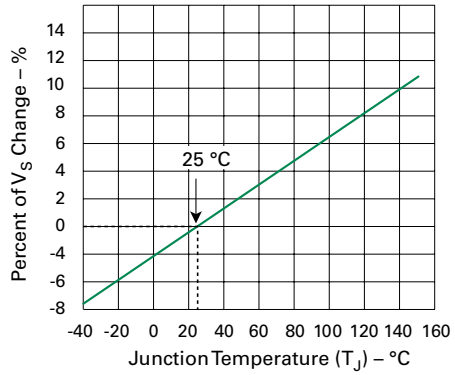
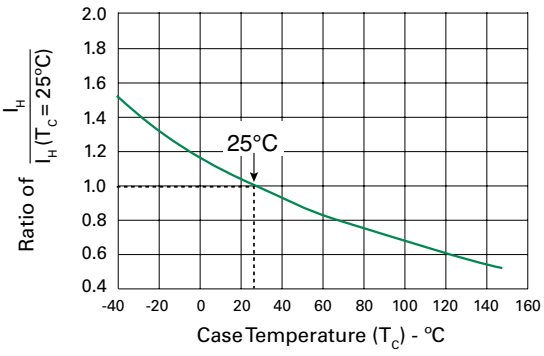
Normalized V_S Change vs. Junction Temperature



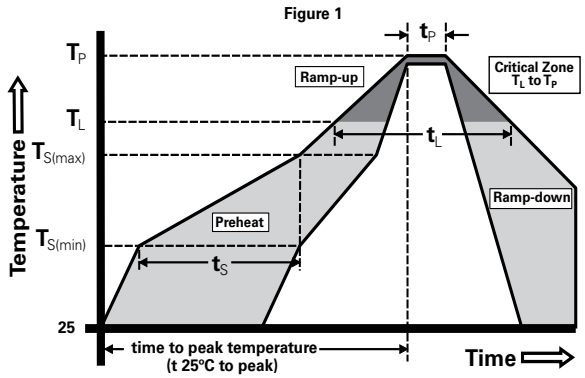
Normalized DC Holding Current vs. Case Temperature



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL Recognized compound meeting flammability rating V-0

Environmental Specifications

High Temp Voltage Blocking	80% Rated V_{DRM} (V_{AC} Peak) +125°C or +150°C, 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 V_{DC} (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles (+260°C Peak). JEDEC-J-STD-020, Level 1

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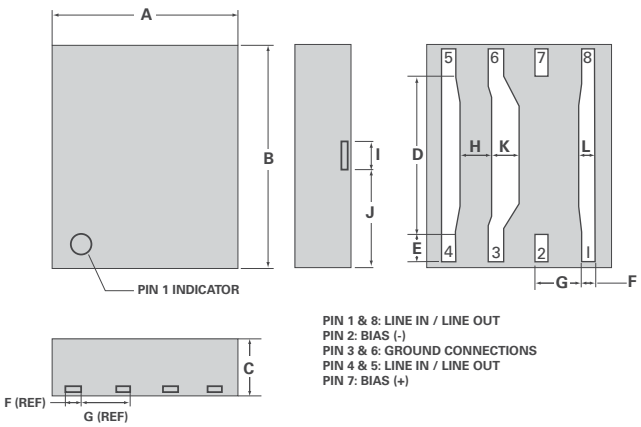
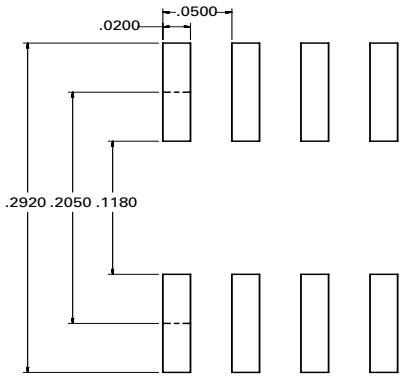
Dimensions — 5x6 QFN

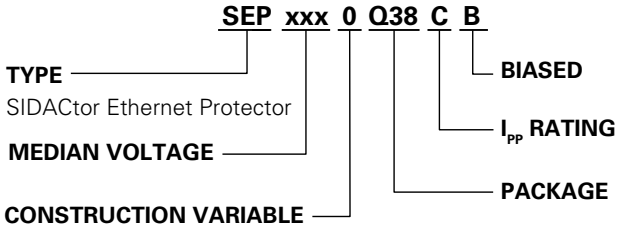


Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.187	0.207	4.745	5.253
B	0.226	0.246	5.745	6.253
C	0.054	0.064	1.374	1.628
D	0.165	0.171	4.199	4.351
E	0.027	0.033	0.686	0.838
F	0.011	0.017	0.279	0.432
G	0.047	0.053	1.194	1.346
H	0.032	0.038	0.800	0.953
I	0.027	0.033	0.686	0.838
J	0.100	0.106	2.540	2.692
K	0.027	0.033	0.686	0.838
L	0.015	0.021	0.381	0.533

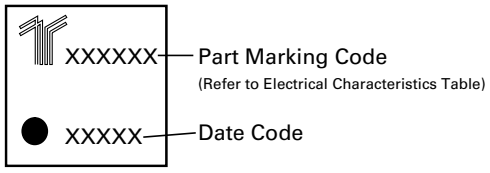
5x6 QFN Solder Pad Layout



Part Numbering



Part Marking



Packing Options

Package Type	Description	Quantity	Added Suffix	Industry Standard
Q38	5x6x1.5 QFN Tape and Reel	4,000	N / A	EIA-481-D

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