swissbit®

Product Fact Sheet

Industrial e•MMC Memory

EM-36 Series

JEDEC e•MMC 5.1 compliant,
BGA 100 ball, Enhanced Mode (pSLC)

Industrial Temperature Grade

Date: June 24, 2022
Revision: 1.00

Made in Germany

Product Fact Sheet
EM-36 Series

swissbit®

Product Summary

- **Capacities:** 5 GBytes, 10 GBytes, 20 GBytes, 40 GBytes, 80 GBytes
- **Operating Temperature Range[1]:** Industrial Operating Temperature -40 to 85°C
- **Endurance in TeraBytes Written (TBW) @ Max Capacity[2]:** up to 2652

Product Features

- Fully compliant with JEDEC e·MMC 5.1 Standard (JESD84-B51)
- 100-ball BGA, 1.0mm pitch
- 14 x 18mm, RoHS compliant
- 3D TLC NAND base technology in Enhanced Mode (pSLC)
- Industrial Operating Temperature -40 to 85°C
- Single enhanced mode partition
- High performance e·MMC 5.1 specification
  - Eleven-wire bus (clock, Data Strobe, 1 bit command, 8 bit data bus) and a hardware reset
  - Three different data bus width modes: 1-bit (default), 4-bit, and 8-bit
  - Clock frequencies 0-200MHz, High Speed Mode HS400
  - Command Queue Feature according to e·MMC Spec 5.1
  - Up to 300MB/s sequential read and up to 230MB/s sequential write
- Power Supply: (Low-power CMOS technology)
  - VCCQ 1.7V...1.95V or 2.7V...3.6V e·MMC supply
  - VCC 2.7V...3.6V NAND Flash supply
- Optimized FW algorithms
  - Power-fail data loss protection
  - Wear Leveling technology
    Equal wear leveling of static and dynamic data. The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is ensured
  - Read Disturb Management
    The read commands per region are monitored and the content is conditionally refreshed when critical levels have occurred
  - Auto Read Refresh
    The interruptible background process maintains the user data for Read Disturb effects or Retention degradation due to high temperature effects
  - Diagnostic features with Device Health Report according to e·MMC Spec 5.1, and detailed Lifetime Monitor data (Swissbit proprietary, accessible through standard e·MMC commands).
  - Field Firmware update[3] according to e·MMC Spec 5.1
  - Discard and Sanitize, Trim
  - Boot Operation Mode and Alternative Boot Operation Mode
  - Replay Protected Memory Block (RPMB)
- High reliability
  - Designed with sophisticated firmware architecture for industrial and embedded markets.
  - Enhanced Mode (pSLC) with higher write performance and endurance than 3D TLC configured products (EM-30).
  - Ideal for application like POS/POI, PLC, IoT, gaming, medical and use as general boot medium for embedded applications.
  - The product is optimized for long life cycle that requires superior data retention as well as power fail safety.
  - Controlled BOM & PCN process

[1] Adequate airflow is required to ensure the temperature does not exceed 85°C (industrial temperature drive)
[2] According to JEDEC (JESD47I), the time to write the full TBW is a minimum of 18 months. Higher average daily data volume reduces the specified TBW. The values listed are estimates and are subject to change without notice.
[3] The support of In-Field FW update capabilities on host systems is recommended.