Si2166-D60

DVB-S/S2/S2X Digital TV Demodulator

Description

The Si2166D integrates digital demodulators for first and second generation satellite DVB standards (DVB-S/S2 and S2X) in a single advanced CMOS die. Leveraging Silicon Labs' proven digital demodulation architecture, the Si2166D achieves excellent satellite reception performance while significantly minimizing front-end design complexity, cost, and power dissipation. Connecting the Si2166D to a satellite silicon tuner results in a high-performance and cost optimized TV or STB front-end solution.

The satellite reception allows demodulating widespread DVB-S, DIRECTV™ (DSS), DVB-S2, DIRECTV™ (AMC) legacy standards, and new Part II of DVB-S2 (S2X) satellite broadcast standard. A zero-IF interface (differential) allows for a seamless connection to market proven satellite silicon tuners. Si2166D embeds DiSEqC™ 2.0 LNB interface for satellite dish control and an equalizer to compensate for echoes in long cable feeds from the antenna to the satellite tuner input.

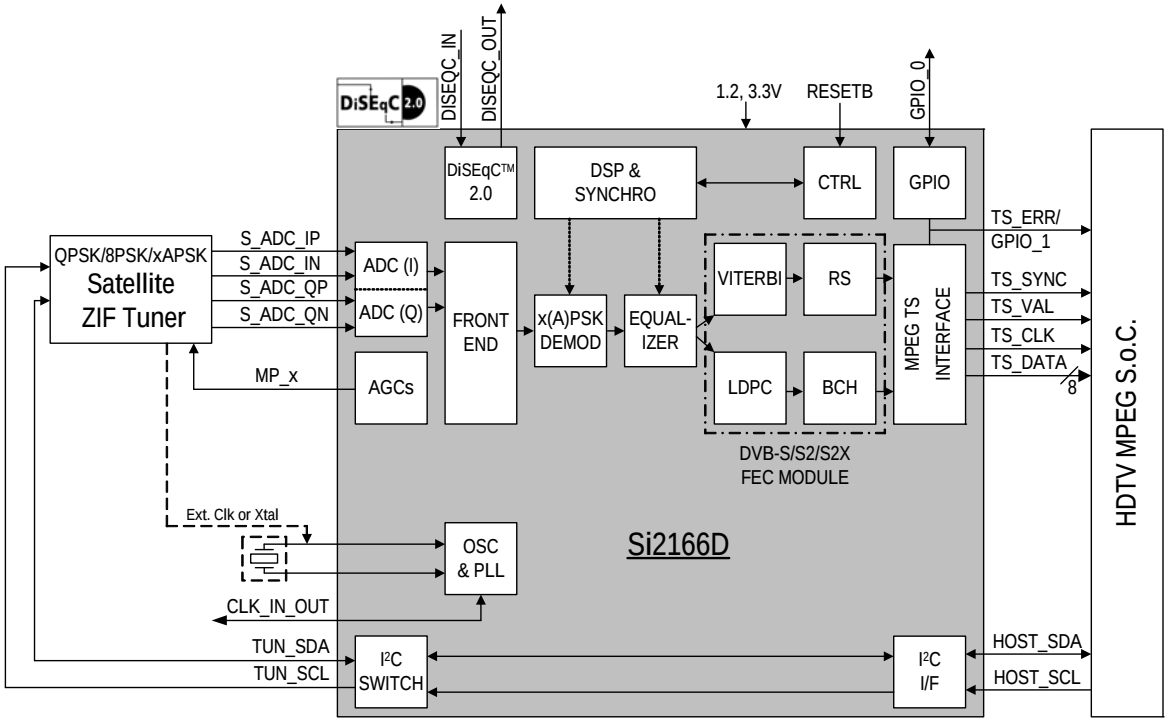
The Si2166D offers an on-chip blind scan algorithm for DVB-S/S2/S2X standards, as well as a blind lock function. The Si2166D programmable transport stream output interface provides a flexible range of output modes and is fully compatible with all MPEG decoders or conditional access modules to support any customer application.

Features

- Pin-to-pin compatible with all Si216x/8x single demods family
- API compatible with all single and dual demods families
- DVB-S2 (ETSI EN 302 307-1 V1.4.1)
  - QPSK/8PSK demodulator
- DVB-S2X (ETSI EN302 307-2 V1.1.1)
  - Support the normative broadcast services
  - QPSK/8PSK, 8/16/32APSKdemodulator
  - Roll-off factors from 0.05 to 0.35
  - VCM supported
  - ISSY and NPD supported
  - MIS supported
  - Output modes: TS, GPCS, and GSE-HEM supported
- DVB-S and DSS supported
  - QPSK demodulator and enhanced FEC decoder
- 1 to 45 MSymbol/s for all satellite standards (<40 MSps in 32APSK)
- LDPC and BCH FEC decoding for DVB-S2/S2X standards
- I^2C serial bus interfaces (master and host)
- Firmware control (embedded ROM/NVM)
- Upgradeable with patch download via I^2C or fast SPI
- Flexible TS output interface (serial, parallel, and slave)
- DiSEqC™ 2.0 interface and Unicable™ support
- Fast lock times
- Low power consumption
- Two power supplies: 1.2 and 3.3 V
- 7x7 mm, QFN-48 pin package, Pb-free/RoHS compliant

Applications

- Full-NIM
- iDTV (integrated Digital TV)
- Digital satellite STB
- PC-TV accessories
- PVR, DVD, and Blue Ray disc recorders



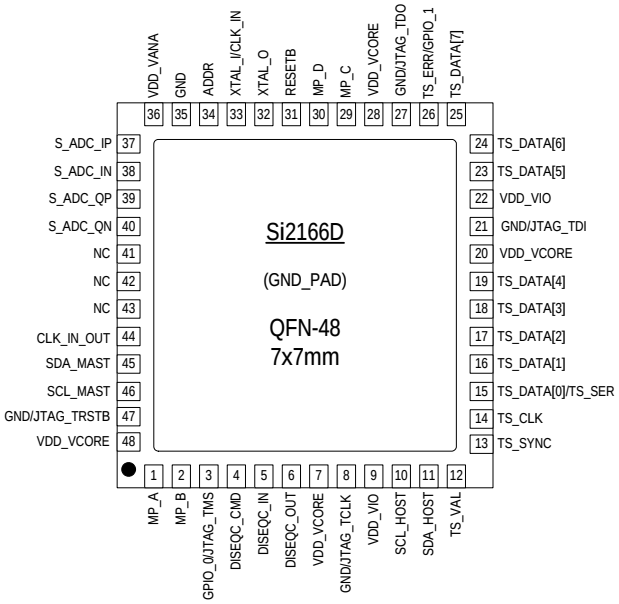
Selected Electrical Specifications

(T_A = –10 to 75 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
General					
Input clock reference		4	—	30	MHz
Supported XTAL frequency		16	—	30	MHz
Total power consumption	DVB-S2[1]	—	421	—	mW
	DVB-S[2]	—	230	—	mW
Thermal resistance	2 layer PCB	—	35	—	°C/W
	4 layer PCB	—	23	—	°C/W
Power Supplies					
V_{DD_VCORE}		1.14	1.20	1.30	V
V_{DD_VANA}		3.00	3.30	3.60	V
V_{DD_VIO}		3.00	3.30	3.60	V

Notes:
1. Test conditions: 32 Mbaud, CR = 3/5, 8PSK, pilots On, parallel TS, C/N at picture failure.
2. Test conditions: 30 Mbaud, CR = 7/8, parallel TS, at QEF: BER = 2 x 10^{-4}.

Pin Assignments



Selection Guide

Part Number	Description
Si2166-D60-GM	DVB-S/S2/S2X Digital TV Demodulator, 7x7 mm QFN-48