Si3217xB
Si3291x

ProSLIC® Single-Chip FXS Solution with FXO Option

Si3217x Features

- Performs all BORSCHT functions
- Ideal for short to medium loops
- Global programmability
- Simplified configuration and diagnostics
  - Supported by ProSLIC API
- Low power standby operation
- Tracking dc-dc controller
- Patented low-power ringing
- Wideband voice support
- DTMF detection
- Pulse metering
- 3.3 V operation
- Pb-free/RoHS-compliant packaging

Si3291x Features

- Greater than 5 kV isolation
- Global programmability
- Up to +6 dBm TX/RX level
- Parallel handset detection
- Type I and II caller ID support
- Integrated ring detector
- Programmable digital hybrid

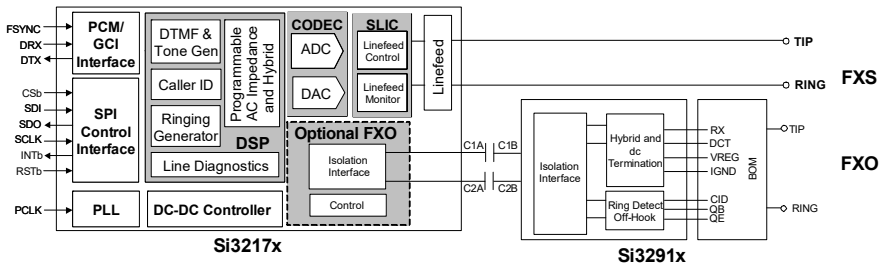
Applications

- Customer Premise Equipment (CPE)
- VoIP DSL Gateways and Routers
- Wireless Local Loop (WLL)
- Integrated Access Devices (IAD)
- Analog Terminal Adapters (ATA)
- Small Office/Home Office (SOHO) PBX

Description

The Si3217x is a family of pin-compatible single-channel ProSLIC products that implement a complete foreign exchange station (FXS) telephony interface solution in accordance with all relevant LSSGR, ITU, and ETSI specifications. Select parts in the series also implement Silicon Laboratories' patented capacitive isolation technology to enable seamless connection to Si3291x series foreign exchange office (FXO) line-side devices. The Si3217x ProSLIC ICs operate from a 3.3 V supply and interface to standard PCM/SPI digital interfaces. The Si3217x integrated dc-dc controller automatically generates the optimal battery voltages required for each line-state. Si3217x ICs are available with voltage ratings of –110 V or –135 V to support a wide range of ringing voltages. See the Ordering Guide for the voltage rating of each Si3217x version. The Si3217x is available in a 5 x 7 mm 42-pin LGA package. The Si3291x is available in a 16-pin SOIC package.

Functional Block Diagram

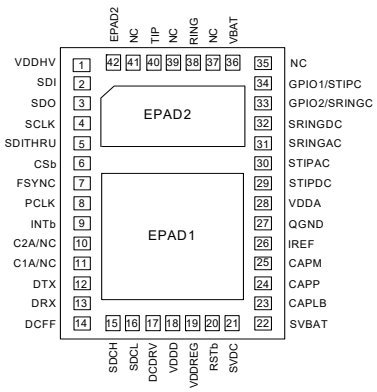


Ordering Information

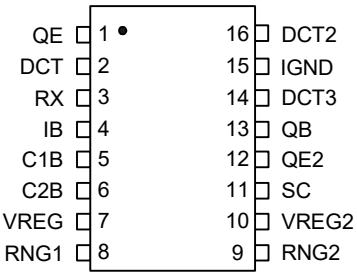
See page 38.

Pin Assignments

Si3217x



Si3291x



Patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A	F-grade	0	25	70	°C
		G-grade	–40	25	85	°C
Silicon Junction Temperature, LGA-42	T_{JHV}	Linefeed Die	—	—	145	°C
Supply Voltage, Si3217x	V_{DDD}, V_{DDA}, V_{DDHV}		3.13	3.3	3.47	V
Battery Voltage, Si32171/6/8[2]	V_{BAT}		–110	–95	–15	V
Battery Voltage, Si32170/7/9[2]	V_{BAT}		–136	–130	–15	V

Notes:
1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Operation at minimum voltage dependent upon loop conditions and dc-dc converter configuration.

Table 2. Power Supply Characteristics for Si3217x

(V_{DD} = 3.3 V, T_A = 0 to 70 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Currents: Reset	I_{DD}	V_T and V_R = Hi-Z , RST = 0	—	9.7	—	mA
	I_{VBAT}		—	0.0	—	mA
Supply Currents: High Impedance, Open	I_{DD}	V_T and V_R = Hi-Z, FXO disabled	—	13.2	—	mA
	I_{VBAT}		—	0.47	—	mA
Supply Currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V, FXO disabled, Automatic Power Save Mode enabled	—	11.2	—	mA
	I_{VBAT}		—	0.44	—	mA
Supply Currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V, FXO disabled, Automatic Power Save Mode disabled	—	27.2	—	mA
	I_{VBAT}		—	1.4	—	mA
Supply Currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V, V_R or V_T = Hi-Z, FXO disabled, Automatic Power Save Mode enabled	—	12.5	—	mA
	I_{VBAT}		—	0.4	—	mA
Supply Currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V, V_R or V_T = Hi-Z, FXO disabled, Automatic Power Save Mode disabled	—	26.3	—	mA
	I_{VBAT}		—	0.95	—	mA

Notes:
1. I_{LOOP} is the dc current in the subscriber loop during the off-hook state.
2. $I_{DD} = I_{DDD} + I_{DDA} + I_{DDC}$.
3. Refer to AN340 for power supply consumption of the recommended applications circuit, including dc-dc converter.

Table 2. Power Supply Characteristics for Si3217x (Continued)
(V_{DD} = 3.3 V, T_A = 0 to 70 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Currents: Forward/Reverse OHT, On-hook	I_{DD}	V_{TR} =48 V, FXO disabled	—	40.6	—	mA
	I_{VBAT}		—	2.3	—	mA
Supply Currents: Forward/Reverse Active, Off-hook	I_{DD}	I_{LOOP} = 20 mA R_{LOAD} = 200 Ω, FXO disabled	—	44.2	—	mA
	I_{VBAT}		—	22.0	—	mA
Supply Currents: Ringing	I_{DD}	V_{TR} =55V_{RMS} + 0 VDC, balanced, FXO disabled	—	28	—	mA
	I_{VBAT}	sinusoidal, f = 20 Hz, R_{LOAD} = 5 REN = 1400 Ω	—	38.2	—	mA
System Side FXO Supply Current	I_{DD}	FXO enabled	—	10.0	—	mA
System Side FXO Supply Current	I_{DD}	FXO enabled, FXO in Sleep Mode	—	6.3	—	mA
System Side FXO Supply Current	I_{DD}	FXO enabled, FXO in Full Power Down Mode	—	0.1	—	mA
System Side FXO Supply Current	I_{DD}	FXO disabled	—	—	0	mA

Notes:
1. I_{LOOP} is the dc current in the subscriber loop during the off-hook state.
2. $I_{DD} = I_{DDD} + I_{DDA} + I_{DDC}$.
3. Refer to AN340 for power supply consumption of the recommended applications circuit, including dc-dc converter.

Table 3. AC Characteristics for FXS
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Level		2.5	—	—	V_{PK}
Overload Compression	2-Wire – PCM	Figure 15	—	—	

Notes:
1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DDD}, V_{DDA}, V_{DDHV} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
6. 0 dBm 0 is equal to 0 dBm into 600 Ω.

Table 3. AC Characteristics for FXS (Continued)
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
Single Frequency Distortion[1]	2-Wire – PCM or PCM – 2-Wire: 200 Hz to 3.4 kHz	+35	40	—	dB
	PCM – 2-Wire – PCM: 200 Hz – 3.4 kHz, 16-bit Linear mode	—	—	–63	dB
Signal-to-(Noise + Distortion) Ratio[2]	200 Hz to 3.4 kHz D/A or A/D 8-bit Active off-hook, and OHT, any Z_T	Figure 14	—	—	
Audio Tone Generator Signal-to-Distortion Ratio[2]	0 dBm0, Active off-hook, and OHT, any Z_T	46	—	—	dB
Intermodulation Distortion		—	—	–41	dB
Gain Accuracy[2]	2-Wire to PCM or PCM to 2-Wire 1014 Hz, Any gain setting	–0.2	—	0.2	dB
Attenuation Distortion vs. Frequency	0 dBm 0[6]	See Figure 16 and 17			
Group Delay vs. Frequency		See Figure 18 and 19			
Gain Tracking[3]	1014 Hz sine wave, reference level –10 dBm Signal level:	—	—	—	—
	3 dB to –37 dB	—	—	0.25	dB
	–37 dB to –50 dB	—	—	0.5	dB
	–50 dB to –60 dB	—	—	1.0	dB
Round-Trip Group Delay	1014 Hz, Within same time-slot	—	450	500	µs
2-Wire Return Loss[4]	200 Hz to 3.4 kHz	26	30	—	dB
Transhybrid Balance[4]	300 Hz to 3.4 kHz	26	30	—	dB

Notes:
1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DDD}, V_{DDA}, V_{DDHV} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
6. 0 dBm 0 is equal to 0 dBm into 600 Ω.

Table 3. AC Characteristics for FXS (Continued)
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Test Condition	Min	Typ	Max	Unit
Noise Performance					
Idle Channel Noise[5]	C-Message weighted	—	8	12	dBrnC
	Psophometric weighted	—	–82	–78	dBmP
PSRR from V_{DDD}, V_{DDA}, V_{DDHV} @ 3.3 V	RX and TX, 200 Hz to 3.4 kHz	—	55	—	dB
Longitudinal Performance					
Longitudinal to Metallic/PCM Balance (forward or reverse)	200 Hz to 1 kHz	58	60	—	dB
	1 kHz to 3.4 kHz	53	58	—	dB
Metallic/PCM to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING	—	50	—	Ω
Longitudinal Current Capability	Active off-hook 60 Hz Reg 73 = 0x0B	—	25	—	mA

Notes:
1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} - V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DDD}, V_{DDA}, V_{DDHV} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.
6. 0 dBm 0 is equal to 0 dBm into 600 Ω.

Table 4. Linefeed Characteristics for FXS
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Loop Resistance	R_{LOOP}	$R_{DC,MAX}$ = 430 Ω I_{LOOP} = 18 mA, V_{BAT} = –52 V, R_{PROT} = 0 Ω	—	—	2000	Ω
DC Feed Current		Differential	—	—	45	mA
		Common Mode	—	—	30	mA
		Differential + Common Mode	—	—	45	mA
DC Loop Current Accuracy		I_{LIM} = 18 mA	—	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	—	—	4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	160	—	640	Ω
DC On-Hook Voltage Accuracy—Ground Start	V_{OHTO}	$I_{RING}<I_{LIM}$; V_{RING} wrt ground, V_{RING} = –51 V	—	—	4	V
DC Output Resistance—Ground Start	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	160	—	640	Ω
DC Output Resistance—Ground Start	R_{TOTO}	TIP to ground	400	—	—	kΩ
Loop Closure Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ground Key Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ring Trip Threshold Accuracy		AC detection, V_{RING} = 70 Vpk, no offset, I_{TH} = 80mA	—	—	4	mA
		DC detection, 20 V dc offset, I_{TH} = 13 mA	—	—	1	mA
		DC Detection, 48 V DC offset, R_{loop} = 1500 Ω	—	—	3	mA
Ringing Amplitude*	$V_{RINGING}$	Si32171/6/8 Open circuit, V_{BAT} = –110 V	108	—	—	V_{PK}
		Si32170/7/9 Open circuit, V_{BAT} = –136 V	132	—	—	V_{PK}
Sinusoidal Ringing Total Harmonic Distortion	R_{THD}	Si32171/6/8 : 60 V_{RMS}, 15 V_{OFFSET}, 0–5 REN	—	1	—	%
		Si32170/7/9 : 55 V_{RMS}, 48 V_{OFFSET}, 0–5 REN				
Ringing Frequency Accuracy		f = 16 Hz to 60 Hz	—	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF times	—	—	50	ms
Loop Voltage Sense Accuracy		$V_{TIP} – V_{RING}$ = 48 V	—	2	4	%

Table 4. Linefeed Characteristics for FXS (Continued)
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Loop Current Sense Accuracy		I_{LOOP} = 18 mA	—	7	10	%
Power Alarm Threshold Accuracy		Power Threshold = 1.0 W V_{BAT} = –56 V, I_{LDDD} = 40 mA, R_{LOAD} = 600 Ω	—	15	—	%
Test Load Impedance	R_{TEST}	HVIC_STATE_SPARE[23] = 1; $\lvert V_{T/R} \rvert \leq 50$ V	3.6	5.3	7.7	kΩ
Test Load Voltage	V_{TL}	HVIC_STATE_SPARE[23] = 1	±5		±50	V
***Note:** Ringing amplitude is set for 108 or 128 V peak and measured at TIP-RING using no series protection resistance.						

Table 5. Monitor ADC Characteristics for FXS
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity	DNLE		—	1	—	LSB
Integral Nonlinearity (8-bit resolution)	INLE		—	1	—	LSB
Gain Error			—	5	—	%

Table 6. Loop Characteristics for FXO
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0 DCV = 00, MINI = 11, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0 DCV = 11, MINI = 00, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ILIM = 1 DCV = 11, MINI = 00, DCR = 0	—	—	40	V
On-Hook Leakage Current	I_{LK}	V_{TR} = –48 V	—	—	5	µA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 0	10	—	120	mA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 1	10	—	60	mA
***Note:** The ring signal will not be detected below the minimum. The ring signal will be detected above the maximum.						

Table 6. Loop Characteristics for FXO (Continued)

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Ring Current		dc current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage*	V_{RD}	RT2 = 0, RT = 0	13.5	15	16.5	V_{rms}
Ring Detect Voltage*	V_{RD}	RT2 = 0, RT = 1	19.35	21.5	23.65	V_{rms}
Ring Detect Voltage*	V_{RD}	RT2 = 1, RT = 1	40.5	45	49.5	V_{rms}
Ring Frequency	F_R		13	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal will not be detected below the minimum. The ring signal will be detected above the maximum.

Table 7. AC Characteristics for FXO

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, Fs = 8000 Hz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1	—	200	—	Hz
Transmit Full-Scale Level[1]	V_{FS}	FULL = 0 (0 dBm)	—	1.1	—	V_{PEAK}
		FULL = 1 (+3.2 dBm)[Note 2]	—	1.58	—	V_{PEAK}
		FULL2 = 1 (+6.0 dBm)[Note 2]	—	2.16	—	V_{PEAK}
Receive Full-Scale Level[1,3]	V_{FS}	FULL = 0 (0 dBm)	—	1.1	—	V_{PEAK}
		FULL = 1 (+3.2 dBm)[Note 2]	—	1.58	—	V_{PEAK}
		FULL2 = 1 (+6.0 dBm)[Note 2]	—	2.16	—	V_{PEAK}
Dynamic Range[4,5,6]	DR	ILIM = 0, DCV = 11, MINI=00 DCR = 0, I_L = 100 mA	—	80	—	dB
Dynamic Range[4,5,6]	DR	ILIM = 0, DCV = 00, MINI=11 DCR = 0, I_L = 20 mA	—	80	—	dB
Dynamic Range[4,5,6]	DR	ILIM = 1, DCV = 11, MINI=00 DCR = 0, I_L = 50 mA	—	80	—	dB

Notes:

1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1 on page 12.
2. With FULL = 1, the transmit and receive full-scale level of +3.2 dBm can be achieved with a 600 Ω ac termination. While the transmit and receive level in dBm varies with reference impedance, the DAA will transmit and receive 1 dBV into all reference impedances. With FULL2 = 1, the transmit and receive full-scale level of +6.0 dBm can be achieved with a 600 Ω termination. In this mode, the DAA will transmit and receive +1.5 dBV into all reference impedances.
3. Receive full-scale level produces –0.9 dBFS at DTX.
4. DR = 20 x log (RMS V_{FS}/RMS Vin) + 20 x log (RMS V_{in}/RMS noise). The RMS noise measurement excludes harmonics. Here, V_{FS} is the 0 dBm full-scale level per Note 1 above.
5. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
6. Vin = 1 kHz, –3 dBFS.
7. THD = 20 x log (RMS distortion/RMS signal).
8. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log (RMS V_{IN}/RMS noise). V_{CID} is the 1.5 V full-scale level with the enhanced caller ID circuit. With the typical CID circuit, the V_{CID} full-scale level is 6 V peak, and the DR_{CID} decreases to 50 dB.
9. Refer to Tables 8–9 for relative gain accuracy characteristics (passband ripple).
10. Analog hybrid only. Z_{ACIM} controlled by ACIM in Register 30.

Table 7. AC Characteristics for FXO (Continued)
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, Fs = 8000 Hz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Total Harmonic Distortion[6,7]	THD	ILIM = 0, DCV = 11, MINI=00 DCR = 0, I_L = 100 mA	—	–72	—	dB
Transmit Total Harmonic Distortion[6,7]	THD	ILIM = 0, DCV = 00, MINI=11 DCR = 0, I_L = 20 mA	—	–78	—	dB
Receive Total Harmonic Distortion[6,7]	THD	ILIM = 0, DCV = 00, MINI=11 DCR = 0, I_L = 20 mA	—	–78	—	dB
Receive Total Harmonic Distortion[6,7]	THD	ILIM = 1,DCV = 11, MINI=00 DCR = 0, I_L = 50 mA	—	–78	—	dB
Dynamic Range (Caller ID mode)[8]	DR_{CID}	VIN = 1 kHz, –13 dBFS	—	62	—	dB
Caller ID Full-Scale Level[8]	V_{CID}		—	1.5	—	V_{PEAK}
Gain Accuracy[6,9]		2-W to DTX, TXG2, RXG2, TXG3, and RXG3 = 0000	–0.5	0	0.5	dB
Transhybrid Balance[10]		300–3.4 kHz, Z_{ACIM} = Z_{LINE}	20	—	—	dB
Transhybrid Balance[10]		1 kHz, Z_{ACIM} = Z_{LINE}	—	30	—	dB
Two-Wire Return Loss		300–3.4 kHz, all ac terminations	25	—	—	dB
Two-Wire Return Loss		1 kHz, all ac terminations	—	32	—	dB

Notes:
1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1 on page 12.
2. With FULL = 1, the transmit and receive full-scale level of +3.2 dBm can be achieved with a 600 Ω ac termination. While the transmit and receive level in dBm varies with reference impedance, the DAA will transmit and receive 1 dBV into all reference impedances. With FULL2 = 1, the transmit and receive full-scale level of +6.0 dBm can be achieved with a 600 Ω termination. In this mode, the DAA will transmit and receive +1.5 dBV into all reference impedances.
3. Receive full-scale level produces –0.9 dBFS at DTX.
4. DR = 20 x log (RMS V_{FS}/RMS Vin) + 20 x log (RMS V_{in}/RMS noise). The RMS noise measurement excludes harmonics. Here, V_{FS} is the 0 dBm full-scale level per Note 1 above.
5. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
6. Vin = 1 kHz, –3 dBFS.
7. THD = 20 x log (RMS distortion/RMS signal).
8. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log (RMS V_{IN}/RMS noise). V_{CID} is the 1.5 V full-scale level with the enhanced caller ID circuit. With the typical CID circuit, the V_{CID} full-scale level is 6 V peak, and the DR_{CID} decreases to 50 dB.
9. Refer to Tables 8–9 for relative gain accuracy characteristics (passband ripple).
10. Analog hybrid only. Z_{ACIM} controlled by ACIM in Register 30.

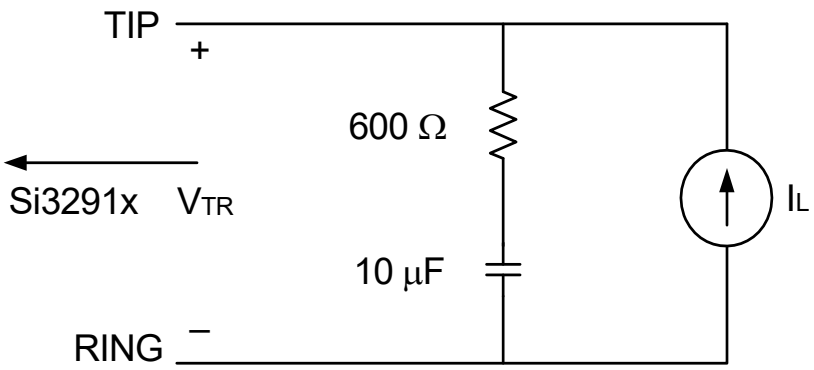


Figure 1. Test Circuit for Loop Characteristics

Table 8. Digital FIR Filter Characteristics for FXO—Transmit and Receive
(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	s
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 2, 3, 4, and 5.					

Table 9. Digital IIR Filter Characteristics for FXO—Transmit and Receive
(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	s
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 6, 7, 8, and 9. Figures 10 and 11 show group delay versus input frequency.					

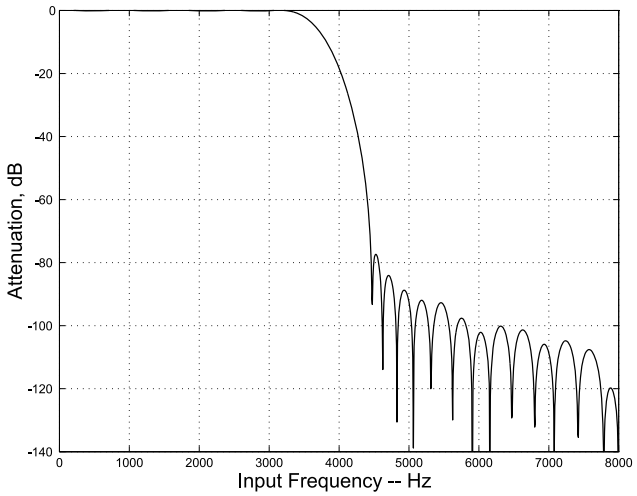


Figure 2. FIR Receive Filter Response

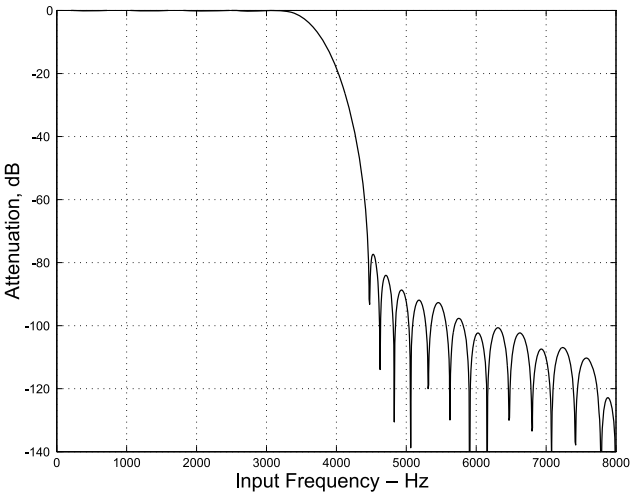


Figure 4. FIR Transmit Filter Response

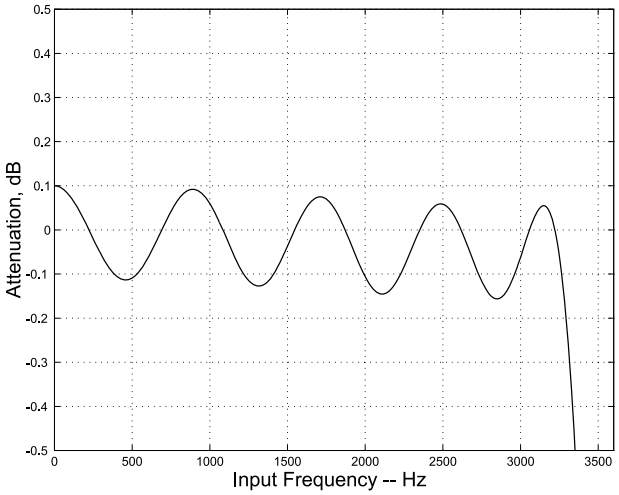


Figure 3. FIR Receive Filter Passband Ripple

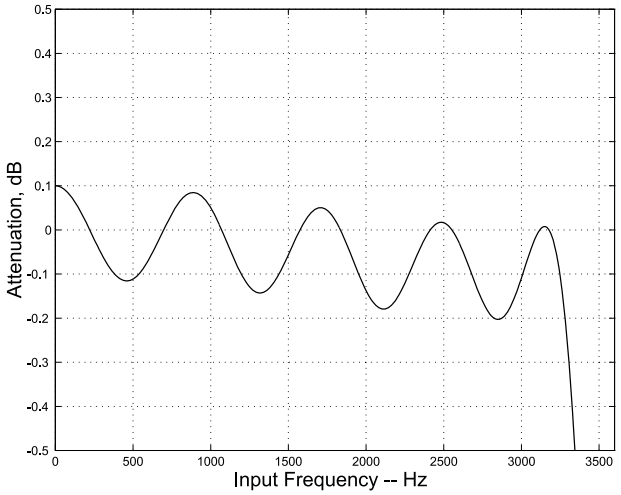


Figure 5. FIR Transmit Filter Passband Ripple

For Figures 1–5, all filter plots apply to a sample rate of Fs = 8 kHz.

For Figures 6–9, all filter plots apply to a sample rate of Fs = 8 kHz.

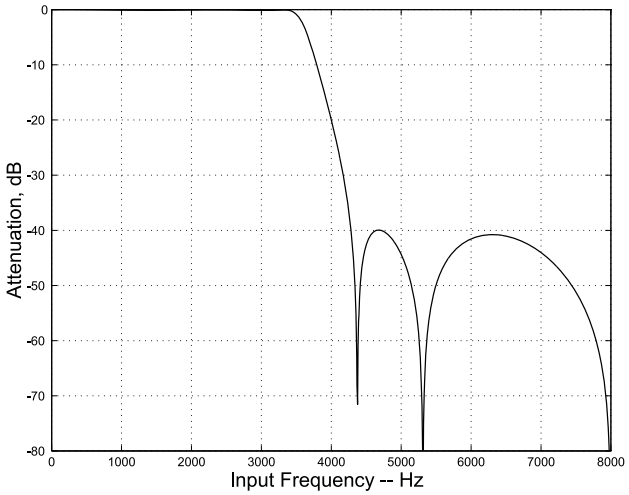


Figure 6. IIR Receive Filter Response

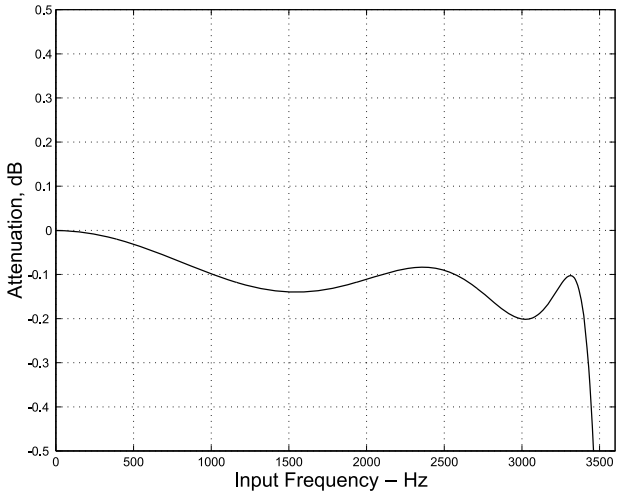


Figure 9. IIR Transmit Filter Passband Ripple

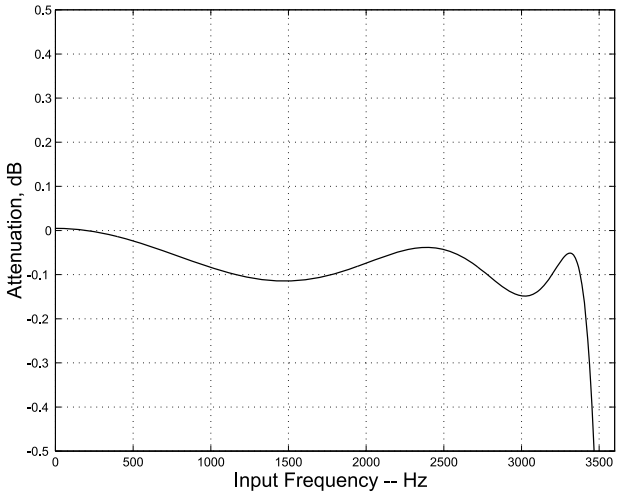


Figure 7. IIR Receive Filter Passband Ripple

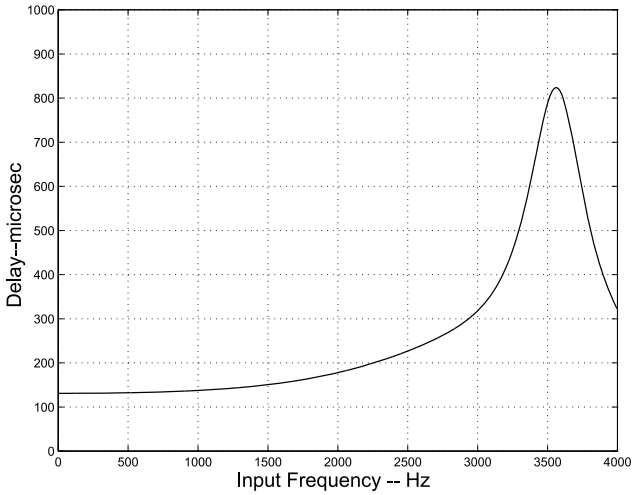


Figure 10. IIR Receive Group Delay

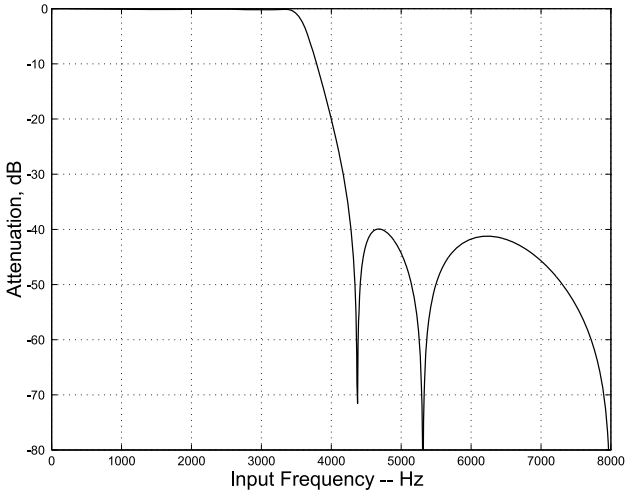


Figure 8. IIR Transmit Filter Response

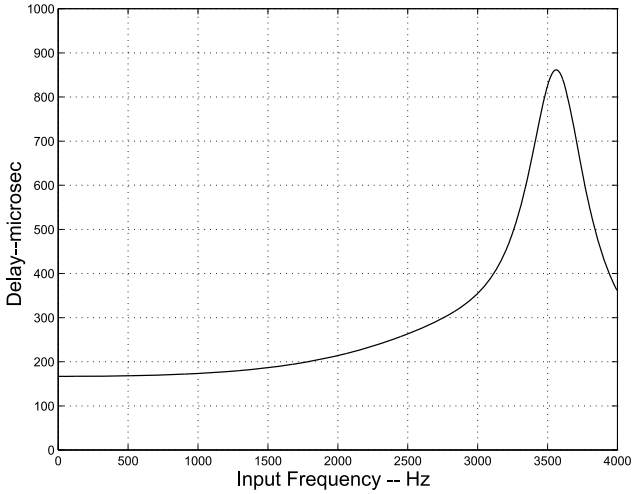


Figure 11. IIR Transmit Group Delay

Table 10. Digital I/O Characteristics
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DD}	—	V_{DD}	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DD}	V
High Level Output Voltage*	V_{OH}	DTX, SDO, SDITHRU, GPIO1/STIPC, GPIO2/SRINGC: I_O = –4 mA	V_{DD} – 0.6	—	—	V
		C1A, C2A: I_O = –2 mA				
Low Level Output Voltage*	V_{OL}	DTX, SDO, INTb, SDITHRU, GPIO1/STIPC, GPIO2/SRINGC: I_O = 4 mA	—	—	0.4	V
		C1A, C2A: I_O = 2 mA				
SDITHRU and RSTb Internal Pullup Current			33	42	65	µA
Input Leakage Current	I_L		—	—	10	µA

***Note:** V_{IH}/V_{IL}, V_{OH}/V_{OL} do not apply to C1A/C2A.

Table 11. Switching Characteristics—General Inputs[1]
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, RSTb	t_r	—	—	5	ns
RSTb Pulse Width, SPI Daisy Chain Mode[3]	t_{rl}	33/PCLK	—	—	µs

Notes:
1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DD} – 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. The minimum RSTb pulse width assumes the SDITHRU pin is tied to ground via a pulldown resistor no greater than 10 kΩ per device.
3. The minimum RSTb pulse width is 33/PCLK frequency (i.e., 33/8.192 MHz = 4 µs).

Table 12. Switching Characteristics—SPI
(V_{DDA} = 3.13 to 3.47 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		62	—	—	ns
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, CSb Rise to SDO Tri-state	t_{d3}		—	—	20	ns
Setup Time, CSb to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, CSb to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Chip Selects	t_{cs}		220	—	—	ns
SDI to SDITHRU Propagation Delay	t_{d4}		—	4	10	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_{DDD} - 0.4$ V, V_{IL} = 0.4 V						

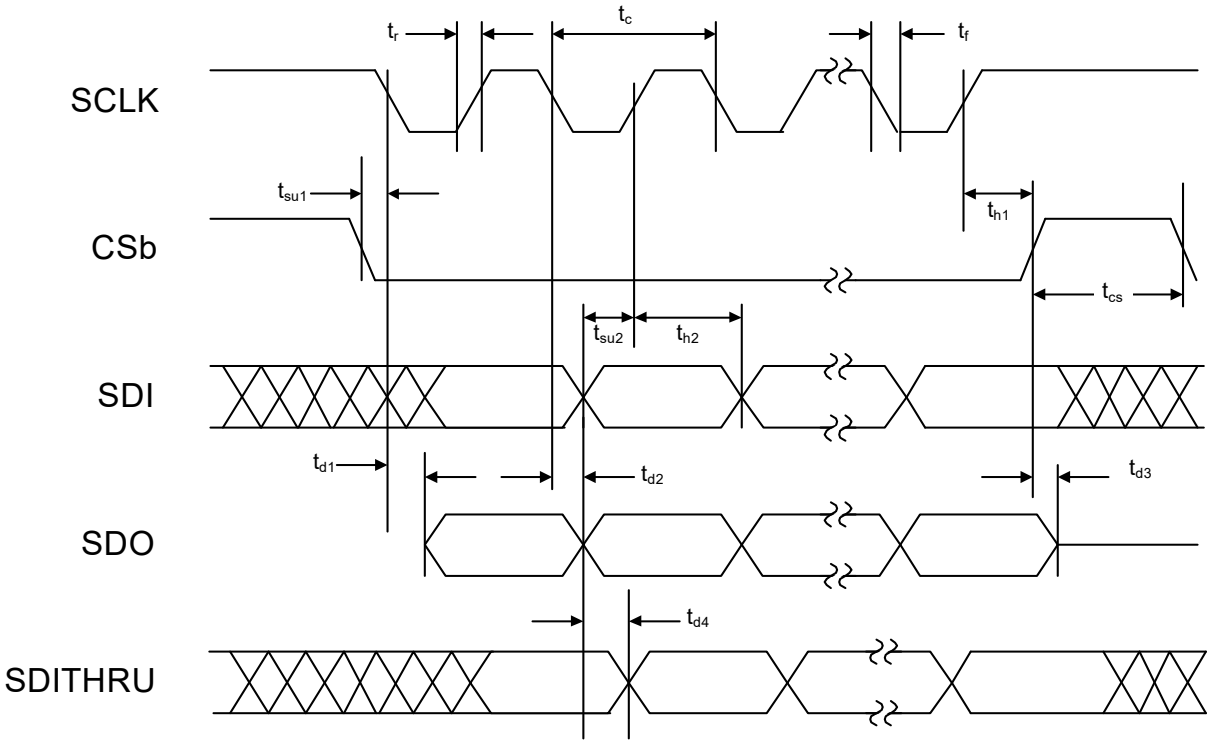


Figure 12. SPI Timing Diagram

Table 13. Switching Characteristics—PCM Highway Interface
(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min[1]	Typ[1]	Max[1]	Units
PCLK Period (–40 to +85 °C)	$t_{p(industrial)}$		122	—	1953	ns
PCLK Period (0 to +70 °C)	$t_{p(commercial)}$		122	—	3906	ns
PCLK Jitter Tolerance for FXS	$t_{jitter(FXS)}$		—	—	8	ns_{RMS}
PCLK Jitter Tolerance for FXO	$t_{jitter(FXO)}$		—	—	2	ns
Valid PCLK Inputs[2]			— — — — — — — —	512 768 1.024 1.536 1.544 2.048 4.096 8.192	— — — — — — — —	kHz kHz MHz MHz MHz MHz MHz MHz
FSYNC Period[3]	t_{fs}		—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
FSYNC Jitter Tolerance[4]	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tri-state[5]	t_{d3}		—	—	20	ns
Setup Time, FSYNC to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, FSYNC to PCLK Fall	t_{h1}		20	—	—	ns
Setup Time, DRX to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, DRX to PCLK Fall	t_{h2}		20	—	—	ns
FSYNC Pulse Width	t_{wfs}		t_p	—	125 µs–t_p	

Notes:
1. All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} – $V_{I/O}$ – 0.4 V, V_{IL} = 0.4 V.
2. A constant PCLK and FSYNC are required.
3. FSYNC source is assumed to be 8 kHz under all operating conditions.
4. FSYNC Jitter Tolerance relative to PCLK.
5. Specification applies to PCLK fall to DTX tristate when that mode is selected.

Table 14. Absolute Maximum Ratings and Thermal Information[1]

Parameter	Symbol	Test Condition	Value	Unit
Storage Temperature Range	T_{STG}		–55 to 150	°C
Thermal Resistance, Typical[2] LGA-42	θ_{JA}		53	°C/W
	θ_{JB}		33	
	θ_{JC}		39	
Continuous Power Dissipation[3,4] LGA-42	P_D	T_A = 85 °C	0.75	W
Maximum Junction Temperature, LGA-42 (Linefeed Die)	T_{JHV}	Continuous	145	°C
Maximum Junction Temperature LGA-42 (Low Voltage Die)	T_{JLV}		125	°C
Thermal Resistance, Typical[2] SOIC-16	θ_{JA}		85	°C/W
Continuous Power Dissipation[3] SOIC-16	P_D	T_A = 85 °C	0.47	W
Maximum Junction Temperature SOIC-16	T_J		125	°C
Si3217x				
Supply Voltage	V_{DDD}, V_{DDA}, V_{DDHV}		–0.5 to 4.0	V
Digital Input Voltage	V_{IND}		–0.3 to 3.6	V
Battery Supply Voltage[5], Si32171/6/8	V_{BAT}		+0.4 to –115	V
Battery Supply Voltage[5], Si32170/7/9	V_{BAT}		+0.4 to –140	V
Tip or Ring Voltage, Si32171/6/8[6]	V_{TIP}, V_{RING}		–130	V
Tip or Ring Voltage, Si32170/7/9[6]	V_{TIP}, V_{RING}		–140	V
TIP, RING Current	I_{TIP}, I_{RING}		±100	mA

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.
2. The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed correctly. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane.
3. Operation of the Si3217x or Si3291x above 125 °C junction temperature may degrade device reliability.
4. Si3217x linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold. The thermal shutdown threshold should normally be set to 145 °C; when in the ringing state with cadence the thermal shutdown may be set to 200 °C. For optimal reliability long term operation of the Si3217x linefeed above 150 °C junction temperature should be avoided.
5. The dv/dt of the voltage applied to the VBAT pins must be limited to 10 V/µs.
6. Specification requires circuit for surge event as shown in typical application circuit.

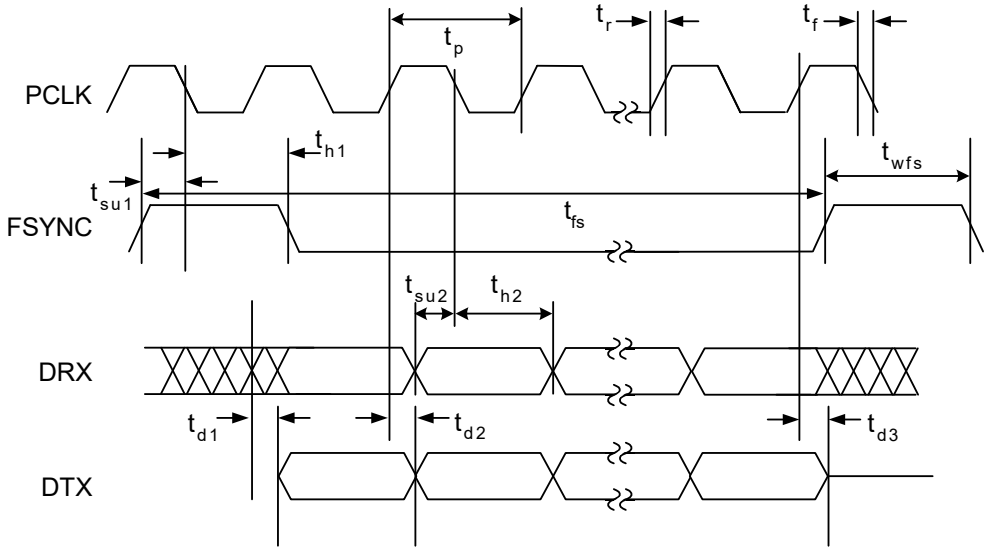


Figure 13. PCM Highway Interface Timing Diagram

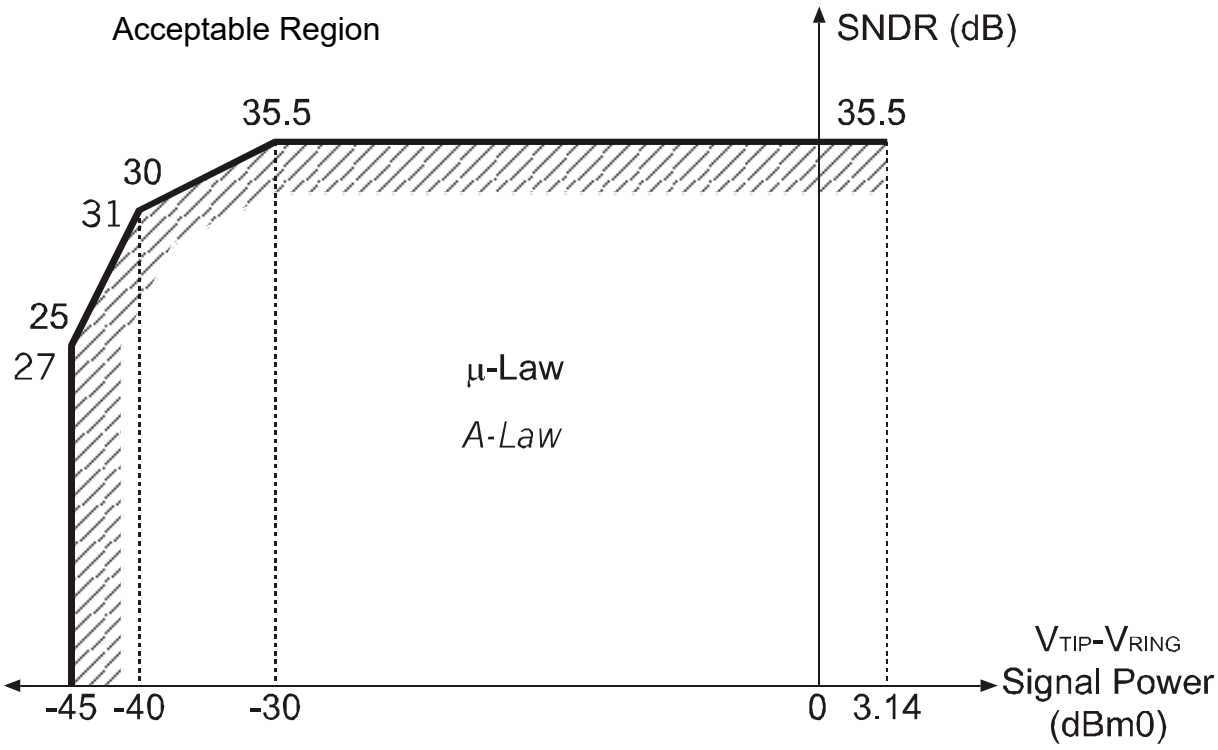


Figure 14. Transmit and Receive Path SNDR

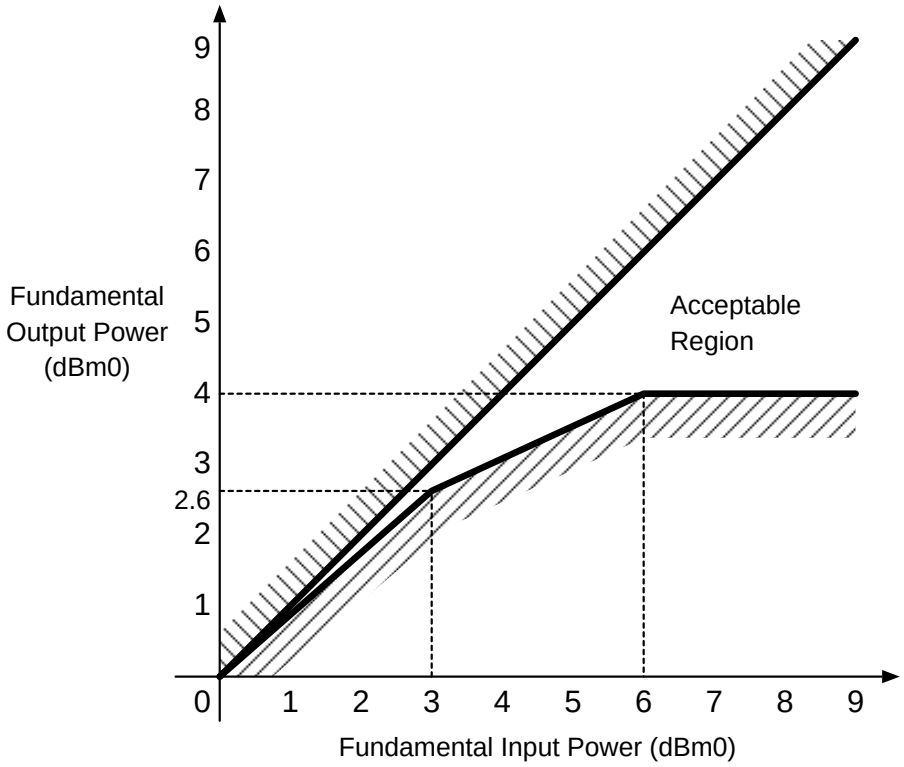


Figure 15. Overload Compression Performance

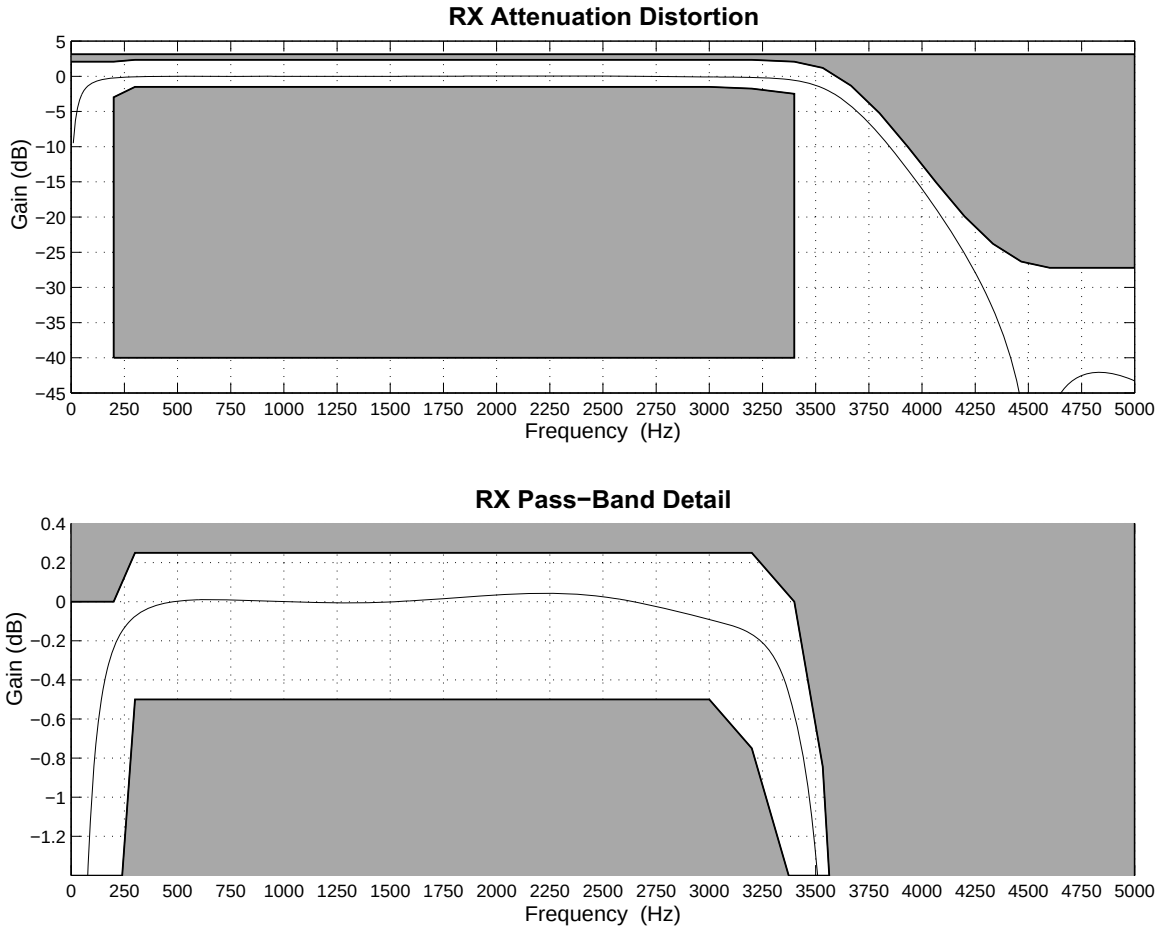


Figure 16. Receive Path Frequency Response

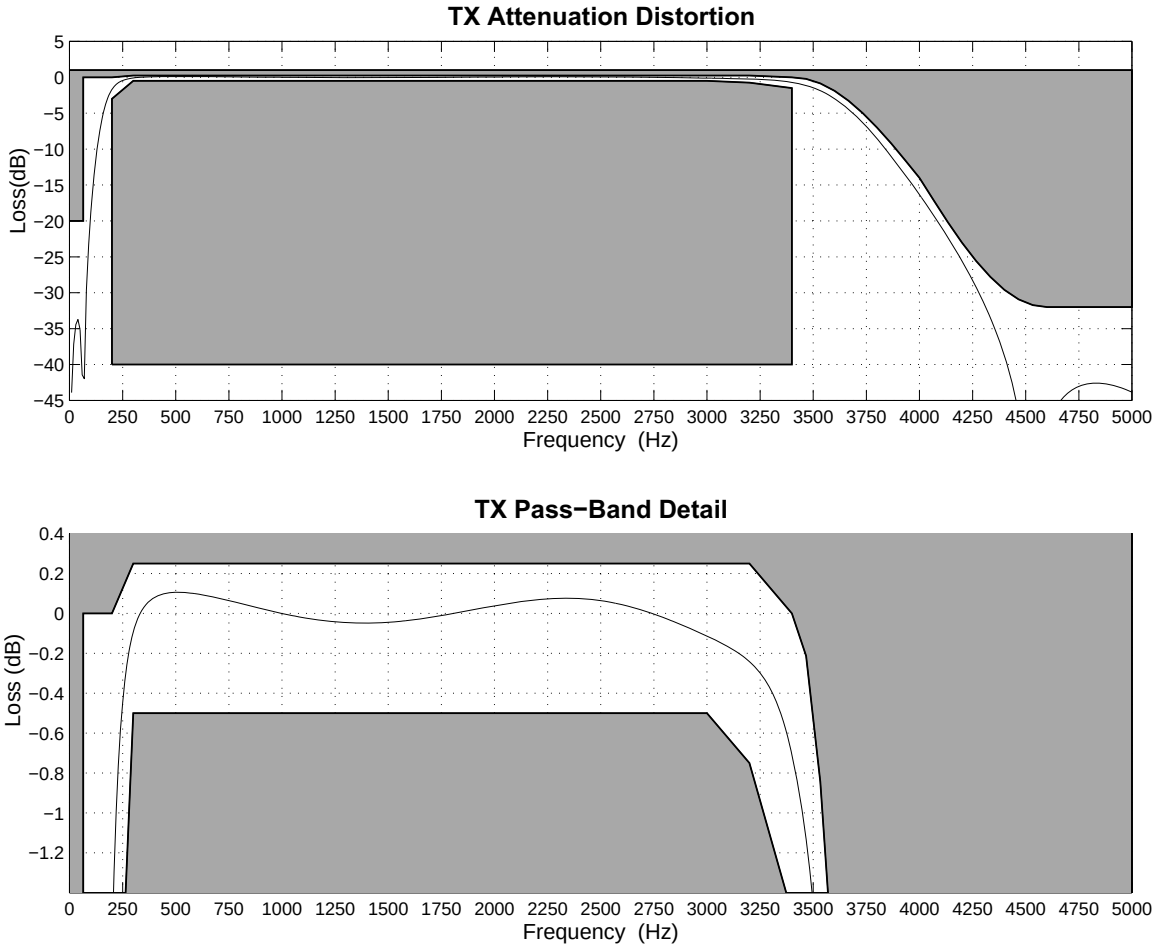


Figure 17. Transmit Path Frequency Response

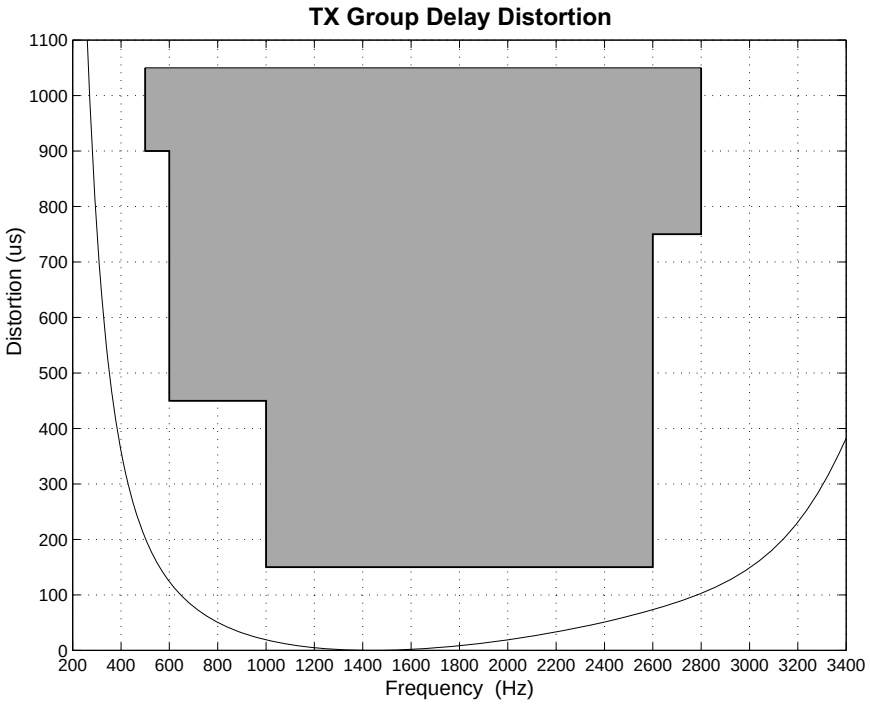


Figure 18. Transmit Group Delay Distortion

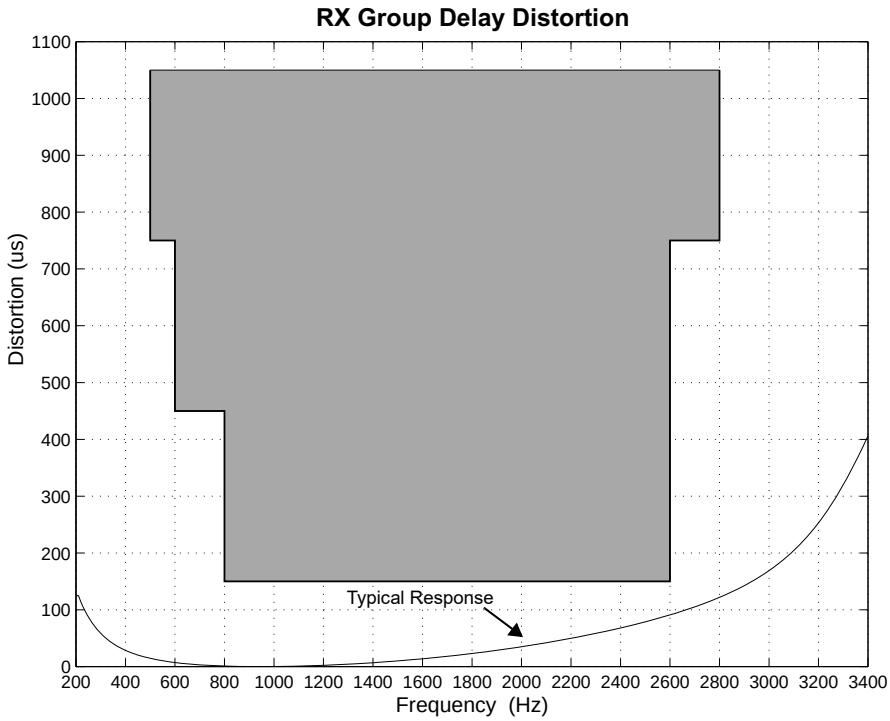


Figure 19. Receive Group Delay Distortion

2. Overview

The Si3217x series provides all SLIC, codec, DTMF detection, and signal generation functions needed for one complete analog telephone interface. The Si3217x performs all battery, over-voltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions; it also supports extensive metallic loop testing capabilities.

The Si3217x provides a standard voice-band (200 Hz–3.4 kHz) audio codec and, optionally, an audio codec with both wideband (50 Hz–7 kHz) and standard voice-band modes. The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality while the standard voice-band mode provides standard telephony audio bandwidth. The Si3217x incorporates a programmable dc-dc converter controller that reacts to line conditions to provide the optimal battery voltage required for each line-state. Si3217x ICs are available with voltage ratings of –110 V or –135 V to support a wide range of ringing voltages; see "8. Ordering Guide," on page 38 for the voltage rating of each Si3217x version.

Programmable on-hook voltage, programmable off-hook loop current, reverse battery operation, loop or ground start operation, and on-hook transmission are supported. Loop current and voltage are continuously monitored by an integrated monitoring ADC.

The Si3217x supports balanced 5 REN ringing with or without a programmable dc offset. The available voltage offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements.

Select part numbers in the series also implement Silicon Laboratories' capacitive isolation technology to enable a seamless connection to Si3291x DAA ICs. Digital voice data transfer occurs over a standard PCM bus. Control data is transferred using a standard SPI. Si3217x ICs are available in a 42-pin LGA package. The Si3291x devices are available in a 16-pin SOIC.

3. FXS Features

3.1. DC Feed Characteristics

ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics.

When in the active state, the ProSLIC operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in Figure 20. The constant-voltage region has a low resistance, typically 160 Ω. The constant-current region approximates infinite resistance.

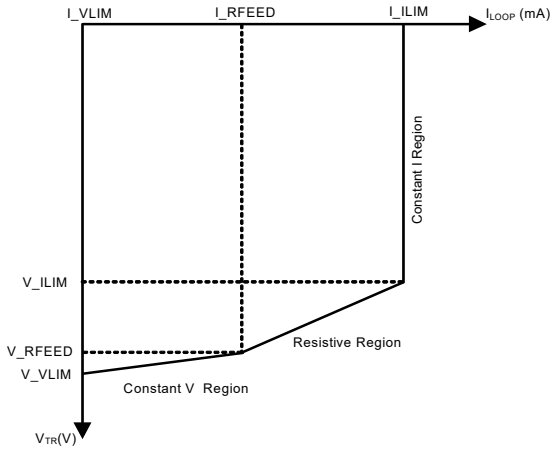


Figure 20. ProSLIC DC Feed Characteristics

3.2. Linefeed Operating States

The linefeed interface includes eight different register-programmable operating states as listed in Table 15. The Open state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

3.3. Line Voltage and Current Monitoring

The ProSLIC continuously monitors the TIP, RING, and battery voltages and currents via an on-chip ADC and stores the resulting values in individual RAM locations. Additionally, the loop voltage (V_{TIP}–V_{RING}), loop current, and longitudinal current values are calculated based on the TIP and RING measurements and are stored in unique register locations for further processing. The ADC updates all registers at a rate of 2 kHz or greater.

3.4. Power Monitoring and Power Fault Detection

The Si3217x line monitoring functions are used to continuously protect against excessive power conditions. The Si3217x contains an on-chip, analog sensing diode that provides real-time temperature data and turns off the device when a preset threshold is exceeded.

If the Si3217x detects a fault condition or overpower condition, it automatically sets that device to the open state and generates a "power alarm" interrupt.

The interrupt can be masked, but masking the automatic transition to open is not recommended since it is used to protect the Si3217 HVIC under excessive power conditions.

The various power alarms and linefeed faults supporting automatic intervention are described below.

1. Total power exceeded.
2. Excessive foreign current or voltage on TIP and/or RING.
3. Thermal shutdown event.

3.5. Thermal Overload Shutdown

If the die temperature exceeds the maximum junction temperature threshold, TJmax, of 145 °C or 200 °C, the device has the ability to shut itself down to a low-power state without user intervention. The thermal shutdown circuit contains a sufficient amount of hysteresis and/or turn-on delay time so as to remain shut down during a power cross event, where 50 Hz or 60 Hz, 600 V, is connected to TIP and/or RING.

Table 15. Linefeed Operating States

Linefeed State	Description
Open	Output is high-impedance, and all line supervision functions are powered down. Audio is powered down. This is the default state after powerup or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in line diagnostics mode as a high impedance state during linefeed testing. A power fault condition may also force the device into the open state.
Forward Active Reverse Active	Linefeed circuitry and audio are active. In Forward Active state, the TIP lead is more positive than the RING lead; in Reverse Active state, the RING lead is more positive than the TIP lead. Loop closure and ground key detect circuitry are active.
Forward OHT Reverse OHT	Provides data transmission during an on-hook loop condition (e.g., transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the TIP lead is more positive than the RING lead; in Reverse OHT state, the RING lead is more positive than the TIP lead.
TIP Open	Provides an active linefeed on the RING lead and sets the TIP lead to high impedance (>400 kΩ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.
RING Open	Provides an active linefeed on the TIP lead and sets the RING lead to high impedance (>400 kΩ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.
Ringing	Drives programmable ringing signal onto TIP and RING leads with or without dc offset.
Line Diagnostics	The channel is put into diagnostic mode. In this mode, the channel has special diagnostic resources available.

3.6. Loop Closure Detection

The Si3217x provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two unique thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status, and a maskable interrupt bit is also provided.

3.7. Ground Key Detection

The Si3217x provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two unique thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status, and a maskable interrupt bit is also provided.

3.8. Ringing Generation

The Si3217x provides the ability to generate a programmable sinusoidal or trapezoidal ringing waveform, with or without dc offset. The ringing frequency, wave shape, cadence, and offset are all register-programmable. Three ringing modes are supported: balanced, unbalanced, and low-power ringing (LPR). Figure 21 illustrates the fundamental differences between the three ringing modes.

3.9. Polarity Reversal

The Si3217x supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

3.10. Two-Wire Impedance Synthesis

The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Si3217x to the reference impedance. Most real or complex two-wire impedances can be generated with appropriate register coefficients.

3.11. Transhybrid Balance Filter

The trans-hybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path.

3.12. Tone Generators

The Si3217x includes two digital tone generators that allow a wide variety of single- or dual-tone frequency and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.

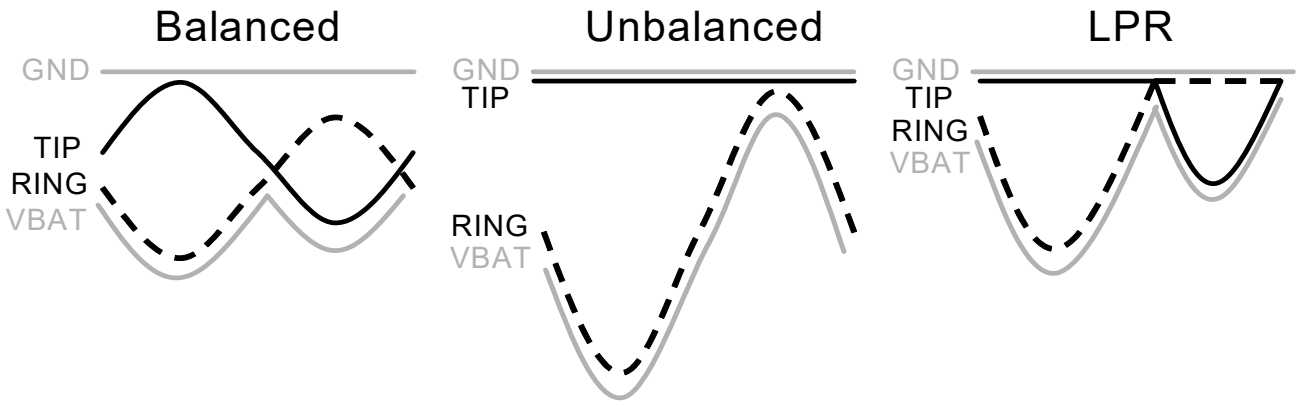


Figure 21. Ringing Modes

3.13. DTMF Detection

In DTMF, two tones generate a DTMF digit. One tone is chosen from four possible row tones, and one tone is chosen from four possible column tones. The sum of these tones constitutes one of 16 possible DTMF digits. Select Si3217x ICs support DTMF detection as outlined in "8. Ordering Guide," on page 38. The DTMF detector can be utilized by the FXS or FXO interface.

3.14. Pulse Metering (Si32170/1 Only)

The pulse metering system for the Si32170/1 is designed to inject a 12 or 16 kHz billing tone into the audio path with maximum amplitude of 2.5 V_{RMS} at TIP and RING into a 200 Ω ac load impedance. The tone is generated in the DSP via a table lookup that guarantees spectral purity by not allowing drift. The tone will ramp up until it reaches a host-programmed threshold, at which point it will maintain that level until instructed to ramp down, thus creating a trapezoidal envelope.

The amplitude is controlled by an automatic gain control circuit (AGC). While the tone is ramping up, the AGC takes the feedback audio and applies it to a band pass filter, which is programmed for the 12 or 16 kHz frequency of interest. When the peak is detected, the ramp is stopped.

See AN340 section 2.3.9 for additional details and considerations on Pulse Metering.

3.15. DC-DC Controller

The Si3217x integrates a dc-dc controller that operates from a single positive dc input. The controller dynamically manages an external dc-dc converter circuit to generate the optimal battery voltage for each operating state.

3.16. Wideband Audio

Select Si3217x ICs support a software-selectable wideband (50 Hz–7 kHz) and narrowband (200 Hz–3.4 kHz) audio codec. The wideband mode provides an expanded audio band at a 16-bit, 16 kHz sample rate for enhanced audio quality while maintaining standard telephony audio compatibility. Wideband audio samples are transmitted and received on the PCM interface using two consecutive 8 kHz frames.

3.17. In-Circuit and Metallic Loop Testing (MLT)

A rich set of features is provided for in-circuit testing of the FXS system and the connected telephone line (MLT):

- Tone generators
- Audio diagnostic filters
- Digital and analog loop-back modes
- Internal test load
- Monitor ADC
- DSP algorithms

Using these facilities, it is possible to test the Si3217x's dc-dc converter, codec, line-feed, PCM bus interface, DSP, SPI bus interface, and call progress state-machine as well as testing the connected telephone line and external protection circuitry.

The audio diagnostic filters on the FXS are intended to provide programmable filtering of the TX digital audio signal and calculate the peak and/or average signal power of the filters' outputs. The signal powers are then compared to programmable thresholds. The programmable filters can be used to band-pass filter a certain tone or notch out certain tones, so that the signal power measurements are frequency selective. This filtering is useful in a telephony system because it can measure harmonic distortion, intermodulation, noise, etc.

The Si3217x incorporates an internal test load with a 5 kΩ nominal value that can be connected across Tip/Ring (Figure 22). The audio diagnostics system and built-in test load can be used to test the FXS interface (Si3217x) itself without requiring an external load, a connected line, or any relays. This facility can be used for production and in-service testing of such things as:

- Dial tone draw/break
- Audio quality measurements
- Pulse digit detection
- DC feed
- Ringtrip
- Polarity reversal
- Transmission loss

MLT, e.g., GR-909, is facilitated by the built-in DSP, monitor ADC, and test load. They provide the ability to detect multiple fault conditions within the CPE as well as on the Tip/Ring pair (T-R). Thirteen different measured and/or calculated parameters are reported by the Monitor ADC. Host software for use in conjunction with the ProSLIC API is available from Silicon Labs. Typical MLT tests include:

- Hazardous Potential Test – This checks for ac voltage > 50 V_{RMS} or dc voltage > 135 V between Tip and Ground (T-G) or Ring and Ground (R-G).
- Foreign Electromotive Force Test – Checks T-G or R-G for ac voltage > 10 V_{RMS} or dc voltage > 6 V. Uses same threshold as for hazardous voltage test.
- Resistive Faults Test – Checks for dc resistance from T-R, T-G or R-G. Any measurement < 150 kΩ is considered a resistive fault.
- Receiver-Off-Hook Test – Distinguishes between a T-R resistive fault and an off-hook condition.
- Ringers Test – Measures the magnitude of the connected ring load (REN) across T-R. Results are > 0.175 REN and < 5 REN for a valid load
- AC Line Impedance (line length) – T-R, T-G, and R-G. Generates a tone at several specific frequencies (audio band) and measures the reflected signal amplitude (complex spectrum) that comes back (with transhybrid balance filter disabled). The reflected signal is then used to calculate the line impedance based on certain assumptions of wire gauge, etc.
- Line Capacitance – T-R, T-G, R-G. Generates a linear ramp function with polarity reversal, and measures the time constant.

Diagnostic information is available even in the presence of fault conditions that cause the system's protection devices (fuses, PTCs, etc.) to open. A high-impedance sensing path (pins SRINGC and STIPC) can be used to measure the conditions on Tip/Ring even when the FXS system is effectively disconnected from the line. No relay is required and this sensing path inherently meets Dielectric Withstand per GR-49 (> 1000 V).

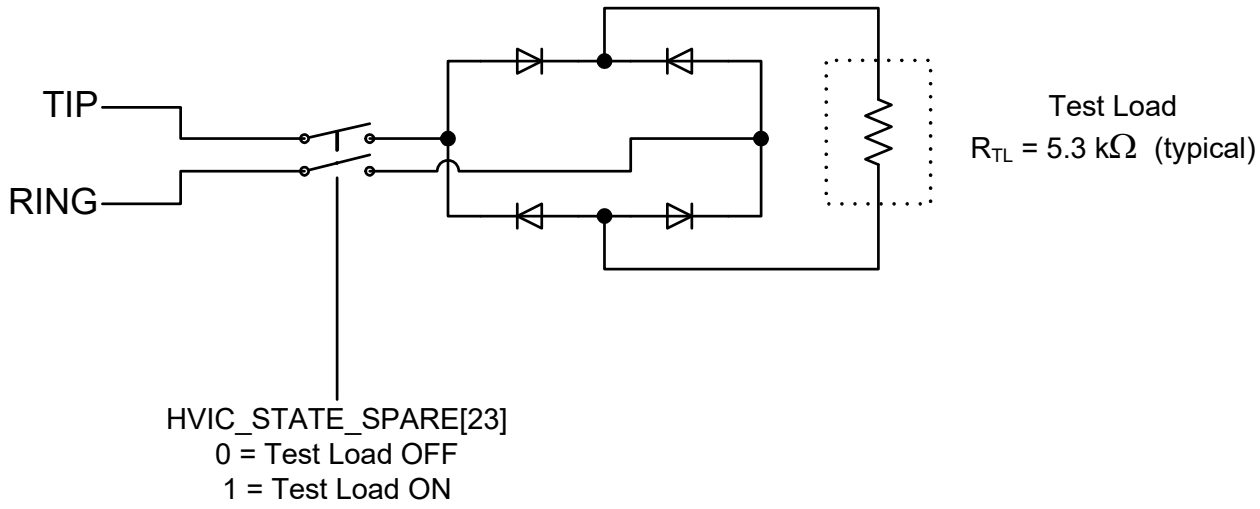


Figure 22. Si3217x Internal Test Load Circuit

4. FXO Features

4.1. Isolation Barrier

The Si32178/9 and Si3291x achieve an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories' patented signal processing techniques.

The isolation barrier provides greater than 5 kV isolation.

4.2. Power Management

The Si32178/9 FXO circuitry supports four power management modes: reset mode, normal mode, sleep mode and powerdown mode. When in reset mode, the Si32178/9 FXO is operational, except for the communication link to the line-side device (Si3291x). In normal mode, the chipset is fully operational. Sleep mode provides a low-power state that only supports ring detection, ring validation and wake-up-on-ring features. The powerdown mode puts the chipset in a non-functional state that requires the least power. Normal operation can be restored by issuing a reset.

4.3. In-Circuit Testing

Six FXO loopback modes are available to support production line testing and end-user diagnostics. Four of the test modes require a line-side power source.

4.4. Transmit/Receive Full-Scale Level

The Si32178/9 supports programmable maximum transmit and receive levels. The default signal level supported by the Si32178/9 is 0 dBm into a 600 Ω load. Two additional modes of operation offer increased transmit and receive level capability to enable use of the DAA in applications that require higher signal levels. The full-scale mode increases the full-scale signal level to +3.2 dBm into a 600 Ω load or 1 dBV into all reference impedances. The enhanced full-scale mode increases the full-scale signal level to +6.0 dBm into a 600 Ω load or 1.5 dBV into all reference impedances. The full-scale and enhanced full-scale modes provide the ability to trade off TX power and TX distortion for a peak signal. By using the programmable digital gain registers in conjunction with the enhanced full-scale signal level mode, a specific power level (+3.2 dBm for example) can be achieved across all ac termination settings.

4.5. Line Voltage Measurement

Line voltage can be measured in both on-hook and off-hook states with a resolution of 1V per bit and a range of -128 to 127V. Values between –3 to 3 V can, optionally, be forced to zero to mask measurements between –2 to 2 V, which may be unpredictable.

Polarity reversal detection is triggered whenever the sign of the measured value changes between positive and negative states.

4.6. Loop Current Measurement

Loop current sensing is available in the off-hook state. Loop currents are measurable down to the minimum operating loop current of the DAA, which is programmable to 10, 12, 14 or 16mA. Currents can be measured with a resolution of 1.1 or 3.3 mA over a range of 0 to 127 mA. If the loop current exceeds the programmed current limit of the device (160 mA or 60 mA), an over-current event is reported.

4.7. Parallel Handset Detection

The integrated line sensing capabilities of the Si32178/9 can be used to detect a parallel handset going off-hook. When off-hook, a significant change in loop current signals a parallel phone off-hook or on-hook event. When on-hook, a significant drop in line-voltage signals a parallel phone off-hook event.

4.8. DC Termination

The DAA has programmable settings for the dc impedance, current limiting, minimum operational loop current and TIP/RING voltage. The dc impedance of the DAA is normally represented with a 50 Ω slope as shown in Figure 23, but can be changed to an 800 Ω slope. This higher dc termination presents a higher resistance to the line as loop current increases.

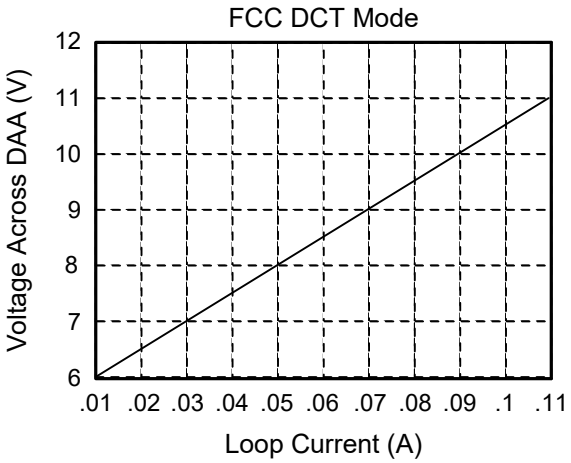


Figure 23. FCC Mode I/V Characteristics

For applications requiring current limiting per the TBR21 standard, the ILIM bit may be set to select this mode. In this mode, the dc I/V curve is changed to a 2000 Ω slope above 40 mA, as shown in Figure 24. This allows the DAA to operate with a 50 V, 230 Ω feed, which is the maximum linefeed specified in the TBR21 standard.

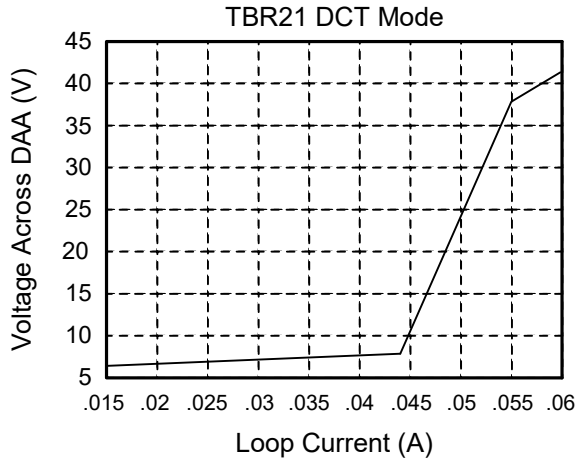


Figure 24. TBR21 Mode I/V Characteristics

4.9. AC Termination

The Si32911 is optimized to support only CTR21/TBR21 and FCC-compliant countries. The Si32919 is a globally-compliant DAA solution. The following table highlights the available ac termination settings in each device:

Table 16. AC Termination Settings for the Si3291x Line-Side Devices

Si32911	Si32919	AC Termination
✓	✓	600 Ω
	✓	900 Ω
✓	✓	270 Ω + (750 Ω || 150 nF) 275 Ω + (780 Ω || 150 nF)
	✓	220 Ω + (820 Ω || 120 nF) 220 Ω + (820 Ω || 115 nF)
	✓	370 Ω + (620 Ω || 310 nF)
	✓	320 Ω + (1050 Ω || 230 nF)
	✓	370 Ω + (820 Ω || 110 nF)
	✓	270 Ω + (750 Ω || 150 nF)
	✓	275 Ω + (780 Ω || 115 nF)
	✓	120 Ω + (820 Ω || 110 nF)
	✓	350 Ω + (1000 Ω || 210 nF)
	✓	200 Ω + (680 Ω || 100 nF)
	✓	600 Ω + 2.16 µF
	✓	900 Ω + 1 µF
	✓	900 Ω + 2.16 µF
	✓	600 Ω + 1 µF
	✓	Global complex impedance

4.10. Ring Detection

The Si32178/9 supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal of the ring signal. See “Transhybrid Balance” on page 31. The Si32919 supports three programmable ring thresholds: 15 V ±10%, 21 V ±10%, and 45 V ±10%. The Si32911 supports 15 V ±10%.

4.11. Ring Validation

Ring validation prevents false triggering of a ring detection by validating the ring parameters. Invalid signals, such as a line-voltage change when a parallel handset goes off-hook, pulse dialing, or a high-voltage line test are ignored. Ring validation can be enabled during normal operation and in sleep mode when a valid external PCLK signal is supplied.

The ring validation circuit calculates the time between alternating crossings of positive and negative ring thresholds for a programmed period of time to validate that the ring frequency is within tolerance. High and low frequency tolerances are also programmable.

4.12. Ringer Impedance and Threshold

The ring detector on the Si3291x device is resistively coupled to the line. This coupling produces a high ringer impedance to the line of approximately 20 MΩ to meet the majority of country PTT specifications including FCC and TBR21.

A synthesized ringer impedance can also be enabled to comply with maximum ringer impedance specifications of several countries including Poland, South Africa, and Slovenia.

4.13. Pulse Dialing and Spark Quenching

Pulse dialing is accomplished by going off- and on-hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have strict specifications for pulse fidelity including make and break times, make resistance, and rise and fall times. In a traditional, solid-state dc holding circuit, there are a number of issues in meeting these requirements. The Si3217x dc holding circuit has active control of the on- and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries, such as Italy, the Netherlands, South Africa, and Australia, deal with the on-hook transition during pulse dialing. The Si32919 supports three distinct on-hook speeds to pass spark quenching tests without additional BOM components.

4.14. Receive Overload Detection

The Voice DAA chipset is capable of monitoring and reporting receive overload conditions on the line. Billing tones, parallel phone off-hook events, polarity reversals and other disturbances on the line may trigger multiple levels of overload detection.

Certain events, such as billing tones, can be sufficiently large to disrupt the line-derived power supply of an Si3291x line side device. The Si3291x devices support a dynamically-enabled high-impedance mode to ensure that they maintain the off-hook line state during these events.

4.15. On-Hook Line Monitor

The on-hook line monitor mode allows the Si32178/9 to receive line activity when in an on-hook state. This mode is typically used to detect caller ID data (see “4.16. Transhybrid Balance”). Caller ID data can be gained up or attenuated in the device.

4.16. Transhybrid Balance

The Si32178/9 contains an on-chip analog hybrid that performs the 2- to 4-wire conversion and near-end echo cancellation. This hybrid circuit is adjusted for each ac termination setting selected to achieve a minimum transhybrid balance of 20 dB when the line impedance matches the selected ac termination.

The Si3217x also offers a programmable digital hybrid stage for additional near-end echo cancellation. For each ac termination setting, the hybrid can be programmed with coefficients to increase cancellation of real-world line impedances. This digital filter can produce 10 dB or greater of near-end echo cancellation in addition to the trans-hybrid loss from the analog hybrid circuitry.

5. System Interfaces

5.1. SPI Control Interface

The controller interface to the Si3217x is a 4-wire interface modeled after microcontroller and serial peripheral devices. The interface consists of a clock (SCLK), chip select (CS), serial data input (SDI), and serial data output (SDO). In addition, the ProSLIC devices feature a serial data through output (SDITHRU) to support operation of up to 16 channels using a single chip select line. The FXS port and FXO port (if available and enabled) each occupy one SPI channel. The device operates with both 8-bit and 16-bit SPI controllers.

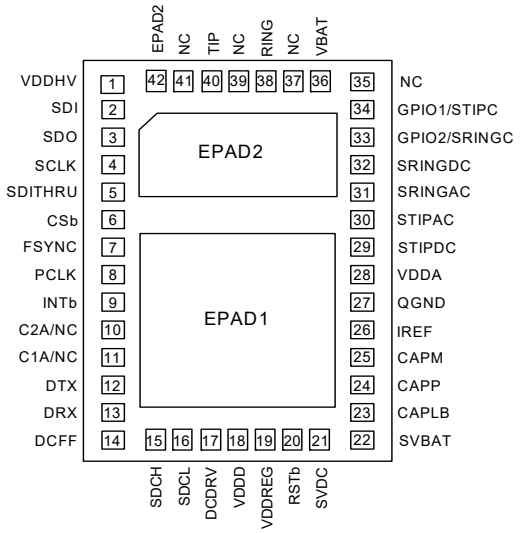
5.2. PCM Interface and Companding

The Si3217x contains a flexible, programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled by the PCM clock (PCLK) and frame sync (FSYNC) inputs as well as the PCM Mode Select, PCM Transmit Start, and PCM Receive Start settings.

The interface can be configured to support from 8 to 128 8-bit time slots in each 125 µs frame, corresponding to a PCM clock (PCLK) frequency range of 512 kHz to 8.192 MHz. 1.544 MHz is also supported.

The Si3217x supports both µ-255 Law (µ-Law) and A-law companding formats in addition to 16-bit linear data mode with no companding.

6. Pin Descriptions: Si3217x

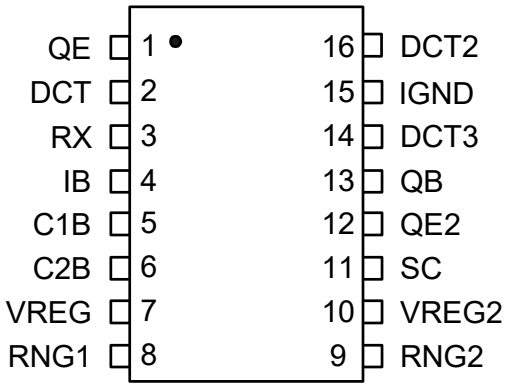


Pin #	Pin Name	Description
1	VDDHV	IC Voltage Supply.
2	SDI	Serial Port Data Input. Serial port control data input.
3	SDO	Serial Port Data Output. Serial port control data output.
4	SCLK	**Serial Port Bit Clock Input.** Serial port clock input. Controls the serial data on SDO and latches the data on SDI.
5	SDITHRU	**SDI Passthrough.** Cascaded SDI output signal for daisy-chain mode.
6	CSb	**Chip Select Input.** Active low. When inactive, SCLK and SDI are ignored and SDO is high impedance. When active, the serial port is operational.
7	FSYNC	Frame Sync Clock Input. 8 kHz frame synchronization signal for the PCM bus. May be short or long pulse format.
8	PCLK	PCM Bus Clock Input. Clock input for PCM bus timing.
9	INTb	Interrupt Output. Maskable interrupt output. Open drain output for wire-ORed operation with FXS interrupts enabled only. Output becomes push-pull if FXO interrupts are enabled.
10	C2A/NC	Si32178/9 only: Connects to one side of the isolation capacitor C1. Used to communicate with the FXO line-side device. For versions of Si3217x that do not support an FXO I/F or if the FXO line-side device is not populated this pin should be left unbiased.

Pin #	Pin Name	Description
11	C1A/NC	Si32178/9 only: Connects to one side of the isolation capacitor C2. Used to communicate with the FXO line-side device. For versions of Si3217x that do not support an FXO I/F or if the FXO line-side device is not populated this pin should be left unbiased.
12	DTX	**Transmit PCM Data Output.** Output data to PCM bus.
13	DRX	**Transmit PCM Data Input.** Input data from PCM bus.
14	DCFF	**DC Feed-Forward/High Current General Purpose Output.** Feed-forward drive of external bipolar transistors to improve dc-dc converter efficiency
15	SDCH	**DC Monitor.** DC-DC converter monitor input used to detect overcurrent situations in the converter
16	SDCL	**DC Monitor.** DC-DC converter monitor input used to detect overcurrent situations in the converter.
17	DCDRV	**DC Drive/Battery Switch.** DC-DC converter control signal output, which drives external bipolar transistor or MOSFET.
18	VDDD	**IC Voltage Supply.** Digital power supply for internal digital circuitry.
19	VDDREG	**Regulated Core Power Supply.**
20	RSTb	**Reset Input.** Active low input. Hardware reset used to place all control registers in the default state.
21	SVDC	**DC-DC Input Voltage Sensor.** Serves V_{DC} input to dc-dc converter.
22	SVBAT	**VBAT Sense.** Analog current input used to sense voltage on dc-dc converter output voltage lead.
23	CAPLB	**Calibration Capacitor.**
24	CAPP	**SLIC Stabilization Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
25	CAPM	**SLIC Stabilization Capacitor.** Capacitor used in low pass filter to stabilize SLIC feedback loops.
26	IREF	**Current Reference Input.** Connects to an external resistor used to provide a high accuracy reference current.
27	QGND	**Quiet Ground Reference Input.**

Pin #	Pin Name	Description
28	VDDA	**Analog Supply Voltage.** Analog power supply for internal analog circuitry.
29	STIPDC	**TIP DC Sense.** Analog current input used to sense voltage on the TIP lead.
30	STIPAC	**TIP AC Sense Input.** Analog ac input used to detect voltage on the TIP lead.
31	SRINGAC	**RING AC Sense Input.** Analog ac input used to detect voltage on the RING lead
32	SRINGDC	**RING DC Sense Input.** Analog current input used to sense voltage on the RING lead.
33	GPIO2 SRINGC	**General Purpose I/O.** RING Coarse Sense Input. Voltage sensing outside protection circuit.
34	GPIO1 STIPC	**General Purpose I/O.** TIP Coarse Sense Input. Voltage sensing outside protection circuit.
35	NC	**No Connect.** This pin should be left unbiased.
36	VBAT	**Battery Voltage Supply.** Connect to battery supply from dc-dc converter.
37	NC	**No Connect.** This pin should be left unbiased.
38	RING	**RING Terminal.** Connect to the RING lead of the subscriber loop.
39	NC	**No Connect.** This pin should be left unbiased.
40	TIP	**TIP Terminal.** Connect to the TIP lead of the subscriber loop.
41	NC	**No Connect.** This pin should be left unbiased.
42	NC	**No Connect.** This pin is internally connected to EPAD2 and should be left unbiased.
—	EPAD1	**Exposed paddle.** Connect to ground.
—	EPAD2	**Exposed paddle.** Connect to electrically-isolated low thermal impedance inner layer and/or backside thermal plane using multiple thermal vias.

7. Pin Descriptions: Si3291x



Pin #	Pin Name	Description
1	QE	**Transistor Emitter.** Connects to the emitter of Q3.
2	DCT	**DC Termination.** Provides dc termination to the telephone network.
3	RX	**Receive Input.** Serves as the receive side input from the telephone network.
4	IB	**Internal Bias.** Provides a bias voltage to the device.
5	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1. Used to communicate with the system-side device (Si32178/9).
6	C2B	**Isolation Capacitor 2B.** Connects to one side of isolation capacitor C2. Used to communicate with the system-side device (Si32178/9).
7	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
8	RNG1	**Ring 1.** Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the DAA.
9	RNG2	**Ring 2.** Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the DAA.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	SC	**SC Connection.** Enables external transistor network. Should be tied through a 0 Ω resistor to I_{GND}.

Pin #	Pin Name	Description
12	QE2	**Transistor Emitter 2.** Connects to the emitter of Q4.
13	QB	**Transistor Base.** Connects to the base of transistor Q4.
14	DCT3	**DC Termination 3.** Provides dc termination to the telephone network.
15	IGND	**Isolated Ground.** Connects to ground on the line-side interface.
16	DCT2	**DC Termination 2.** Provides dc termination to the telephone network.

8. Ordering Guide

Table 17. Si3217x-3291x Ordering Guide[1]

P/N	Description	Package	Max V_{BAT}	Temperature
Si32170-B-FM1	Narrowband FXS, PCM Interface, DTMF detection, pulse metering	LGA[2]	–136 V	0 to 70 °C
Si32170-B-GM1	Narrowband FXS, PCM Interface, DTMF detection, pulse metering	LGA[2]	–136 V	–40 to 85 °C
Si32171-B-FM1	Narrowband FXS, PCM Interface, DTMF detection, pulse metering	LGA[2]	–110 V	0 to 70 °C
Si32171-B-GM1	Narrowband FXS, PCM Interface, DTMF detection, pulse metering	LGA[2]	–110 V	–40 to 85 °C
Si32176-B-FM1	Wideband capable FXS, PCM Interface	LGA[2]	–110 V	0 to 70 °C
Si32176-B-GM1	Wideband capable FXS, PCM Interface	LGA[2]	–110 V	–40 to 85 °C
Si32177-B-FM1	Wideband capable FXS, PCM Interface	LGA[2]	–136 V	0 to 70 °C
Si32177-B-GM1	Wideband capable FXS, PCM Interface	LGA[2]	–136 V	–40 to 85 °C
Si32178-B-FM1	Wideband capable FXS with FXO support, PCM Interface, DTMF detection	LGA[2]	–110 V	0 to 70 °C
Si32179-B-FM1	Wideband capable FXS with FXO support, PCM Interface, DTMF detection	LGA[2]	–136 V	0 to 70 °C

Notes:
1. Adding the suffix "R" to the part number (e.g. Si32176-B-FM1R) denotes tape and reel.
2. LGA – Land Grid Array.

FXO P/N	Region	Ringer Thresholds	On-Hook Speeds	Temperature
Si32911-A-FS	FCC/CTR21	1	2	0 to 70 °C
Si32919-A-FS	Global	3	3	0 to 70 °C

Note: Adding the suffix “R” to the part number (e.g., Si32919-A-FSR) denotes tape and reel.

Table 18. Si3217x Revision B Evaluation Kit Ordering Guide

Part Number	Description	V_{BAT} Max
Si32178BQC11SL0KIT	Wideband FXS, 100 V, 3 W Quasi-Cuk (MOSFET and inductor based) dc-dc converter EVB	–100 V
Si32179BFB11SL0KIT	Wideband FXS, 136 V, 7.6 W flyback (MOSFET transformer based) dc-dc converter EVB	–136 V

9. Package Outline

9.1. 42-Pin LGA

Figure 25 illustrates the package details for the Si3217x. Table 19 lists the values for the dimensions shown in the illustration.

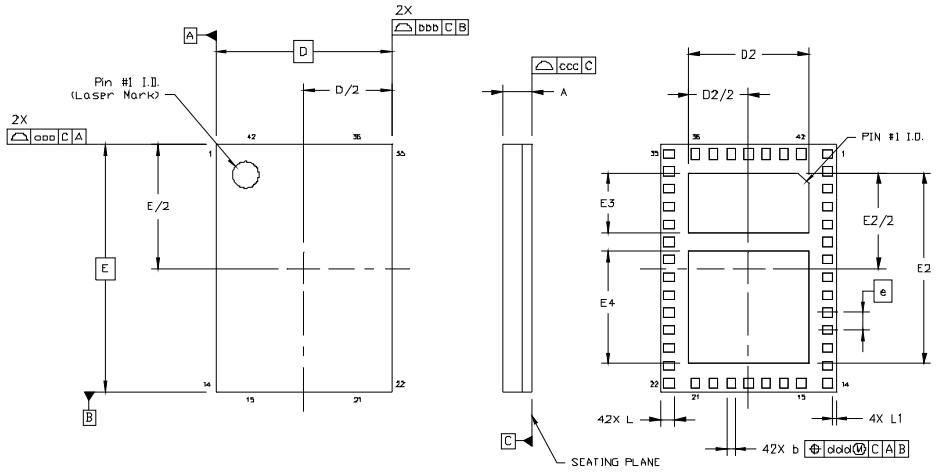


Figure 25. 42-Pin LGA Package

Table 19. 42-Pin LGA Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
b	0.20	0.25	0.30
D		5.00 BSC	
D2	3.35	3.40	3.45
e		0.50 BSC	
E		7.00 BSC	
E2	5.35	5.40	5.45
E3	1.65	1.70	1.75
E4	3.15	3.20	3.25
L	0.35	0.40	0.45
L1	0.05	0.10	0.15
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. PCB Land Pattern Si3217x LGA

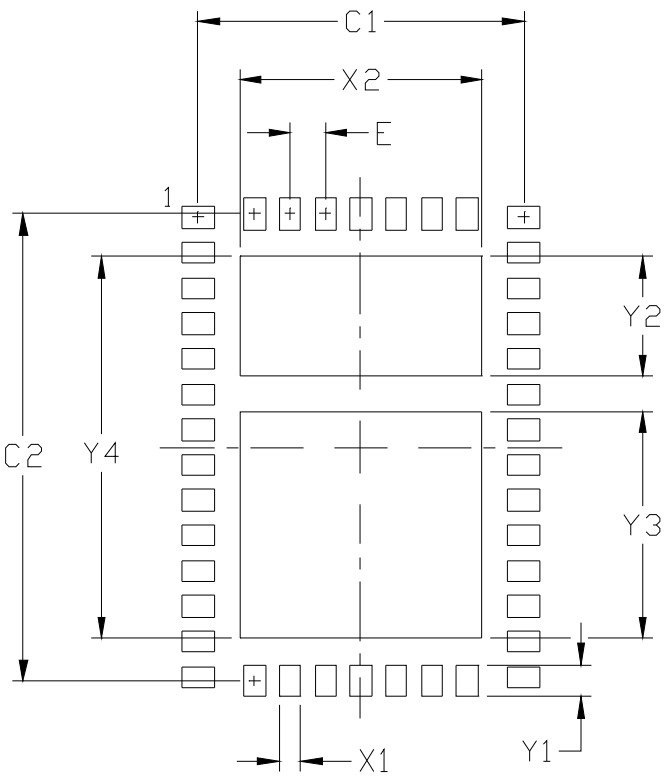


Table 20. PCB Land Pattern

Dimension	mm
C1	4.60
C2	6.60
E	0.50
X1	0.30
X2	3.45
Y1	0.45
Y2	1.75
Y3	3.25
Y4	5.45

Notes:
General

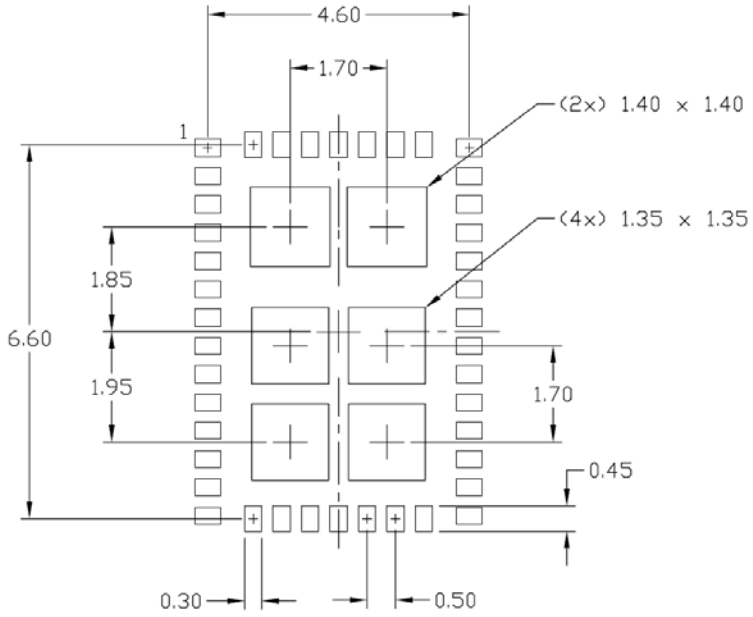
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

10.1. Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

10.2. Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 1x2 array of 1.40 mm square openings on 1.7 mm pitch should be used for the top center pad and a 2x2 array of 1.35 mm square openings on 1.7 mm pitch should be used for the bottom center pad (as shown below).



10.3. Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

11. Package Outline: 16-Pin SOIC

Figure 26 illustrates the package details for the Si3291x. Table 21 lists the values for the dimensions shown in the illustration.

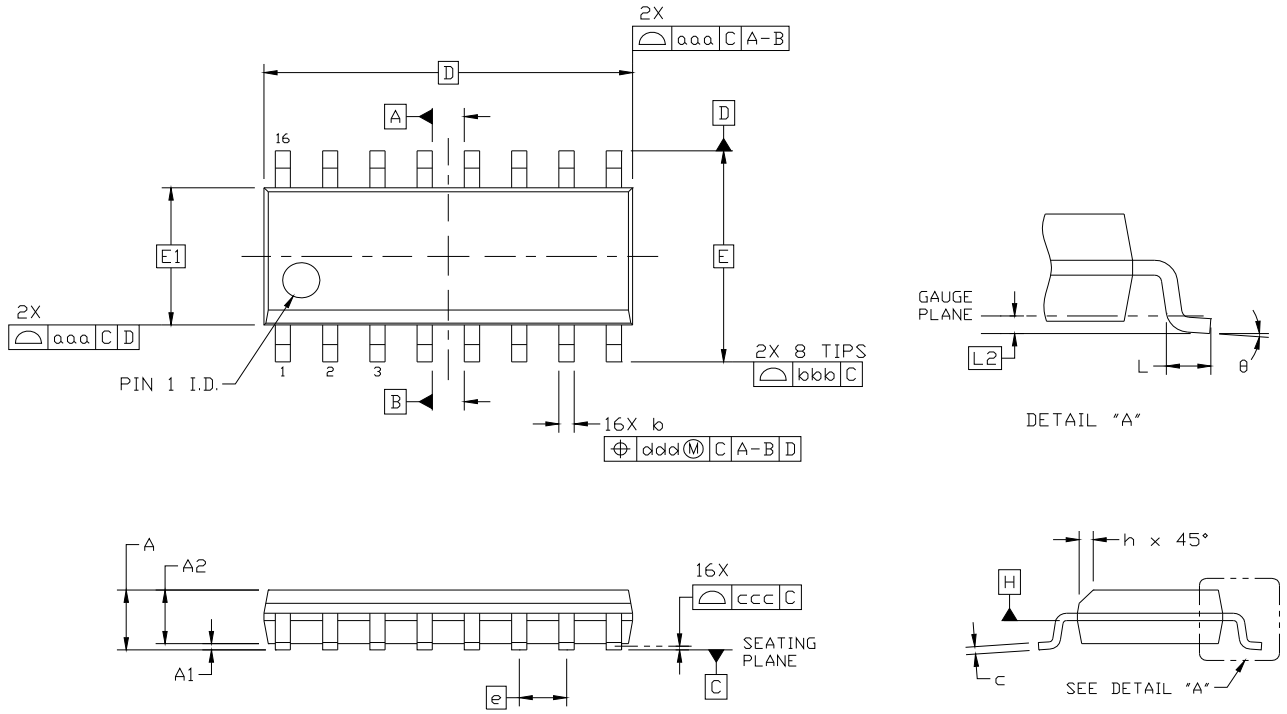


Figure 26. 16-Pin Small Outline Integrated Circuit (SOIC) Package

Table 21. 16-Pin SOIC Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. PCB Land Pattern Si3291x SOIC

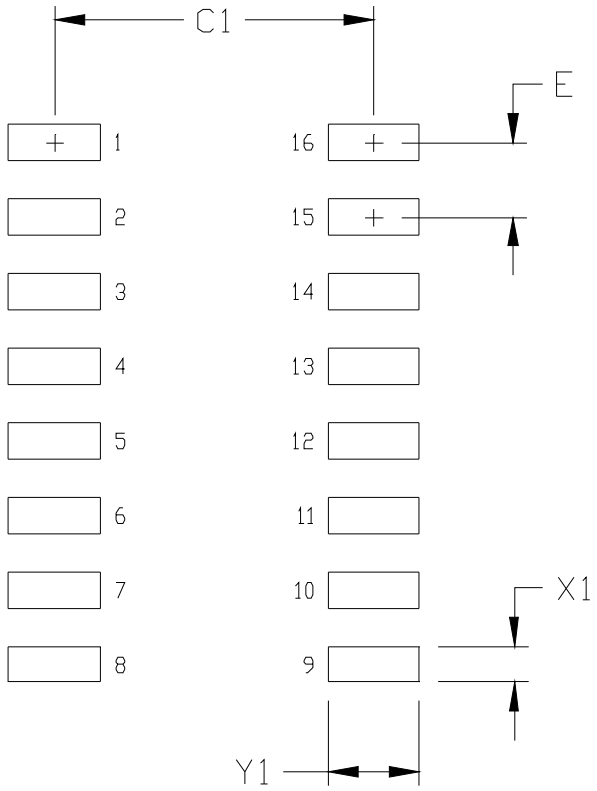


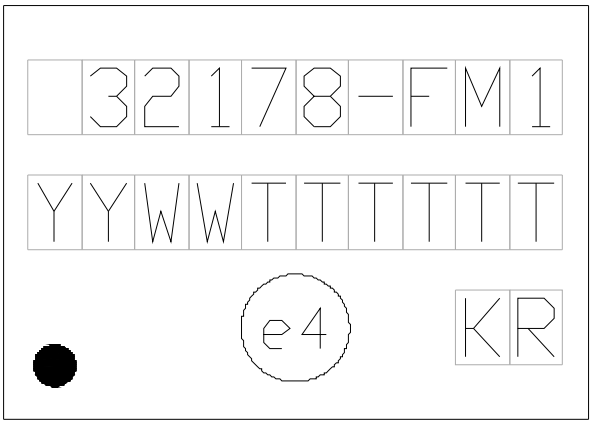
Table 22. PCB Land Pattern

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05mm is assumed.

13. Top Markings

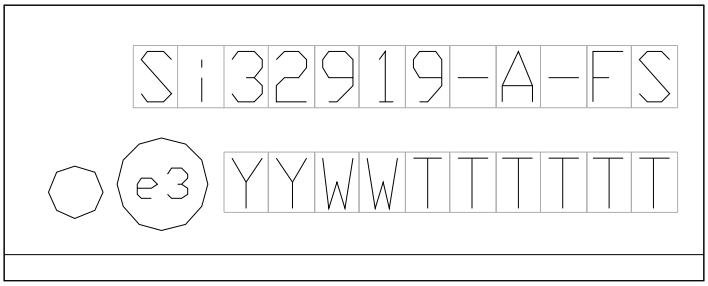
13.1. Si3217x LGA Package Top Marking



13.2. Si3217x LGA Package Top Marking Explanation

Line 1 Marking:	**Device Part Number**	**e.g., 32178-FM1**
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 0.5 mm Diameter Lower Left-Justified	Pin 1 Identifier
	Circle = 1.3 mm Diameter Center-Justified	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	e.g., KR

13.3. Si32919 Top Mark



13.4. Si3291x Top Mark Explanation

Line 1 Marking:	**Customer Part Number**	**Si32919-A-FS**
Line 2 Marking:	Circle = 1.3 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT = Mfg Code	Manufacturing Code

Revision History

Revision 1.5

February, 2021

- Removed references to 256 kHz PCLK, which is not supported.
- Clarified interrupt pin description in “6. Pin Descriptions: Si3217x” .
- Removed Si32178-B-GM1, Si32179-B-GM1, Si32919-A-GS, Si32911-A-GS, all Si3217x-B-FM, and all Si3217x-B-GM from “8. Ordering Guide” .
- Removed schematics and bill of materials sections as these are covered in “AN340: Si3217x Designer's Guide”.
- Updated EVB ordering numbers.

Revision 1.4

March, 2013

- Added new part numbers Si32170 and Si32179.
- Corrected formatting.
- Added additional thermal resistance values θ_{JB} and θ_{JC}.
- Standardized test condition for supply currents measurement and values in Table 2 for Forward/Reverse Active, Off-hook state to match data sheets of other current ProSLICs.

Revision 1.3

March, 2012

- Added industrial temperature (–40 to 85 °C) options for the Si32178 and Si3219x devices.

Revision 1.2

November, 2011

- Added LGA package information.
- Corrected thermal resistance, θ_{JA}, to 53°C/W and adjusted maximum continuous power dissipation, PD, to 0.75W.
- Added definition of dBm0.
- Added specification for RST (with overbar) internal pull up current (same as SDITHRU).
- Added support for PCLK as low as 256kHz (3906ns period) for commercial temperature parts only (0°C to +70°C).
- Changed PCLK jitter tolerance spec for FXS to 8 nsRMS.
- Added PCLK jitter tolerance for FXO devices - 2 nsRMS.
- Corrected SDCL connection in top level schematic to make it clear that it is not connected directly to ground.

Revision 1.1

April, 2010

- Removed ringing amplitude with 5 REN load from Table 4 because these values were specified with an invalid RDO of 100 Ω.
- Decreased maximum PCLK period to 1953 ns (was 3906 ns) in Table 13 and added PCLK jitter tolerance of ±8 ns.
- Updated schematics, BOMs and added buck-boost dc-dc converter schematics.
- Added package top mark drawings.
- Added PCB land patterns and soldering notes.

Revision 1.0

May, 2009

- Renamed Si32176H to Si32177.
- Updated descriptions of voltage ratings in the Description section on front page and the Overview section.
- Updated Ordering Guide.
- Updated V_{BAT} entries in Table 1 and Table 2.
- Added V_{TIP} and V_{RING} entries to Table 1.
- Updated front page Description section.
- Updated Table 14.
- Updated Table 1, 2, 3, 4, 5, 10, and 13.
- Added Typical Applications schematics.
- Added Figure 20, 21, 22, and 19.
- Updated section “2. Overview” , “3.4. Power Monitoring and Power Fault Detection” , “3.14. Pulse Metering (Si32170/1 Only)” , “3.17. In-Circuit and Metallic Loop Testing (MLT)” , “6. Pin Descriptions: Si3217x” , “7. Pin Descriptions: Si3291x” , and “11. Package Outline: 16-Pin SOIC” .

Revision 0.12

November, 2008

- Added description of maximum battery ratings to front page description.
- Deleted operating temperature range in Table 1.
- Changed TA from 70°C to 85°C for continuous power dissipation entries in Table 1.
- Added -130V rated devices to Table 1.
- Replaced TBD for SOIC-16 Continuous Power Dissipation.
- Added Battery Voltage row for Si3217xH to Table 2.
- Updated supply currents in Table 3.
- Added Ringing Amplitude information for –130 V rated devices to Table 5.
- Edited second and third paragraphs in the Overview Section with information about -130V rated ICs.
- Updated the FXS table in the Ordering Guide.
- Added G-grade devices under Product Identification.
- Added part number information to Package Outline descriptions in sections 10 and 11.

Revision 0.11

August, 2008

- Corrected name of pin 34 on Si3217 pin assignment diagrams.
- Corrected names and descriptions for Si3217 pins numbers 10, 11, 21, and 22.
- Expanded descriptions for Si3217 pins numbers 35, 37,39, 41 and 42.
- Changed EPAD names to match reference design schematics.
- Removed footnote from Si3217 pin descriptions table.
- Added C1A, C1B, C2A, C2B pin names to Functional Block Diagram.
- Added entries for C1A, and C2A to Table 11, “DC Characteristics”.
- Harmonized IO polarities of for VOH and VOL test conditions for outputs in Table 11.
- Deleted references to relay drivers in Table 11.
- Corrected GPIO1/STIPC and GPIO2/SRINGC entries in Table 11.
- Deleted INT entry for V_{OH} in Table 11.
- Added Si3291x to title.
- Added image and pin assignment diagram for Si3291x to cover page.

- Deleted VBAT = –135 V and VBAT = –130 V entries from Ringing Amplitude row of Table 5.
- Clarified titles of Tables 4 through 8 to indicate FXS or FXO.
- Corrected references in footnote 1 of Table 8.
- Added Figures 1 through 11.
- Added Tables 9 and 10.
- Replaced Si32911/19 with Si3291x throughout.
- Replaced Si3217 with Si3217x throughout.
- Replaced Si3291 with Si3291x throughout.
- Deleted G-Grade from Table 2.
- Removed 3.3 V from title of Table 3.
- Filled-in Typical supply currents in Table 3.
- Added system-side FXO supply current rows to Table 3.
- Added reference to AN340 to the Calibration Time row in Table 5.
- Corrected footnote in Table 5.
- Deleted Si32175-A-FM and Si32177-A-FM from Ordering Guide.
- Added Section 9 Product Identification.

Revision 0.1

August, 2008

- Initial release.