UG405: Si3471 EVB User's Guide

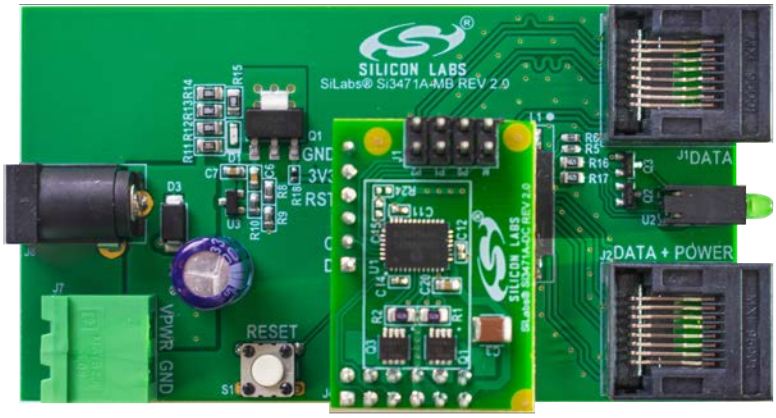
Si3471 Single 90 W Ethernet Port EVB

The Si3471 is a fully autonomous 802.3bt PSE capable of supplying 90 W on a single PoE Ethernet port. Three static I/O pins configure the maximum power the Si3471 will grant to a connected PD. The Si3471 includes a built-in LED driver to indicate the status of the PoE Ethernet port.

Configured as a single Ethernet port mid-span, the Si3471 EVB provides easy access to all Si3471 features. The compact design includes a two-layer daughtercard and a two-layer baseboard. Both are excellent starting points for new Si3471 designs.

KEY FEATURES

- Adds 90 W PoE to a non-powered Ethernet cable
- Configurable max power output and access to Si3471 features
- Small, simple, two layer PCBs
- Only 1.8 x 3.25 inches, 46 x 83 mm
- IEEE 802.3bt compliant
- 54 V, 90 W power supply included



Parameter	Condition	Specifications
PSE Input Voltage Range	Connector J1	52 to 57 V
PoE Type/Class	Type 4, Class 8	IEEE 802.3bt
Daughtercard Size		0.875 x 1.25 inches, 22 x 32 mm
Baseboard Size		1.8 x 3.25 inches, 46 x 83 mm
EVB Height	Does not include headers	1 inch, 25 mm

Table of Contents

1. Kit Description and Powering up the Si3471 EVB

The Si3471 EVB consists of a two-layer daughtercard and a two-layer baseboard. The daughtercard includes the Si3471, FETs, and a header for configuring the PWRAVL and MIDb pins on the Si3471.

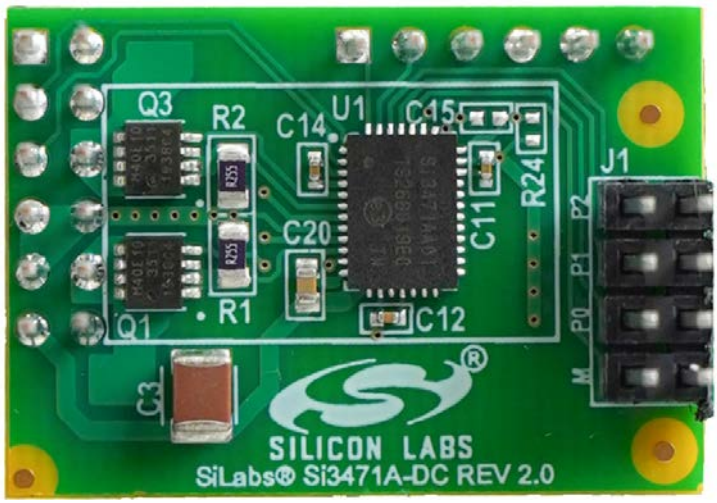


Figure 1.1. Si3471 EVB Daughtercard

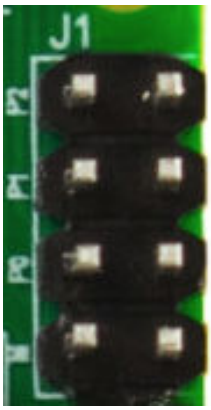


Figure 1.2. J1 Configuration Header

Adding a jumper to P0, P1, or P2 pulls the corresponding PWRAVL pin low. Adding a jumper to M pulls the MIDb pin low. The Si3471 EVB is shipped without any jumpers installed (Class 8 power). See 3. Configuring Maximum Available Power for configuration details.

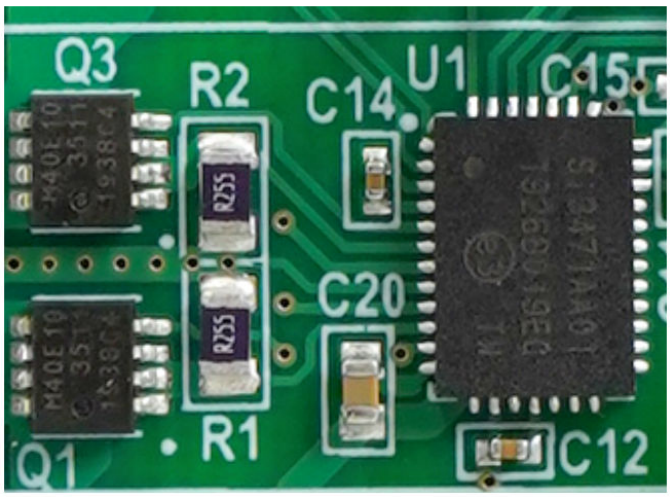


Figure 1.3. Si3471 and External FETs

The above figure shows the Si3471 and external FETs for powering the four twisted pairs in the Ethernet cable.

The Si3471 EVB baseboard includes the RJ45 Ethernet jacks, 802.3bt Ethernet magnetics, status LEDs, a reset button, and power jacks. The shrouded header, J5, is installed for EVB production use only and is not used for end user evaluation. The RJ45 connector, J1, accepts non-powered Ethernet, and the RJ45 connector, J2, outputs Power over Ethernet plus any Ethernet data from J1. Two LEDs indicate the status of the Si3471 EVB. The lower LED is connected to the LED2 driver on the Si3471, and the upper LED is connected to the LED1 driver on the Si3471. In the default Class 8 configuration of the Si3471, only the upper LED is used as the LED2 driver is only used when the Si3471 is configured for 802.3at operation. Finally, the push button is tied to RESETb and resets the Si3471.

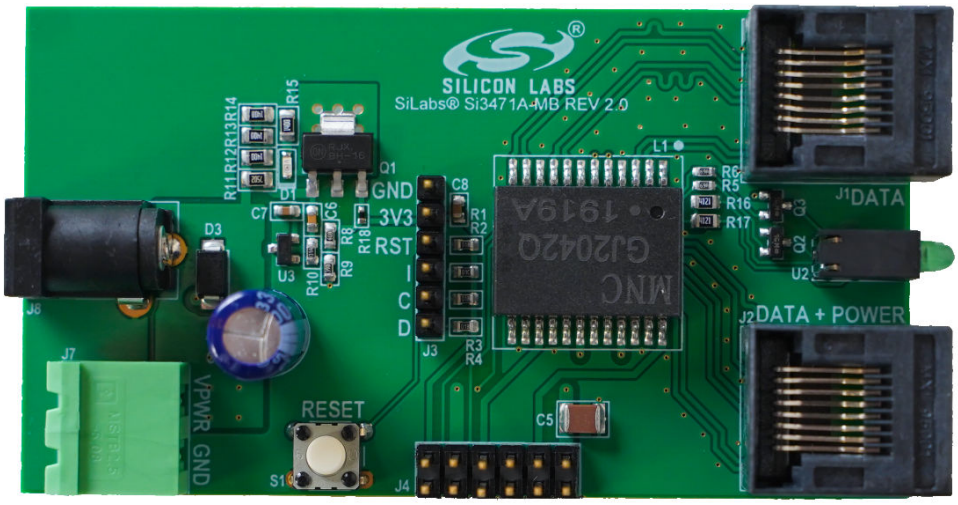


Figure 1.4. Si3471 EVB Baseboard

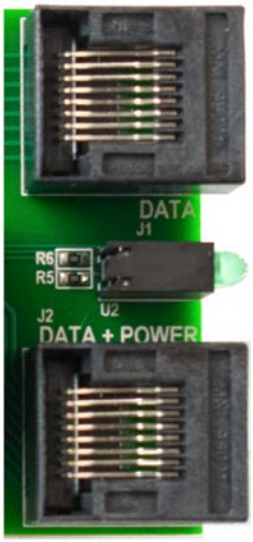


Figure 1.5. J1 and J2

J1 accepts non-PoE Ethernet, and J2 outputs 802.3bt PoE and adds any Ethernet data traffic from J1.

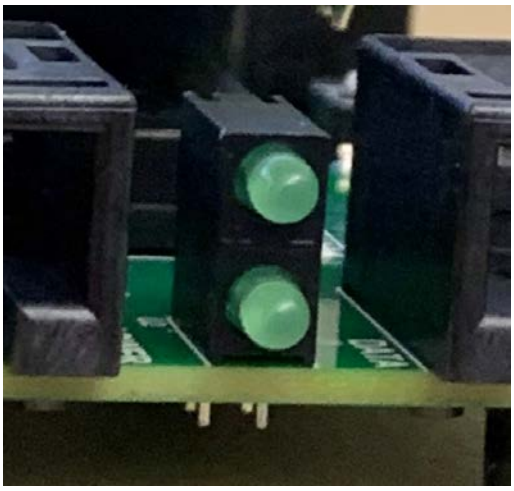


Figure 1.6. Upper and Lower LEDs

The upper LED is tied to the LED1 driver, and the lower LED is tied to the LED2 driver on the Si3471.

Figure 1.7. S1 Reset Button

S1 resets the Si3471.

Table 1.1. LED Status Indicators[1]

LED Indicator	Status
LED on, no blinking	Port successfully powered at requested power level.
LED blinking slowly	Looking for a valid detection signature.
LED blinking quickly	Error condition, such as port overload.

Note:
1. See the Si3471 Data Sheet for more information.

The Si3471 EVB can be powered using either a standard barrel jack (J8) or two-wire connection (J7) using standard PoE voltages of 52 to 57 V. The barrel jack accepts either 2.1 or 2.5 mm adapters. The barrel jack is rated only for 24 V operation and must only be used with human supervision in an air-conditioned, nominal-room-temperature and low-humidity environment. When using a commercially available dc power supply, the dc power jack should already be connected to the EVB before plugging the supply into the ac mains. As such, DO NOT plug/unplug power at the dc jack. If there is a need to reset the board, use the supplied pushbutton reset.

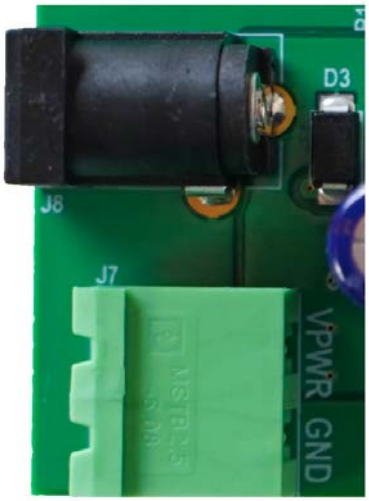


Figure 1.8. Barrel Jack with Two Terminal Power Connectors

2. Si3471 Daughtercard and Baseboard Schematics

Silicon Labs will provide a free schematic and PCB layout review. To submit a support request for the review, visit www.siliconlabs.com/support.

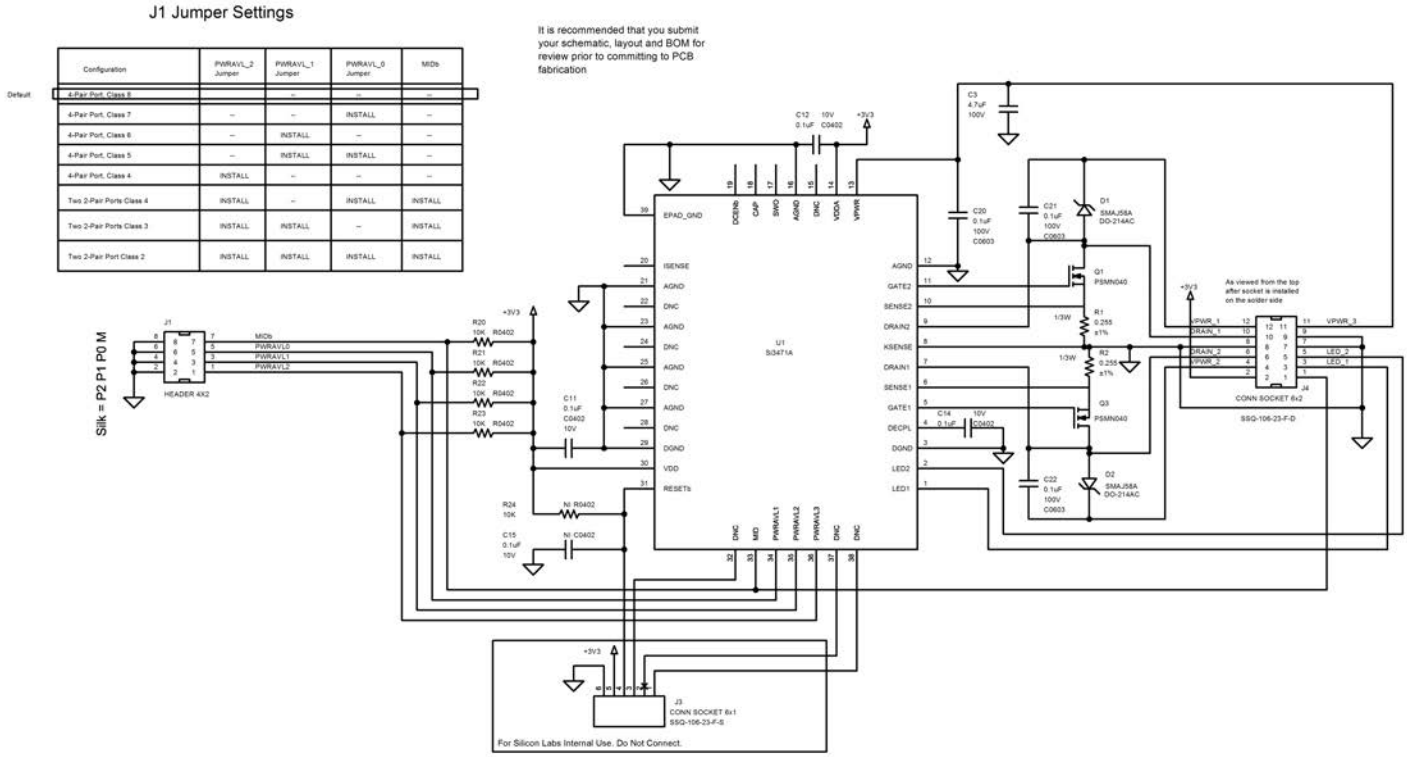


Figure 2.1. Daughtercard Schematic

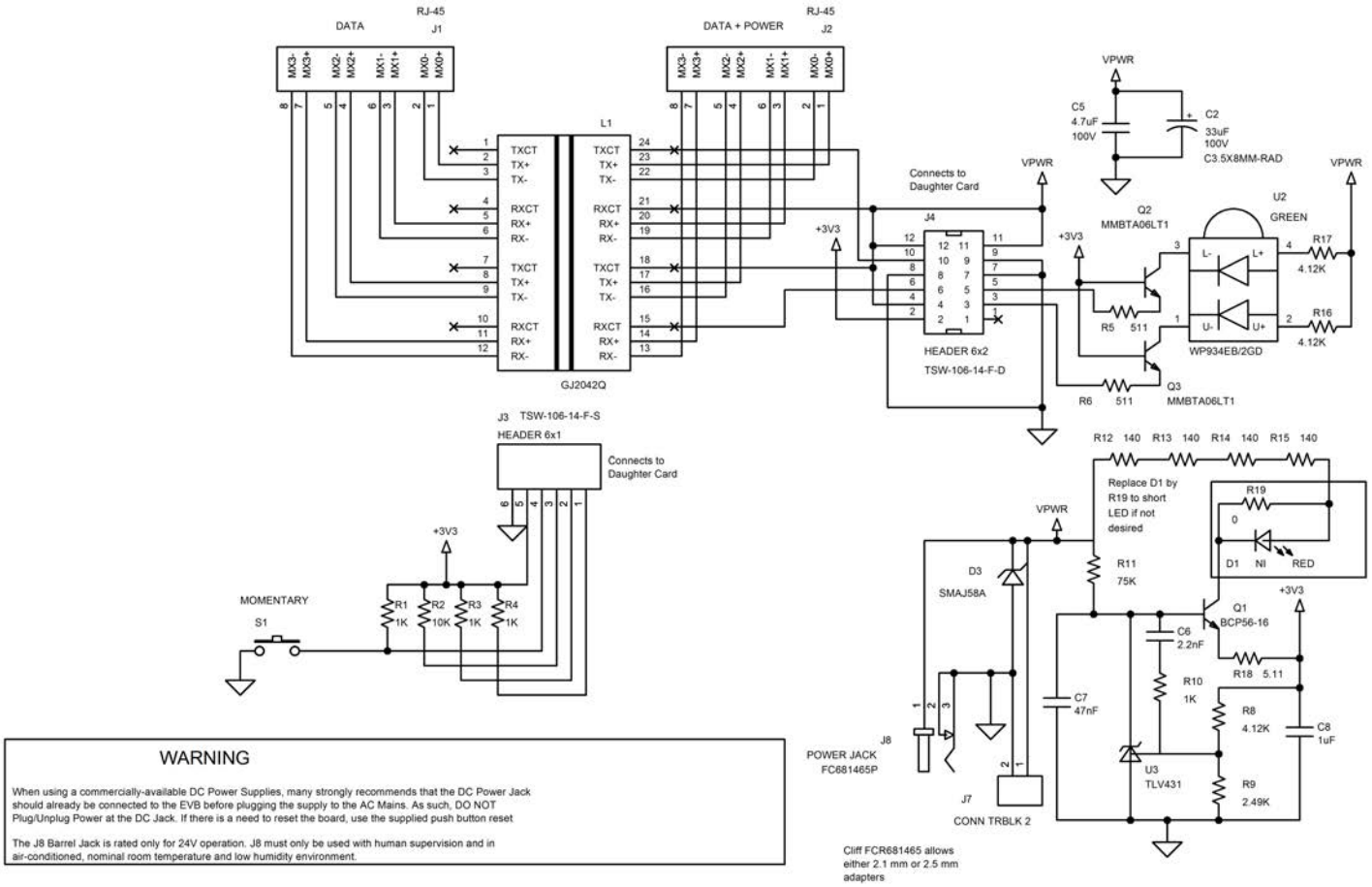


Figure 2.2. Baseboard Schematic

3. Configuring Maximum Available Power

The PWRAVL pins on the Si3471 configure the maximum power the Si3471 will grant to a connected PD. J1 on the daughtercard allows the PWRAVL pins to be configured when using the Si3471 EVB. The following table shows the jumper settings and their corresponding maximum power.

Table 3.1. Jumper Settings and Maximum PD Power

Configuration	Maximum Power Granted to PD	M Jumper MIDb	P0 Jumper PWRAVL0	P1 Jumper PWRAVL1	P2 Jumper PWRAVL2
Single 4-pair port, Class 8 (Default Configuration)	90 W	—	—	—	—
Single 4-pair port, Class 7	75 W	—	Install	—	—
Single 4-pair port, Class 6	60 W	—	—	Install	—
Single 4-pair port, Class 5	45 W	—	Install	Install	—
Single 4-pair port, Class 4	30 W	—	—	—	Install
Two 2-pair ports, Class 4[1]	60 W	—	Install	—	Install
Two 2-pair ports, Class 3[1]	30.8 W	—	—	Install	Install
Two 2-pair ports, Class 2[1]	15 W	—	Install	Install	Install

Note:
1. Si3471 EVB only supports one Ethernet port

4. Layout

Daughtercard PCB Layout

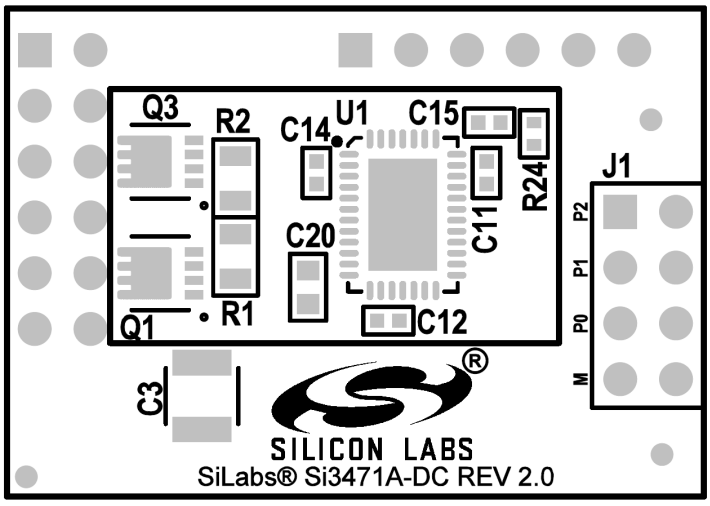


Figure 4.1. Top Silkscreen

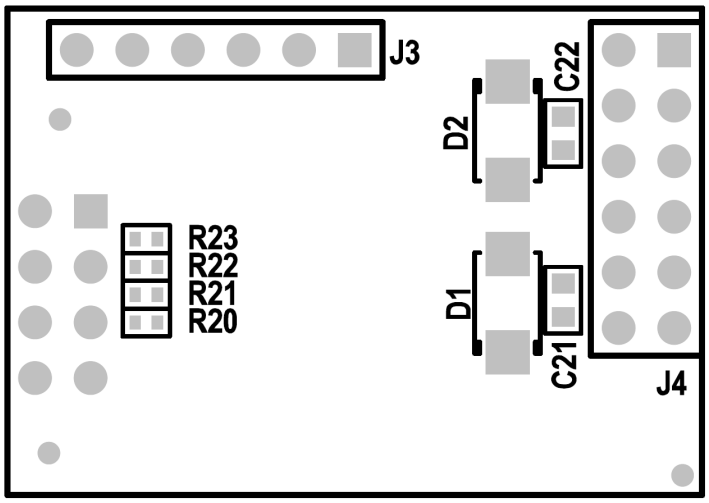


Figure 4.2. Bottom Silkscreen

PRIMARY SIDE

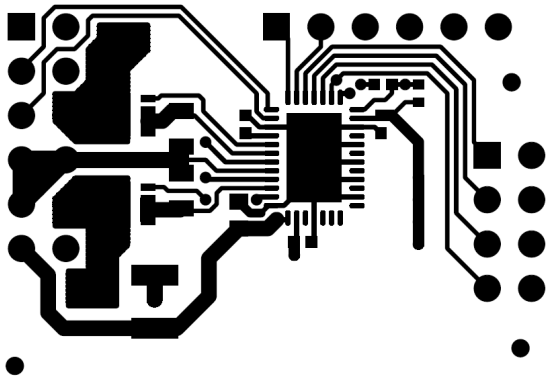


Figure 4.3. Top Layer

SECONDARY SIDE

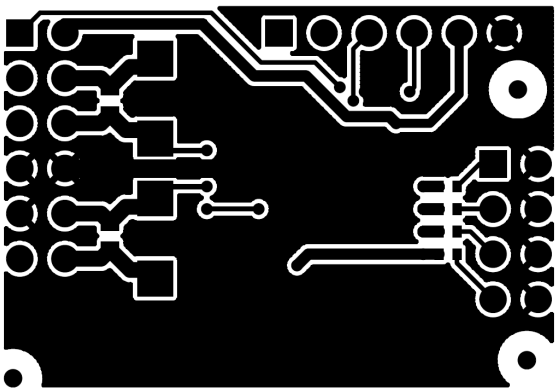


Figure 4.4. Bottom Layer

Baseboard Layout

PRIMARY SILKSCREEN

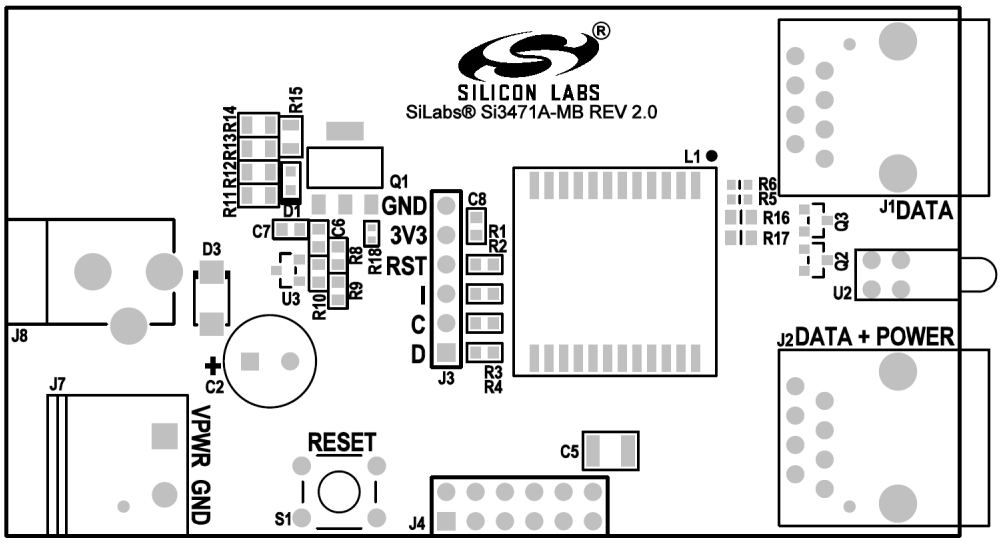


Figure 4.5. Top Silkscreen

PRIMARY SIDE

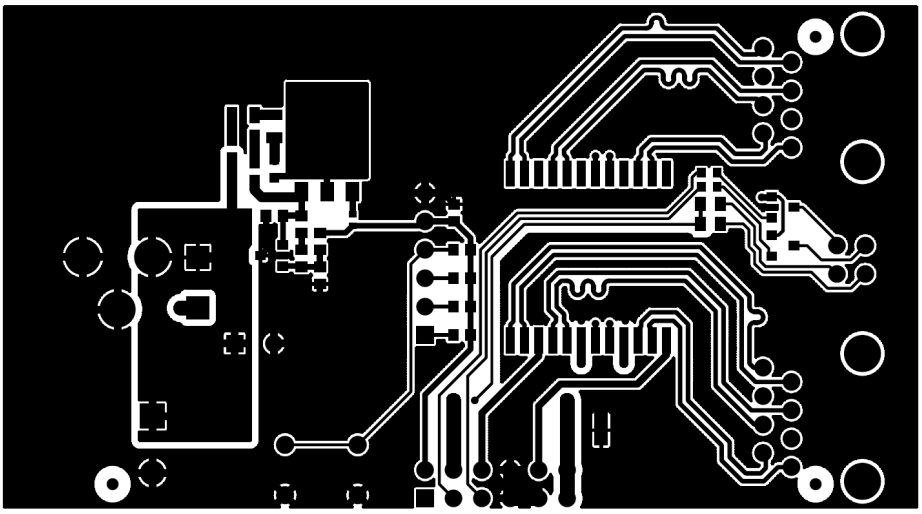


Figure 4.6. Top Layer

SECONDARY SIDE

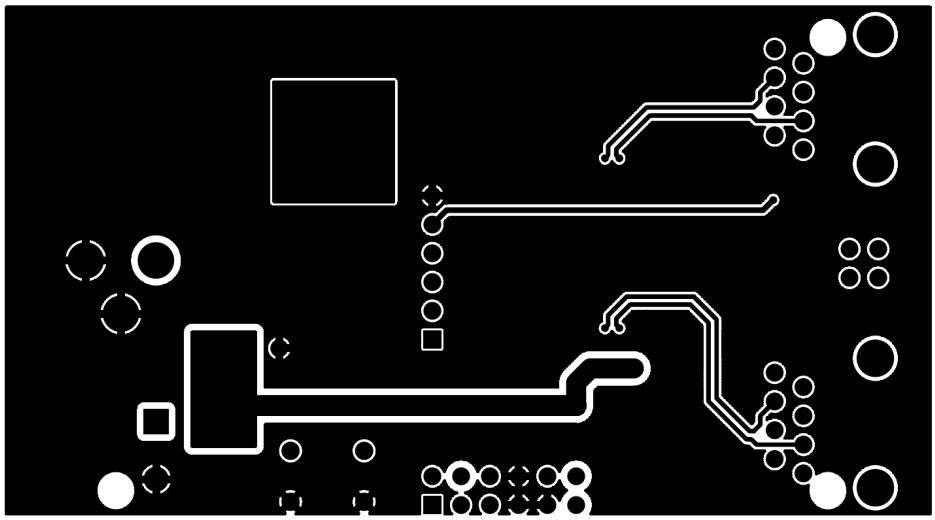


Figure 4.7. Bottom Layer

5. Bill of Materials

Table 5.1. Si3471 Daughtercard Bill of Materials

Ref	Qty	Value	PCB Footprint	Mfr	Mfr Part Number
C3	1	4.7 µF	C1210	TDK	C3225X7S2A475M200AB
C11	1	0.1 µF	C0402	Venkel	C0402X7R100-104K
C12	1	0.1 µF	C0402	Venkel	C0402X7R100-104K
C14	1	0.1 µF	C0402	Venkel	C0402X7R100-104K
C15	1	0.1 µF	C0402	Venkel	C0402X7R100-104K
C20	1	0.1 µF	C0603	Venkel	C0603X7R101-104K
C21	1	0.1 µF	C0603	Venkel	C0603X7R101-104K
C22	1	0.1 µF	C0603	Venkel	C0603X7R101-104K
D1	1	SMAJ58A	DO-214AC	Littelfuse	SMAJ58A
D2	1	SMAJ58A	DO-214AC	Littelfuse	SMAJ58A
J1	1	HEADER 4X2	CONN-2X4	Samtec	TSW-104-08-T-D
J3	1	CONN SOCKET 6x1	CONN-1X6	Samtec	SSQ-106-23-F-S
J4	1	CONN SOCKET 6x2	CONN2X6-SKT	Samtec	SSQ-106-23-F-D
PCB1	1	Si3471A-DC-EVB-Rev2.0	N/A	Silicon Labs	Si3471A-DC-EVB-Rev2.0
Q1	1	PSMN040	LFPAK33	Nexperia	PSMN040-100MSE
Q3	1	PSMN040	LFPAK33	Nexperia	PSMN040-100MSE
R1	1	0.255	R0805	KOA Speer Electronics	SR732ATTDR255F
R2	1	0.255	R0805	KOA Speer Electronics	SR732ATTDR255F
R20	1	10 kΩ	R0402	Venkel	CR0402-16W-103J
R21	1	10 kΩ	R0402	Venkel	CR0402-16W-103J
R22	1	10 kΩ	R0402	Venkel	CR0402-16W-103J
R23	1	10 kΩ	R0402	Venkel	CR0402-16W-103J
R24	1	10 kΩ	R0402	Venkel	CR0402-16W-103J
U1	1	Si3471A	QFN38N5X7P0.5	Silicon Labs	Si3471-A-A01-IM

Table 5.2. Si3471 Motherboard Bill of Materials

Ref	Qty	Value	PCB Footprint	Mfr	Mfr Part Number
C2	1	33 µF	C3.5X8MM-RAD	ECA2AM330	Panasonic
C5	1	4.7 µF	C1210	C3225X7S2A475M200AB	TDK
C6	1	2.2 nF	C0603	C0603X7R160-222K	Venkel
C7	1	47 nF	C0603	C0603X7R160-473M	Venkel
C8	1	1 µF	C0603	C0603X7R160-105K	Venkel
R19	1	0	R0603	CR0603-16W-000	Venkel
D3	1	SMAJ58A	DO-214AC	SMAJ58A	Littelfuse
JP1	1	PLUG		1757019	Phoenix Contact
J1,J2	2	RJ-45	RJ45-95001	095501-2881	MOLEX
J3	1	HEADER 6x1	CONN-1X6	TSW-106-14-F-S	Samtec
J4	1	HEADER 6x2	CONN-2X6	TSW-106-14-F-D	Samtec
J7	1	CONN TRBLK 2	CONN-TB-1757242	1757242	Phoenix Contact
J8	1	POWER JACK	CONN-3-PWR-CLIFF	FC681465P	Cliff Electronic
L1	1	GJ2042Q	ETH1-460L	GJ2042Q	Mentech
		WA8704-ALD		WA8704-ALD	Coilcraft
PCB1	1	Si3471A-MB-EVB-Rev2.0	N/A	Si3471A-MB-EVB-Rev2.0	Silicon Labs
Q1	1	BCP56-16	SOT223-BCE	BCP56-16	On Semiconductor
Q2,Q3	2	MMBTA06LT1	SOT23-BEC	MMBTA06LT1	On Semi
R1, R3, R4	3	1 kΩ	R0603	CR0603-10W-1001F	Venkel
R2	1	10 kΩ	R0603	CR0603-10W-1002F	Venkel
R5, R6	2	511 Ω	R0603	CR0603-10W-5110F	Venkel
R8	1	4.12 kΩ	R0603	CR0603-10W-4121F	Venkel
R9	1	2.49 kΩ	R0603	CR0603-16W-2491F	Venkel
R10	1	1 kΩ	R0603	CR0603-16W-1001F	Venkel
R11	1	75 kΩ	R0805	CR0805-8W-7502F	Venkel
R12, R13, R14, R15	4	140 Ω	R0805	CR0805-8W-1400F	Venkel
R16, R17	2	4.12 kΩ	R0805	CR0805-8W-4121F	Venkel
R18	1	5.11 Ω	R0402	CR0402-16W-5R11F	Venkel
SF1, SF2, SF3, SF4	4	BUMPER	RUBBER_FOOT_SMALL	SJ61A6	3M
S1	1	MOMENTARY	SW4N6.5X4.5-PB	EVQ-PAC04M	PANASONIC CORP
U2	1	GREEN	LED-DUAL-RT	WP934EB/2GD	Kingbright
U3	1	TLV431	TLV431-DBZ	TLV431BCDBZR	TI

6. Design and Layout Checklist

Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

7. Sifos Test Report

The table below shows the test results of the Sifos Technologies 802.3bt 4Pr Conformance Test Suite version 5.1.0n. All tests pass. However, Sifos had not yet added weighting to each test, leaving the calculated Sifos Interop Index to report "#DIV/0!".

Table 7.1. PSE Conformance Test Suite

Chassis ID: 10.11.13.80 TestLoop: 1	PSA-3000 Ports		Min	Max	Average	LowLi-mit	P/F	HighLi-mit	P/F
	1-1	Units							
Test: det_v									
Open_Circuit_Voc_A=	8.7	V	8.7	8.7	8.7	0	Pass	30	Pass
Open_Circuit_Voc_B=	8.6	V	8.6	8.6	8.6	0	Pass	30	Pass
Backoff_Voltage_A=	0.1	V	0.1	0.1	0.1	0	Pass	2.8	Pass
Backoff_Voltage_B=	0.1	V	0.1	0.1	0.1	0	Pass	2.8	Pass
Backoff_Voltage_Ss=	0.1	V	0.1	0.1	0.1	0	Pass	2.8	Pass
Max_Det_Step_V_A=	8.16	V	8.16	8.16	8.16	3.8	Pass	10	Pass
Max_Det_Step_V_B=	8.14	V	8.14	8.14	8.14	3.8	Pass	10	Pass
Min_Det_Step_V_A=	4.07	V	4.07	4.07	4.07	2.8	Pass	9	Pass
Min_Det_Step_V_B=	4.05	V	4.05	4.05	4.05	2.8	Pass	9	Pass
Det_Step_Changes_A=	2	****	2	2	2	1	Pass	9	Pass
Det_Step_Changes_B=	2	****	2	2	2	1	Pass	9	Pass
Min_Step_DV_A=	4.02	V	4.02	4.02	4.02	1	Pass	7.2	Pass
Min_Step_DV_B=	4.01	V	4.01	4.01	4.01	1	Pass	7.2	Pass
Pre-Det_CC_Step_V_A=	0	V	0	0	0	0	Pass	10	Pass
Pre-Det_CC_Step_V_B=	0	V	0	0	0	0	Pass	10	Pass
Test: det_cc									
Presumed_CC_DET_SEQ=	1	****	1	1	1	0	Pass	3	Pass
Conn_Chk_SS_V_A=	7.47	V	7.47	7.47	7.47	2.8	Pass	10	Pass
Conn_Chk_SS_V_B=	4.37	V	4.37	4.37	4.37	2.8	Pass	10	Pass
Conn_Chk_DS_V_A=	7.52	V	7.52	7.52	7.52	2.8	Pass	10	Pass
Conn_Chk_DS_V_B=	4.08	V	4.08	4.08	4.08	2.8	Pass	10	Pass
High_Signature_CC_A=	1	****	1	1	1	1	Pass	1	Pass
High_Signature_CC_B=	1	****	1	1	1	1	Pass	1	Pass
4Pair_Start_Fail=	0	****	0	0	0	0	Pass	0	Pass
Test: det_i									
Isc_Init_A=	2.62	mA	2.62	2.62	2.62	0	Pass	5	Pass
Isc_Init_B=	3.28	mA	3.28	3.28	3.28	0	Pass	5	Pass
Isc_Det_A=	2.62	mA	2.62	2.62	2.62	0	Pass	5	Pass
Isc_Det_B=	3.28	mA	3.28	3.28	3.28	0	Pass	5	Pass
Det_Slew_A=	0.0524	V/µs	0.0524	0.0524	0.0524	0	Pass	0.1	Pass

Chassis ID: 10.11.13.80 TestLoop: 1	PSA-3000 Ports		Min	Max	Average	LowLi-mit	P/F	HighLi-mit	P/F
	1-1	Units							
Det_Slew_B=	0.0656	V/µs	0.0656	0.0656	0.0656	0	Pass	0.1	Pass
Test: det_range									
Rgood_Max_Single=	28	kΩ	28	28	28	27	Pass	32	Pass
Rgood_Min_Single=	17	kΩ	17	17	17	16	Pass	19	Pass
Cgood_Max_Single=	0.1	µF	0.1	0.1	0.1	0	Pass	10	Pass
Rgood_Max_Dual_A=	28	kΩ	28	28	28	27	Pass	32	Pass
Rgood_Max_Dual_B=	28	kΩ	28	28	28	27	Pass	32	Pass
Rgood_Min_Dual_A=	17	kΩ	17	17	17	16	Pass	19	Pass
Rgood_Min_Dual_B=	17	kΩ	17	17	17	16	Pass	19	Pass
Cgood_Max_Dual_A=	0.1	µF	0.1	0.1	0.1	0	Pass	10	Pass
Cgood_Max_Dual_B=	0.1	µF	0.1	0.1	0.1	0	Pass	10	Pass
Test: det_time									
Detect_Time_Tdet_A=	134.8	msec	134.8	134.8	134.8	0	Pass	500	Pass
Detect_Time_Tdet_B=	136.7	msec	136.7	136.7	136.7	0	Pass	500	Pass
Backoff_Time_SS=	390.6	msec	390.6	390.6	390.6	0	Pass	9999	Pass
Det2Det_Time=	41	msec	41	41	41	0	Pass	400	Pass
Test: det_rsource									
PSE_Detect_Source=	0	****	0	0	0	0	Pass	1	Pass
PSE_Source_Zout_A=	0	kΩ	0	0	0	45	Pass	300	Pass
PSE_Source_Zout_B=	0	kΩ	0	0	0	45	Pass	300	Pass
Test: cc_response									
Single_Sig_Response=	1	****	1	1	1	1	Pass	1	Pass
Dual_Sig_Response=	1	****	1	1	1	1	Pass	1	Pass
2Pair_PD_A=	1	****	1	1	1	0	Pass	2	Pass
2Pair_PD_B=	0	****	0	0	0	0	Pass	2	Pass
Test: class_v									
Vclass_max_SS=	18.8	V	18.8	18.8	18.8	15.5	Pass	20.5	Pass
Vclass_min_SS=	17.6	V	17.6	17.6	17.6	15.5	Pass	20.5	Pass
Vmark_SS=	9.4	V	9.4	9.4	9.4	7	Pass	10	Pass
Vreset_SS=	0	V	0	0	0	0	Pass	2.8	Pass
Vclass_max_DSA=	18.8	V	18.8	18.8	18.8	15.5	Pass	20.5	Pass
Vclass_max_DSB=	18.8	V	18.8	18.8	18.8	15.5	Pass	20.5	Pass
Vclass_min_DSA=	17.7	V	17.7	17.7	17.7	15.5	Pass	20.5	Pass
Vclass_min_DSB=	17.7	V	17.7	17.7	17.7	15.5	Pass	20.5	Pass
Vmark_DSA=	9.4	V	9.4	9.4	9.4	7	Pass	10	Pass
Vmark_DSB=	9.4	V	9.4	9.4	9.4	7	Pass	10	Pass

Chassis ID: 10.11.13.80 TestLoop: 1	PSA-3000 Ports		Min	Max	Average	LowLi-mit	P/F	HighLi-mit	P/F
	1-1	Units							
Vreset_DSA=	0	V	0	0	0	-1	Pass	2.8	Pass
Vreset_DSB=	0	V	0	0	0	-1	Pass	2.8	Pass
Test: class_time									
Class_Probe_SS=	1	****	1	1	1	0	Pass	1	Pass
EV_Count_7_SS=	5	Events	5	5	5	1	Pass	5	Pass
Long_EV1_Time_SS=	99.6	msec	99.6	99.6	99.6	88	Pass	105	Pass
Min_Class_EV_Time_SS=	7.8	msec	7.8	7.8	7.8	6	Pass	20	Pass
Max_Class_EV_Time_SS=	13.7	msec	13.7	13.7	13.7	6	Pass	20	Pass
Min_Mark_EV_Time_SS=	7.8	msec	7.8	7.8	7.8	6	Pass	12	Pass
Max_Mark_EV_Time_SS=	9.8	msec	9.8	9.8	9.8	6	Pass	12	Pass
Final_Mark_EV_Time_SS=	11.7	msec	11.7	11.7	11.7	6	Pass	256	Pass
Cl_Prb_Reset_Time_SS=	23.4	msec	23.4	23.4	23.4	15	Pass	10000	Pass
Class_Probe_DA=	1	****	1	1	1	0	Pass	1	Pass
EV_Count_5D_DA=	4	Events	4	4	4	1	Pass	4	Pass
Long_EV1_Time_DA=	97.7	msec	97.7	97.7	97.7	88	Pass	105	Pass
Min_Class_EV_Time_DA=	7.8	msec	7.8	7.8	7.8	6	Pass	20	Pass
Max_Class_EV_Time_DA=	15.6	msec	15.6	15.6	15.6	6	Pass	20	Pass
Min_Mark_EV_Time_DA=	7.8	msec	7.8	7.8	7.8	6	Pass	12	Pass
Max_Mark_EV_Time_DA=	9.8	msec	9.8	9.8	9.8	6	Pass	12	Pass
Final_Mark_EV_Time_DA=	9.7	msec	9.7	9.7	9.7	6	Pass	256	Pass
Cl_Prb_Reset_Time_DA=	25.4	msec	25.4	25.4	25.4	15	Pass	10000	Pass
Class_Probe_DB=	1	****	1	1	1	0	Pass	1	Pass
EV_Count_5D_DB=	4	Events	4	4	4	1	Pass	4	Pass
Long_EV1_Time_DB=	99.6	msec	99.6	99.6	99.6	88	Pass	105	Pass
Min_Class_EV_Time_DB=	7.8	msec	7.8	7.8	7.8	6	Pass	20	Pass
Max_Class_EV_Time_DB=	13.7	msec	13.7	13.7	13.7	6	Pass	20	Pass
Min_Mark_EV_Time_DB=	7.8	msec	7.8	7.8	7.8	6	Pass	12	Pass
Max_Mark_EV_Time_DB=	9.8	msec	9.8	9.8	9.8	6	Pass	12	Pass
Final_Mark_EV_Time_DB=	9.7	msec	9.7	9.7	9.7	6	Pass	256	Pass
Cl_Prb_Reset_Time_DB=	25.4	msec	25.4	25.4	25.4	15	Pass	10000	Pass
Test: class_response									
Class_3_Count=	1	****	1	1	1	1	Pass	1	Pass
Class_4_Count=	3	****	3	3	3	1	Pass	3	Pass
Class_5_Count=	4	****	4	4	4	1	Pass	4	Pass
Class_6_Count=	4	****	4	4	4	1	Pass	4	Pass
Class_7_Count=	5	****	5	5	5	1	Pass	5	Pass

Chassis ID: 10.11.13.80 TestLoop: 1	PSA-3000 Ports		Min	Max	Average	LowLi-mit	P/F	HighLi-mit	P/F
	1-1	Units							
Class_8_Count=	5	****	5	5	5	1	Pass	5	Pass
Class_2D_Count_A=	1	****	1	1	1	1	Pass	3	Pass
Class_2D_Count_B=	1	****	1	1	1	1	Pass	3	Pass
Class_3D_Count_A=	1	****	1	1	1	1	Pass	3	Pass
Class_3D_Count_B=	1	****	1	1	1	1	Pass	3	Pass
Class_4D_Count_A=	3	****	3	3	3	1	Pass	3	Pass
Class_4D_Count_B=	3	****	3	3	3	1	Pass	3	Pass
Class_5D_Count_A=	4	****	4	4	4	1	Pass	4	Pass
Class_5D_Count_B=	4	****	4	4	4	1	Pass	4	Pass
Max_SS_Class=	8	****	8	8	8	3	Pass	8	Pass
Max_DS_Class=	5	****	5	5	5	1	Pass	5	Pass
Init_Grant_Match=	1	****	1	1	1	1	Pass	1	Pass
2-Pair_Pairset=	1	****	1	1	1	0	Pass	2	Pass
PRI_4pr_Pairset=	12	****	12	12	12	1	Pass	12	Pass
Test: class_err									
Class_Ilim_A=	84	mA	84	84	84	51	Pass	100	Pass
Class_Ilim_B=	84.3	mA	84.3	84.3	84.3	51	Pass	100	Pass
Pwr_Cl_52_SS=	0	****	0	0	0	0	Pass	0	Pass
Pwr_Cl_52_DSA=	0	****	0	0	0	0	Pass	0	Pass
Pwr_Cl_52_DSB=	0	****	0	0	0	0	Pass	0	Pass
Mark_Ilim_A=	86	mA	86	86	86	0	Pass	105	Pass
Mark_Ilim_B=	84	mA	84	84	84	0	Pass	105	Pass
Inval_Sig_EV2_SS=	1	****	1	1	1	0	Pass	1	Pass
Inval_Sig_EV4_SS=	0	****	0	0	0	0	Pass	1	Pass
Inval_Sig_EV5_SS=	0	****	0	0	0	0	Pass	1	Pass
Inval_Sig_EV2_DSA=	1	****	1	1	1	0	Pass	1	Pass
Inval_Sig_EV2_DSB=	1	****	1	1	1	0	Pass	1	Pass
Inval_Sig_EV4_DSA=	1	****	1	1	1	0	Pass	1	Pass
Inval_Sig_EV4_DSB=	1	****	1	1	1	0	Pass	1	Pass
Test: pwrup_time									
Pwr_On_Time_Tpon_SS=	331.2	msec	331.2	331.2	331.2	0	Pass	400	Pass
Pwr_On_Time_Tpon_DSA=	311.7	msec	311.7	311.7	311.7	0	Pass	400	Pass
Pwr_On_Time_Tpon_DSB=	311.7	msec	311.7	311.7	311.7	0	Pass	400	Pass
Pwrup_Rise_Time_A=	327	µs	327	327	327	15	Pass	50000	Pass
Pwrup_Rise_Time_B=	328	µs	328	328	328	15	Pass	50000	Pass
Pwr_Stagger_Time_SS4=	69.5	msec	69.5	69.5	69.5	-1	Pass	75	Pass

Chassis ID: 10.11.13.80 TestLoop: 1	PSA-3000 Ports		Min	Max	Average	LowLi-mit	P/F	HighLi-mit	P/F
	1-1	Units							
Pwr_Stagger_Time_SS5=	0	msec	0	0	0	0	Pass	75	Pass
Pwr_Stagger_Time_DS=	349.5	msec	349.5	349.5	349.5	0	Pass	1000	Pass
Test: pwrup_inrush									
Iinrush_min_Class_3=	417	mA	417	417	417	400	Pass	9999	Pass
Iinrush_min_Class_5=	836.5	mA	836.5	836.5	836.5	400	Pass	9999	Pass
Iinrush_min_Class_7=	836.6	mA	836.6	836.6	836.6	800	Pass	9999	Pass
Iinrush_min_Class_1D_A=	417.4	mA	417.4	417.4	417.4	400	Pass	9999	Pass
Iinrush_min_Class_1D_B=	417	mA	417	417	417	400	Pass	9999	Pass
Iinrush_4P_max_Class_3=	417.7	mA	417.7	417.7	417.7	0	Pass	450	Pass
Iinrush_4P_max2_Class_5=	837.3	mA	837.3	837.3	837.3	0	Pass	900	Pass
Iinrush_4P_max2_Class_7=	837.5	mA	837.5	837.5	837.5	0	Pass	900	Pass
Iinrush_2P_max_Class_3=	417.4	mA	417.4	417.4	417.4	0	Pass	450	Pass
Iinrush_2P_max2_Class_7=	418.8	mA	418.8	418.8	418.8	0	Pass	600	Pass
Iinrush_2p_max_Cl_1D_A=	418	mA	418	418	418	0	Pass	450	Pass
Iinrush_2p_max_Cl_1D_B=	417.7	mA	417.7	417.7	417.7	0	Pass	450	Pass
Tinrush_minPr_Class_3=	69.34	msec	69.34	69.34	69.3	50	Pass	75	Pass
Tinrush_maxPr_Class_3=	69.34	msec	69.34	69.34	69.3	50	Pass	75	Pass
Tinrush_minPr_Class_7=	69.34	msec	69.34	69.34	69.3	50	Pass	75	Pass
Tinrush_maxPr_Class_7=	69.34	msec	69.34	69.34	69.3	50	Pass	75	Pass
Tinrush_Class_1D_A=	72.47	msec	72.47	72.47	72.5	50	Pass	75	Pass
Tinrush_Class_1D_B=	72.07	msec	72.07	72.07	72.1	50	Pass	75	Pass
Delay_Inrush_Class_7=	69.34	msec	69.34	69.34	69.3	50	Pass	75	Pass
Delay_Inrush_Class_2D_A=	72.07	msec	72.07	72.07	72.1	50	Pass	75	Pass
Delay_Inrush_Class_2D_B=	72.47	msec	72.47	72.47	72.5	50	Pass	75	Pass
45ms_Pwr_Stat_Class_7=	1	****	1	1	1	1	Pass	1	Pass
45ms_Pwr_Stat_Class_2D_A=	1	****	1	1	1	1	Pass	1	Pass
45ms_Pwr_Stat_Class_2D_B=	1	****	1	1	1	1	Pass	1	Pass
Vinrush_Class_2D_A=	31.2	V	31.2	31.2	31.2	30	Pass	60	Pass
Vinrush_Class_2D_B=	31.1	V	31.1	31.1	31.1	30	Pass	60	Pass
Test: pwron_v									
Vpse_Max_Alt_A=	56.05	V	56.05	56.05	56.05	52	Pass	57	Pass
Vpse_Max_Alt_B=	56.1	V	56.1	56.1	56.1	52	Pass	57	Pass
Vpse_Min_Alt_A=	54.9	V	54.9	54.9	54.9	52	Pass	57	Pass
Vpse_Min_Alt_B=	54.88	V	54.88	54.88	54.88	52	Pass	57	Pass
Vport_PSE_diff=	50	mV	50	50	50	0	Pass	150	Pass
V_ripple_A=	7	mVp-p	7	7	7	0	Pass	500	Pass

Chassis ID: 10.11.13.80 TestLoop: 1	PSA-3000 Ports		Min	Max	Average	LowLi-mit	P/F	HighLi-mit	P/F
	1-1	Units							
V_ripple_B=	5	mVp-p	5	5	5	0	Pass	500	Pass
V_noise_A=	6	mVp-p	6	6	6	0	Pass	200	Pass
V_noise_B=	14	mVp-p	14	14	14	0	Pass	200	Pass
V_trans_A=	54.832	V	54.832	54.832	54.832	52	Pass	57	Pass
V_trans_B=	54.784	V	54.784	54.784	54.784	52	Pass	57	Pass
Test: pwron_pwrcap									
pwron_pwrcap=	-1	****	-1	-1	-1	0	Pass	1	Pass
Test: pwron_maxi									
pwron_maxi=	-1	****	-1	-1	-1	0	Pass	1	Pass
Test: pwron_overld									
pwron_overld=	-1	****	-1	-1	-1	0	Pass	1	Pass
Test: mps_dc_valid									
mps_dc_valid=	-1	****	-1	-1	-1	0	Pass	1	Pass
Test: mps_dc_pwrdn									
mps_dc_pwrdn=	-1	****	-1	-1	-1	0	Pass	1	Pass
Test: pwrdn_overld									
pwrdn_overld=	-1	****	-1	-1	-1	0	Pass	1	Pass
Test: pwrdn_time									
pwrdn_time=	-1	****	-1	-1	-1	0	Pass	1	Pass
Test: pwrdn_v									
pwrdn_v=	-1	****	-1	-1	-1	0	Pass	1	Pass
Test Port Model Number:	3202								
Test Port Hardware Version:	8								
Test Port Firmware Version:	4.14								