



SKYWORKS®

Si53313

DUAL 1:5 LOW-JITTER, ANY-FORMAT BUFFER/ LEVEL TRANSLATOR (<1.25 GHz)

Features

- 2 independent banks of 5x differential outputs
- Ultra-low additive jitter: 45 fs rms
- Wide frequency range: dc to 1.25 GHz
- Any-format input with pin selectable output formats: LVPECL, Low Power LVPECL, LVDS, CML, HCSL, LVCMOS
- Asynchronous output enable
- Low output-output skew: <70 ps
- Output clock division: /1, /2, /4 (dc to 725 MHz for /2 and /4)
- Independent V_{DD} and V_{DDO} : 1.8/2.5/3.3 V
- Excellent power supply noise rejection (PSRR)
- Small size: 44-QFN (7 mm x 7 mm)
- RoHS compliant, Pb-free
- Industrial temperature range: -40 to +85 °C

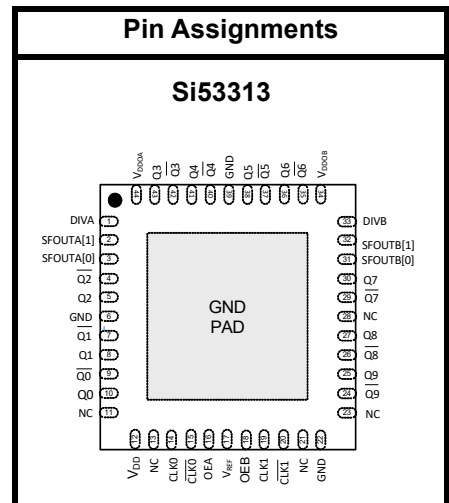
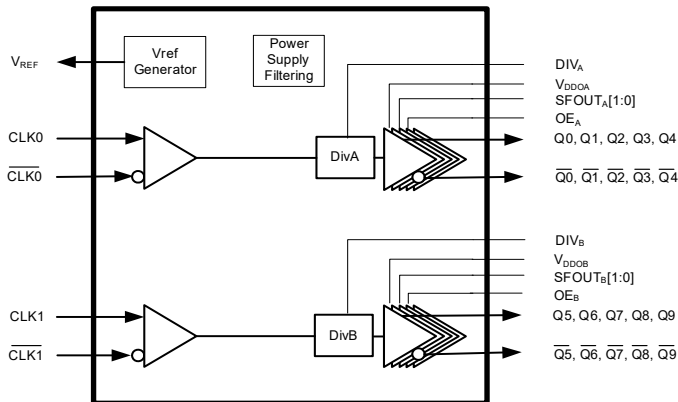
Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

Description

The Si53313 is an ultra low jitter dual 1:5 differential buffer with pin-selectable output clock signal format and divider selection. The Si53313 utilizes Skyworks Solutions' advanced CMOS technology to fanout clocks from dc to 1.25 GHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53313 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments. Independent core and output bank supply pins provide integrated level translation without the need for external circuitry.

Functional Block Diagram



Patents pending

TABLE OF CONTENTS

| Section | Page |
|--|-----------|
| 1. Electrical Specifications | 3 |
| 2. Functional Description | 11 |
| 2.1. Universal, Any-Format Input | 11 |
| 2.2. Input Bias Resistors | 13 |
| 2.3. Voltage Reference (VREF) | 13 |
| 2.4. Universal, Any-Format Output Buffer | 14 |
| 2.5. Flexible Output Divider | 15 |
| 2.6. Output Enable Logic | 15 |
| 2.7. Power Supply (VDD and VDDOX) | 15 |
| 2.8. Output Clock Termination Options | 16 |
| 2.9. AC Timing Waveforms | 19 |
| 2.10. Typical Phase Noise Performance | 20 |
| 2.11. Input Mux Noise Isolation | 23 |
| 2.12. Power Supply Noise Rejection | 23 |
| 3. Pin Description: 44-Pin QFN | 24 |
| 4. Ordering Guide | 27 |
| 5. Package Outline | 28 |
| 5.1. 7x7 mm 44-QFN Package Diagram | 28 |
| 6. PCB Land Pattern | 30 |
| 6.1. 7x7 mm 44-QFN Package Land Pattern | 30 |
| 7. Top Marking | 31 |
| 7.1. Si53313 Top Marking | 31 |
| 7.2. Top Marking Explanation | 31 |
| Document Change List | 32 |
| Contact Information | 33 |

1. Electrical Specifications

Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|------------|----------------------------------|------|-----|------|------|
| Ambient Operating Temperature | T_A | | -40 | — | 85 | °C |
| Supply Voltage Range* | V_{DD} | LVDS, CML | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | LVPECL, low power LVPECL, LVCMOS | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | HCSL | 2.97 | 3.3 | 3.63 | V |
| Output Buffer Supply Voltage* | V_{DDOX} | LVDS, CML, LVCMOS | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | LVPECL, low power LVPECL | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | HCSL | 2.97 | 3.3 | 3.63 | V |

***Note:** Core supply V_{DD} and output buffer supplies V_{DDOX} are independent. LVCMOS clock input is not supported for $V_{DD} = 1.8V$ but is supported for LVCMOS clock output for $V_{DDOX} = 1.8V$. LVCMOS outputs at 1.5V and 1.2V can be supported via a simple resistor divider network. See “2.8.1. LVCMOS Output Termination To Support 1.5 V and 1.2 V”

Table 2. Input Clock Specifications

($V_{DD} = 1.8V \pm 5\%$, $2.5V \pm 5\%$, or $3.3V \pm 10\%$, $T_A = -40$ to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------|---|---------------------|-----|---------------------|------|
| Differential Input Common Mode Voltage | V_{CM} | $V_{DD} = 2.5V \pm 5\%$, $3.3V \pm 10\%$ | 0.05 | — | — | V |
| Differential Input Swing (peak-to-peak) | V_{IN} | | 0.2 | — | 2.2 | V |
| LVCMOS Input High Voltage | V_{IH} | $V_{DD} = 2.5V \pm 5\%$, $3.3V \pm 10\%$ | $V_{DD} \times 0.7$ | — | — | V |
| LVCMOS Input Low Voltage | V_{IL} | $V_{DD} = 2.5V \pm 5\%$, $3.3V \pm 10\%$ | — | — | $V_{DD} \times 0.3$ | V |
| Input Capacitance | C_{IN} | CLK0 and CLK1 pins with respect to GND | — | 5 | — | pF |

Table 3. DC Common Characteristics

($V_{DD} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|--|----------------------|---------------------|----------------------|------------|
| Supply Current | I_{DD} | | — | 65 | 100 | mA |
| Output Buffer Supply Current (Per Clock Output) @100 MHz | I_{DDOX} | LVPECL (3.3 V) | — | 35 | — | mA |
| | | Low Power LVPECL (3.3 V) | — | 35 | — | mA |
| | | LVDS (3.3 V) | — | 20 | — | mA |
| | | CML (3.3 V) | — | 30 | — | mA |
| | | HCSL, 100 MHz, 2 pF load (3.3 V) | — | 35 | — | mA |
| | | CMOS (1.8 V, SFOUT = Open/0), per output, $C_L = 5\text{ pF}$, 200 MHz | — | 5 | — | mA |
| | | CMOS (2.5 V, SFOUT = Open/0), per output, $C_L = 5\text{ pF}$, 200 MHz | — | 8 | — | mA |
| | | CMOS (3.3 V, SFOUT = 0/1), per output, $C_L = 5\text{ pF}$, 200 MHz | — | 15 | — | mA |
| Voltage Reference | V_{REF} | V_{REF} pin ($-500\text{ }\mu\text{A} < I_{REF} < 500\text{ }\mu\text{A}$) | — | $V_{DD}/2$ | — | V |
| Input High Voltage | V_{IH} | SFOUTx, DIVx, CLK_SEL, OEx | $0.8 \times V_{DD}$ | — | — | V |
| Input Mid Voltage | V_{IM} | SFOUTx, DIVx 3-level input pins | $0.45 \times V_{DD}$ | $0.5 \times V_{DD}$ | $0.55 \times V_{DD}$ | V |
| Input Low Voltage | V_{IL} | SFOUTx, DIVx, CLK_SEL, OEx | — | — | $0.2 \times V_{DD}$ | V |
| Internal Pull-down Resistor | R_{DOWN} | CLK_SEL, DIVx, SFOUTx, | — | 25 | — | k Ω |
| Internal Pull-up Resistor | R_{UP} | OEx, DIVx, SFOUTx | — | 25 | — | k Ω |

Table 4. Output Characteristics (LVPECL)

($V_{DDOX} = 2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-----------|----------------|--------------------|------|--------------------|------|
| Output DC Common Mode Voltage | V_{COM} | | $V_{DDOX} - 1.595$ | — | $V_{DDOX} - 1.245$ | V |
| Single-Ended Output Swing | V_{SE} | | 0.40 | 0.80 | 1.050 | V |

***Note:** Unused outputs can be left floating. Do not short unused outputs to ground.

Table 5. Output Characteristics (Low Power LVPECL) $(V_{DDOX} = 2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-----------|---|--------------------|------|--------------------|------|
| Output DC Common Mode Voltage | V_{COM} | $R_L = 100\ \Omega$ across Q_n and $\overline{Q_n}$ | $V_{DDOX} - 1.895$ | | $V_{DDOX} - 1.275$ | V |
| Single-Ended Output Swing | V_{SE} | $R_L = 100\ \Omega$ across Q_n and $\overline{Q_n}$ | 0.20 | 0.60 | 0.85 | V |

Table 6. Output Characteristics—CML $(V_{DDOX} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------|----------|--|-----|-----|-----|------|
| Single-Ended Output Swing | V_{SE} | Terminated as shown in Figure 9 (CML termination). | 200 | 400 | 550 | mV |

Table 7. Output Characteristics—LVDS $(V_{DDOX} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|------------|--|------|------|------|------|
| Single-Ended Output Swing | V_{SE} | $R_L = 100\ \Omega$ across Q_N and $\overline{Q_N}$ | 200 | — | 490 | mV |
| Output Common Mode Voltage ($V_{DDO} = 2.5\text{ V}$ or 3.3 V) | V_{COM1} | $V_{DDOX} = 2.38$ to 2.63 V , 2.97 to 3.63 V , $R_L = 100\ \Omega$ across Q_N and $\overline{Q_N}$ | 1.10 | 1.25 | 1.35 | V |
| Output Common Mode Voltage ($V_{DDO} = 1.8\text{ V}$) | V_{COM2} | $V_{DDOX} = 1.71$ to 1.89 V , $R_L = 100\ \Omega$ across Q_N and $\overline{Q_N}$ | 0.85 | 0.97 | 1.25 | V |

Table 8. Output Characteristics—LVCMOS $(V_{DDOX} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------|----------|----------------|------------------------|-----|------------------------|------|
| Output Voltage High | V_{OH} | | $0.75 \times V_{DDOX}$ | — | — | V |
| Output Voltage Low | V_{OL} | | — | — | $0.25 \times V_{DDOX}$ | V |

***Note:** I_{OH} and I_{OL} per the Output Signal Format Table for specific V_{DDOX} and SFOUTx settings.

Table 9. Output Characteristics—HCSL

($V_{DDOX} = 3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------|----------|---------------------------|------|-----|-----|------|
| Output Voltage High | V_{OH} | $R_L = 50\ \Omega$ to GND | 550 | 700 | 900 | mV |
| Output Voltage Low | V_{OL} | $R_L = 50\ \Omega$ to GND | -150 | 0 | 150 | mV |
| Single-Ended Output Swing | V_{SE} | $R_L = 50\ \Omega$ to GND | 450 | 700 | 850 | mV |
| Crossing Voltage | V_C | $R_L = 50\ \Omega$ to GND | 250 | 350 | 550 | mV |

Table 10. AC Characteristics

($V_{DD} = V_{DDOX} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------|---|------|-----|------|------|
| Frequency ¹ | F | LVPECL, low power LVPECL, LVDS, CML, HCSL | dc | — | 1.25 | GHz |
| | | LVC MOS | dc | — | 200 | MHz |
| Duty Cycle ² | D_C | 200 MHz, 20/80% $T_R/T_F < 10\%$ of period (LVC MOS) (12 mA drive) | 40 | 50 | 60 | % |
| | | 20/80% $T_R/T_F < 10\%$ of period (Differential) | 47 | 50 | 53 | % |
| Minimum Input Clock Slew Rate ³ | SR | Required to meet prop delay and additive jitter specifications (20–80%) | 0.75 | — | — | V/ns |
| Output Rise/Fall Time | T_R/T_F | LVDS, 20/80% | — | — | 325 | ps |
| | | LVPECL, 20/80% | — | — | 350 | ps |
| | | HCSL ⁴ , 20/80% | — | — | 280 | ps |
| | | CML, 20/80% | — | — | 350 | ps |
| | | Low-Power LVPECL, 20/80% | — | — | 325 | ps |
| | | LVC MOS 200 MHz, 20/80%, 2 pF load | — | — | 750 | ps |

Notes:

1. Slew rate should be $\geq 30\text{ mV/ns}$.
2. 50% input duty cycle.
3. When using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.
4. HCSL measurements were made with receiver termination. See Figure 9 on page 17.
5. Output to Output skew specified for outputs with an identical configuration.
6. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
7. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} ($3.3\text{ V} = 100\text{ mV}_{PP}$) and noise spur amplitude measured. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for further details.

Table 10. AC Characteristics (Continued) $(V_{DD} = V_{DDOX} = 1.8\text{ V} \pm 5\%, 2.5\text{ V} \pm 5\%, \text{ or } 3.3\text{ V} \pm 10\%, T_A = -40\text{ to } 85\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------|-----------------------------------|------|------|------|------|
| Minimum Input Pulse Width | T_W | | 360 | — | — | ps |
| Propagation Delay | T_{PLH}, T_{PHL} | LVC MOS (12mA drive with no load) | 1250 | 2000 | 2750 | ps |
| | | LVPECL | 600 | 800 | 1000 | ps |
| | | LVDS | 600 | 800 | 1000 | ps |
| Output Enable Time | T_{EN} | F = 1 MHz | — | 2500 | — | ns |
| | | F = 100 MHz | — | 30 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output Disable Time | T_{DIS} | F = 1 MHz | — | 2000 | — | ns |
| | | F = 100 MHz | — | 30 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output to Output Skew ⁵ | T_{SK} | LVC MOS (12 mA drive to no load) | — | 50 | 120 | ps |
| | | LVPECL | — | 35 | 70 | ps |
| | | LVDS | — | 35 | 70 | ps |
| Part to Part Skew ⁶ | T_{PS} | Differential | — | — | 150 | ps |
| Power Supply Noise Rejection ⁷ | PSRR | 10 kHz sinusoidal noise | — | -63 | — | dBc |
| | | 100 kHz sinusoidal noise | — | -62 | — | dBc |
| | | 500 kHz sinusoidal noise | — | -58 | — | dBc |
| | | 1 MHz sinusoidal noise | — | -55 | — | dBc |

Notes:

1. Slew rate should be ≥ 30 mV/ns.
2. 50% input duty cycle.
3. When using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.
4. HCSL measurements were made with receiver termination. See Figure 9 on page 17.
5. Output to Output skew specified for outputs with an identical configuration.
6. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
7. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} ($3.3\text{ V} = 100\text{ mV}_{PP}$) and noise spur amplitude measured. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for further details.

Table 11. Additive Jitter, Differential Clock Input

| V _{DD} | Input ^{1,2} | | | | Output | Additive Jitter (fs rms, 12 kHz to 20 MHz) ³ | |
|-----------------|----------------------|--------------|---|---------------------------------------|--------|--|-----|
| | Freq (MHz) | Clock Format | Amplitude V _{IN} (Single-Ended, Peak-to-Peak) | Differential 20%-80% Slew Rate (V/ns) | | Clock Format | Typ |
| 3.3 | 725 | Differential | 0.15 | 0.637 | LVPECL | 45 | 65 |
| 3.3 | 725 | Differential | 0.15 | 0.637 | LVDS | 50 | 65 |
| 3.3 | 156.25 | Differential | 0.5 | 0.458 | LVPECL | 160 | 185 |
| 3.3 | 156.25 | Differential | 0.5 | 0.458 | LVDS | 150 | 200 |
| 2.5 | 725 | Differential | 0.15 | 0.637 | LVPECL | 45 | 65 |
| 2.5 | 725 | Differential | 0.15 | 0.637 | LVDS | 50 | 65 |
| 2.5 | 156.25 | Differential | 0.5 | 0.458 | LVPECL | 145 | 185 |
| 2.5 | 156.25 | Differential | 0.5 | 0.458 | LVDS | 145 | 195 |

Notes:

1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 2.

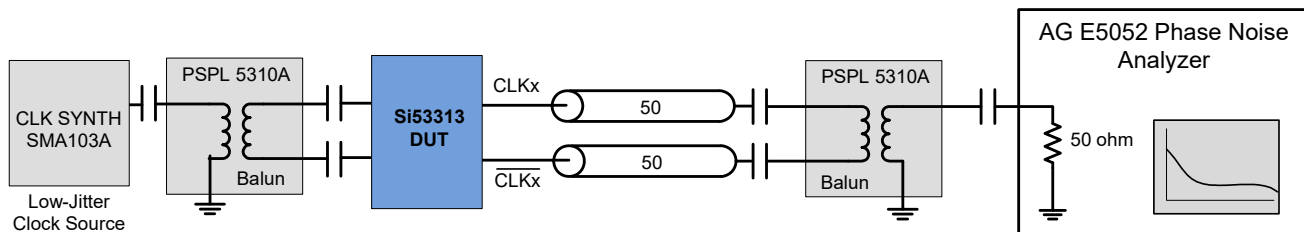


Figure 1. Differential Measurement Method Using a Balun

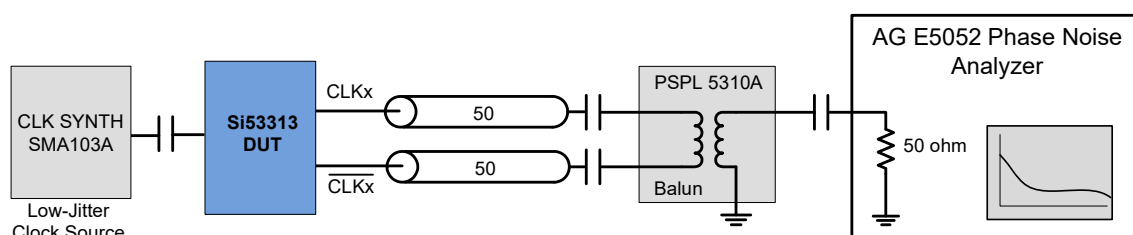
Important: See AN925 for additional information on the dependence of measured additive jitter on the input source jitter.

Table 12. Additive Jitter, Single-Ended Clock Input

| V _{DD} | Input ^{1,2} | | | | Output | Additive Jitter (fs rms, 12 kHz to 20 MHz) ³ | |
|-----------------|----------------------|--------------|---|-----------------------------------|----------------------|---|-----|
| | Freq (MHz) | Clock Format | Amplitude V _{IN} (single-ended, peak to peak) | SE 20%-80% Slew Rate (V/ns) | | Clock Format | Typ |
| 3.3 | 200 | Single-ended | 1.70 | 1 | LVC MOS ⁴ | 120 | 160 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVPECL | 160 | 185 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVDS | 150 | 200 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVC MOS ⁴ | 130 | 180 |
| 2.5 | 200 | Single-ended | 1.70 | 1 | LVC MOS ⁵ | 120 | 160 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVPECL | 145 | 185 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVDS | 145 | 195 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVC MOS ⁵ | 140 | 180 |

Notes:

1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 2.
4. Drive Strength: 12 mA, 3.3 V (SFOUT = 11). LVC MOS jitter is measured single-ended.
5. Drive Strength: 9 mA, 2.5 V (SFOUT = 11). LVC MOS jitter is measured single-ended.

**Figure 2. Single-Ended Measurement Method Using a Balun**

Important: See AN925 for additional information on the dependence of measured additive jitter on the input source jitter.

Table 13. Thermal Conditions

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---------------|----------------|-------|------|
| Thermal Resistance, Junction to Ambient | θ_{JA} | Still air | 49.6 | °C/W |
| Thermal Resistance, Junction to Case | θ_{JC} | Still air | 32.3 | °C/W |

Table 14. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|------------|--|------|-----|----------------|------|
| Storage Temperature | T_S | | -55 | — | 150 | °C |
| Supply Voltage | V_{DD} | | -0.5 | — | 3.8 | V |
| Input Voltage | V_{IN} | | -0.5 | — | $V_{DD} + 0.3$ | V |
| Output Voltage | V_{OUT} | | — | — | $V_{DD} + 0.3$ | V |
| ESD Sensitivity | HBM | HBM, 100 pF, 1.5 k Ω | — | — | 2000 | V |
| ESD Sensitivity | CDM | | — | — | 500 | V |
| Peak Soldering Reflow Temperature | T_{PEAK} | Pb-Free; Solder reflow profile per JEDEC J-STD-020 | — | — | 260 | °C |
| Maximum Junction Temperature | T_J | | — | — | 125 | °C |

Note: Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. Functional Description

The Si53313 is a low-jitter, low-skew dual 1:5 differential output buffer with an independent input for each bank. The device has an any-format input that accepts most common differential or LVCMOS input signals. Each output bank features control pins to select signal format, output enable, output divider setting and LVCMOS drive strength.

2.1. Universal, Any-Format Input

The Si53313 has a universal input stage that enables simple interfacing to a wide variety of clock formats, including LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 15 and 16 summarize the various input ac- and dc-coupling options supported by the device. Figures 3, 4, and 5 show the recommended input clock termination options.

Table 15. LVPECL, LVCMOS, and LVDS

| | LVPECL | | LVCMOS | | LVDS | |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| | AC-Couple | DC-Couple | AC-Couple | DC-Couple | AC-Couple | DC-Couple |
| 1.8 V | N/A | N/A | No | No | Yes | No |
| 2.5/3.3 V | Yes | Yes | No | Yes | Yes | Yes |

Table 16. HCSL and CML

| | HCSL | | CML | |
|-----------|-----------|-----------|-----------|-----------|
| | AC-Couple | DC-Couple | AC-Couple | DC-Couple |
| 1.8 V | No | No | Yes | No |
| 2.5/3.3 V | Yes | Yes | Yes | No |

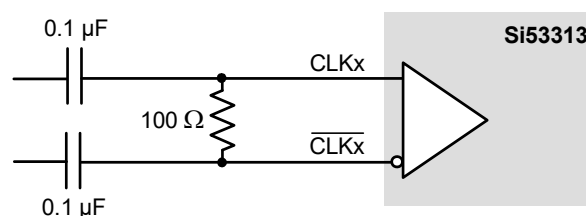


Figure 3. Differential LVPECL, LVDS, CML AC-Coupled Input Termination

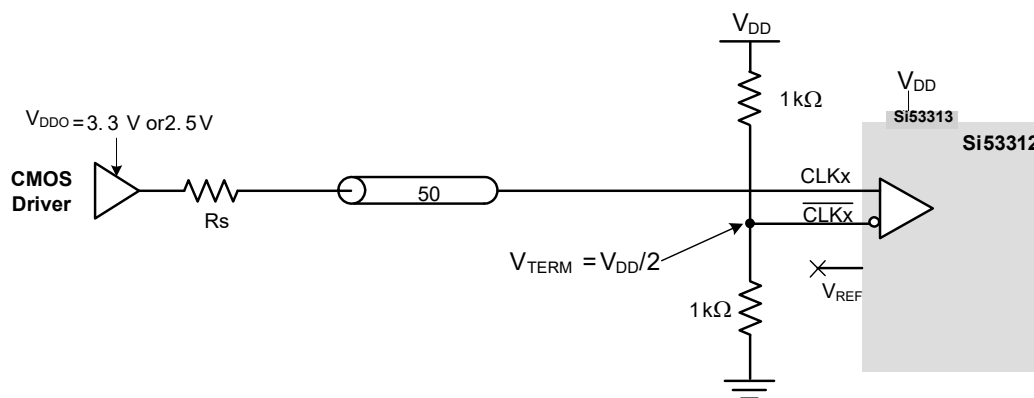
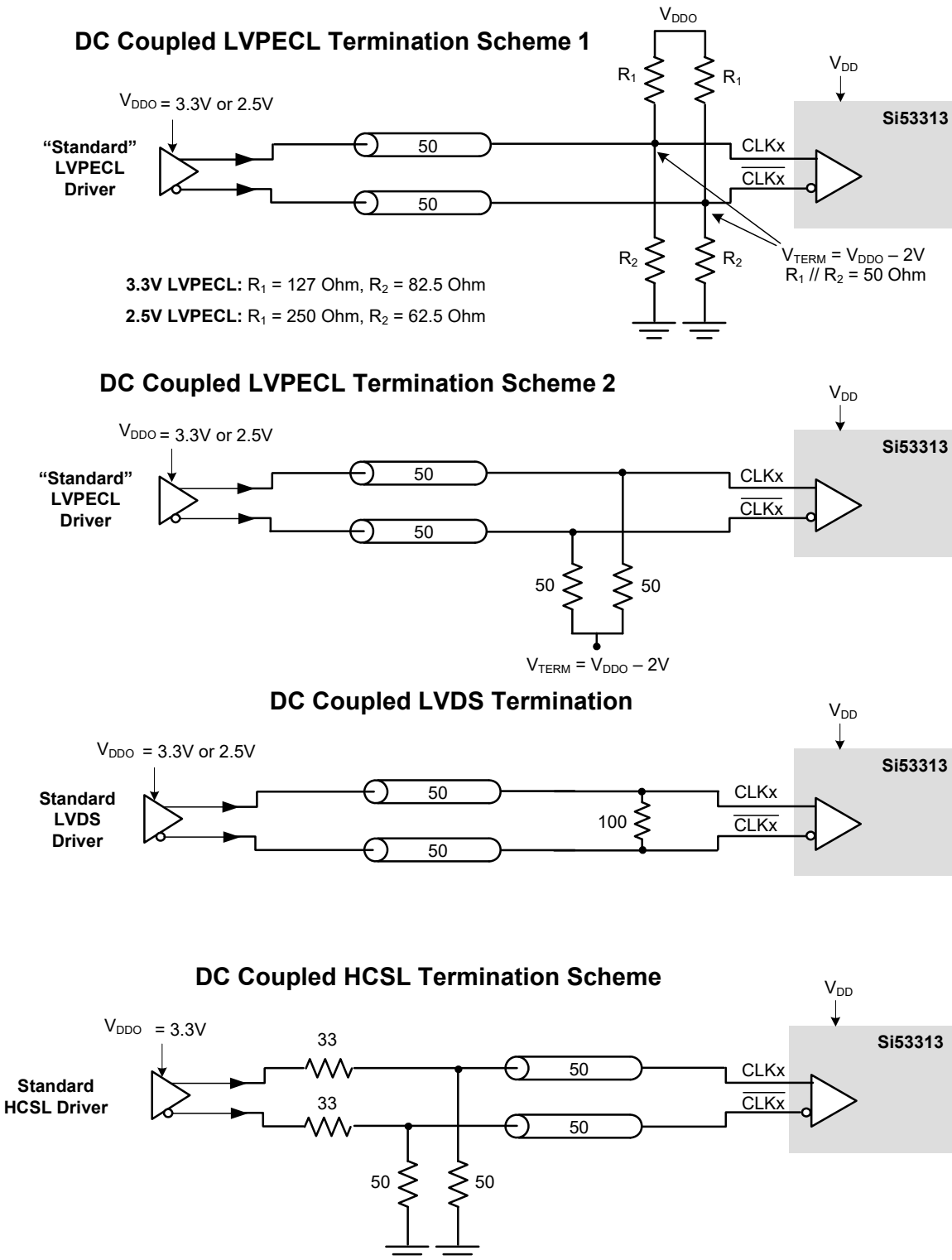


Figure 4. LVCMOS DC-Coupled Input Termination



Note: 33 Ohm series termination is optional depending on the location of the receiver.

Figure 5. Differential DC-Coupled Input Terminations

2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The non-inverting input is biased with a 18.75 kΩ pulldown to GND and a 75 kΩ pullup to V_{DD}. The inverting input is biased with a 75 kΩ pullup to V_{DD}.

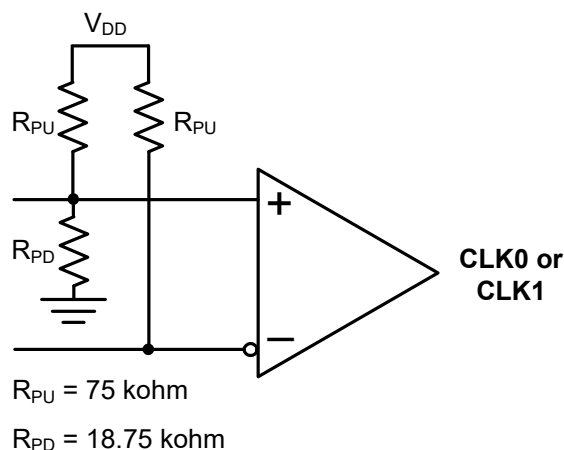


Figure 6. Input Bias Resistors

2.3. Voltage Reference (V_{REF})

The V_{REF} pin can be used to bias the input receiver, as shown in Figure 7 when a single-ended input clock (such as LVCMOS) is used. Note that V_{REF} = V_{DD}/2 and should be compatible with the VCM rating of the single-ended input clock driving the CLK0 or CLK1 inputs. To optimize jitter and duty cycle performance, use the circuit in Figure 4. V_{REF} pin should be left floating when differential clocks are used.

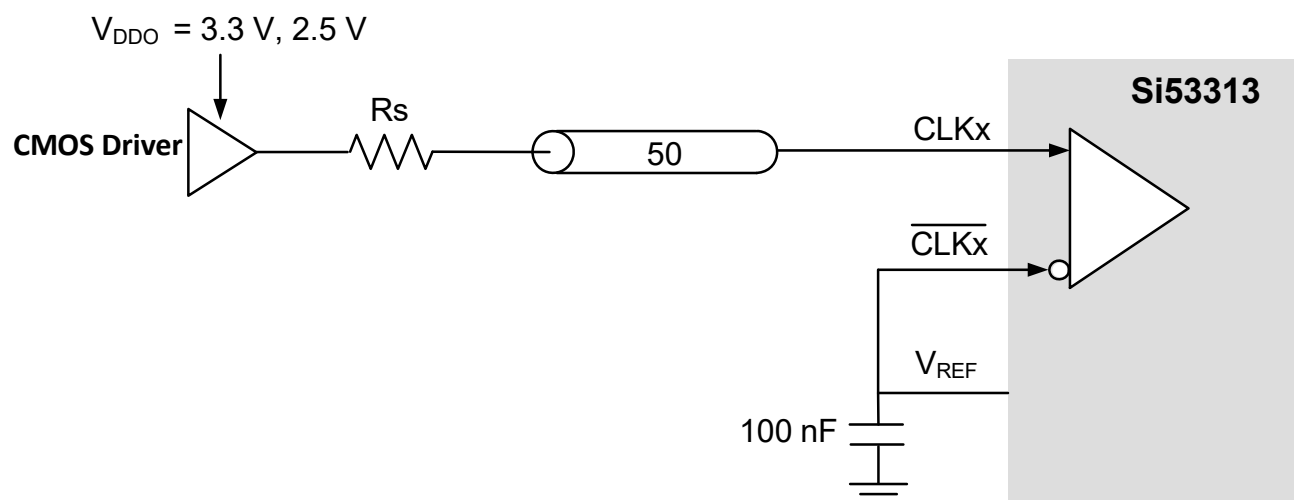


Figure 7. Using Voltage Reference with Single-Ended Input Clock

2.4. Universal, Any-Format Output Buffer

The highly flexible output drivers support a wide range of clock signal formats, including LVPECL, low power LVPECL, LVDS, CML, HCSL, and LVCMOS. SFOUTx[1] and SFOUTx[0] are 3-level inputs that can be pinstrapped to select the Bank A and Bank B clock signal formats independently. This feature enables the device to be used for format/level translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For EMI reduction applications, four LVCMOS drive strength options are available for each V_{DDO} setting.

Table 17. Output Signal Format Selection

| SFOUTx[1] | SFOUTx[0] | $V_{DDOX} = 3.3 \text{ V}$ | $V_{DDOX} = 2.5 \text{ V}$ | $V_{DDOX} = 1.8 \text{ V}$ |
|-----------|-----------|----------------------------|----------------------------|----------------------------|
| Open* | Open* | LVPECL | LVPECL | N/A |
| 0 | 0 | LVDS | LVDS | LVDS |
| 0 | 1 | LVCMOS, 24 mA drive | LVCMOS, 18 mA drive | LVCMOS, 12 mA drive |
| 1 | 0 | LVCMOS, 18 mA drive | LVCMOS, 12 mA drive | LVCMOS, 9 mA drive |
| 1 | 1 | LVCMOS, 12 mA drive | LVCMOS, 9 mA drive | LVCMOS, 6 mA drive |
| Open* | 0 | LVCMOS, 6 mA drive | LVCMOS, 4 mA drive | LVCMOS, 2 mA drive |
| Open* | 1 | LVPECL Low power | LVPECL Low power | N/A |
| 0 | Open* | CML | CML | CML |
| 1 | Open* | HCSL | N/A | N/A |

***Note:** SFOUTx[1:0] are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin is internally biased to $V_{DD}/2$.

2.5. Flexible Output Divider

The Si53313 provides optional clock division in addition to clock distribution. The divider setting for each bank of output clocks is selected via 3-level control pins as shown in the table below. Leaving the DIVx pins open will force a divider value of 1, which is the default mode of operation. Note that when using the on-chip clock divider, a minimum input clock slew rate of 30 mV/ns is required.

Table 18. Divider Selection

| DIVx* | Divider Value | Frequency Range |
|-------|---------------|-----------------|
| Open | ÷1 (default) | dc to 1.25 GHz |
| 0 | ÷2 | dc to 725 MHz |
| 1 | ÷4 | dc to 725 MHz |

***Note:** DIVx are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin is internally biased to $V_{DD}/2$.

2.6. Output Enable Logic

Each 1:5 output has an independent clock input (CLK0/CLK1) and an output enable pin. Table 19 summarizes the input and output clock based upon the state of the input clock and the OE pin.

Table 19. Input Clock and Output Enable Logic

| CLK | OE ¹ | Q ² |
|-----|-----------------|----------------|
| L | H | L |
| H | H | H |
| X | L | L ³ |

Notes:

1. Output enable active high.
2. On the next negative transition of CLK0 or CLK1.
3. Single-ended: Q = low, \bar{Q} = low
Differential: Q = low, \bar{Q} = high.

2.7. Power Supply (V_{DD} and V_{DDOX})

The device includes separate core (V_{DD}) and output driver supplies (V_{DDOX}). This feature allows the core to operate at a lower voltage than V_{DDO} , reducing current consumption in mixed supply applications. The core V_{DD} supports 3.3 V, 2.5 V, or 1.8 V. Each output bank has its own V_{DDOX} supply, supporting 3.3 V, 2.5 V, or 1.8 V as defined in Table 1 on page 3.

2.8. Output Clock Termination Options

The recommended output clock termination options are shown below. Unused output clocks should be left floating.

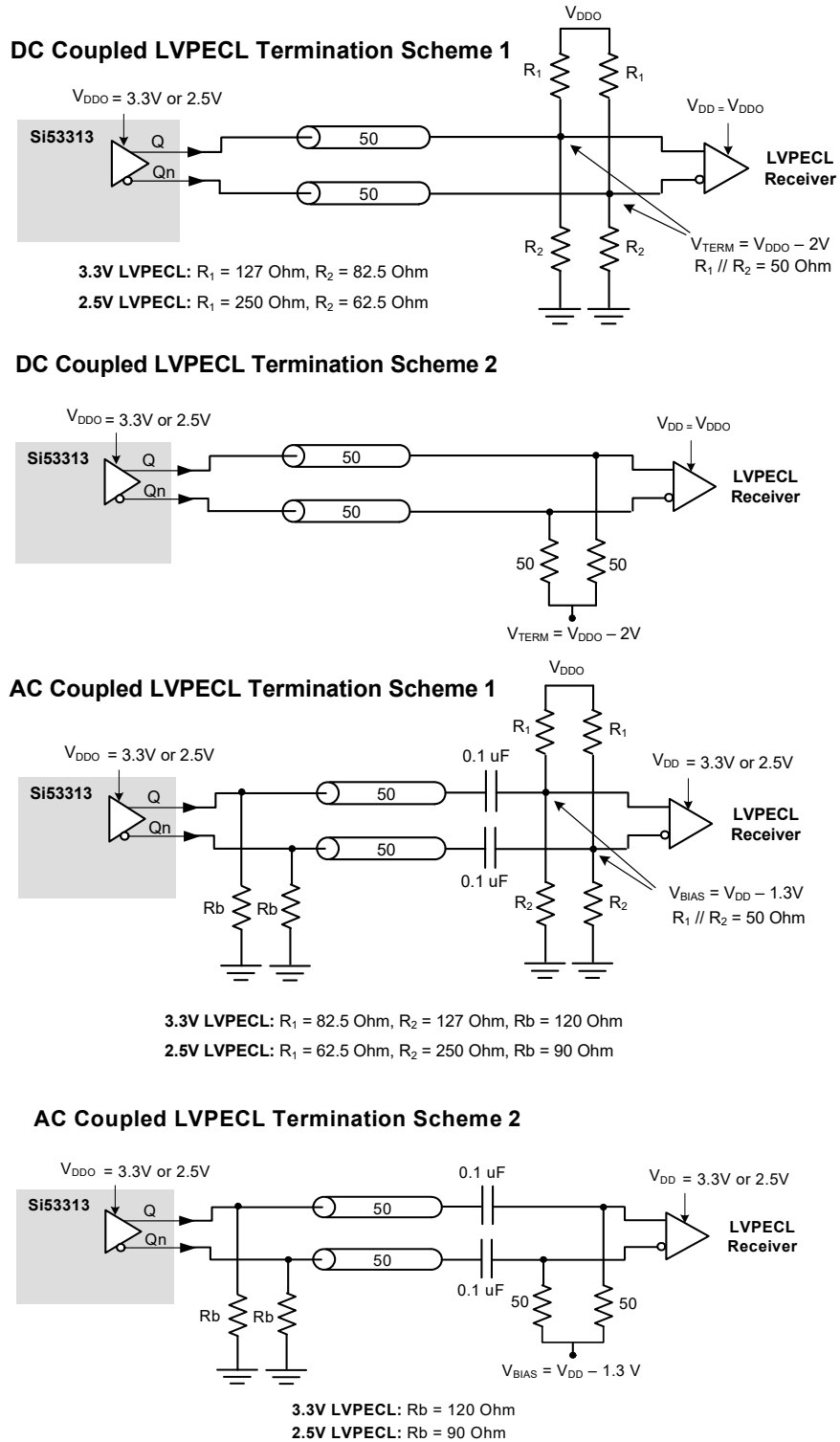
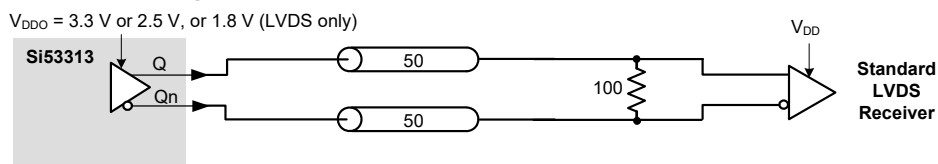
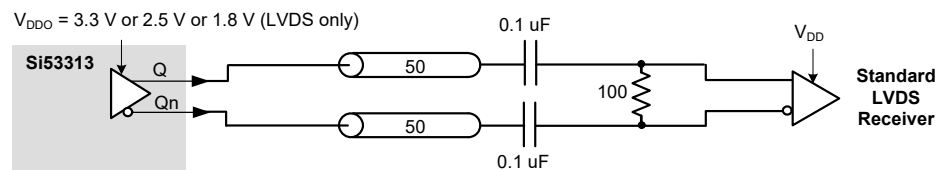


Figure 8. LVPECL Output Termination

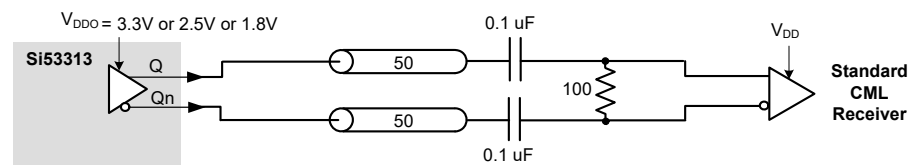
DC Coupled LVDS and Low-Power LVPECL Termination



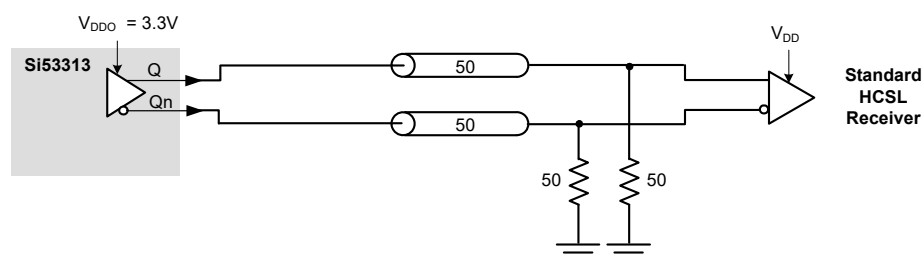
AC Coupled LVDS and Low-Power LVPECL Termination



AC Coupled CML Termination



DC Coupled HCSL Receiver Termination



DC Coupled HCSL Source Termination

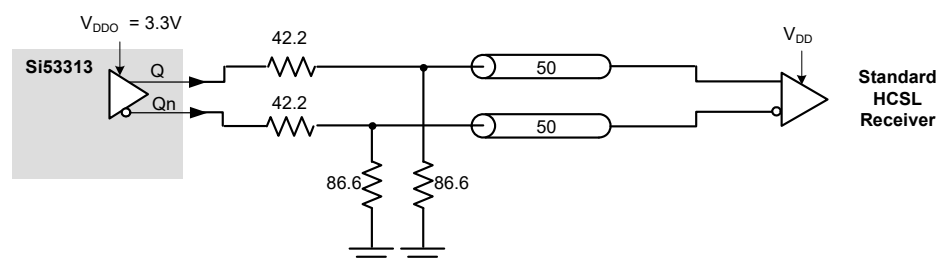


Figure 9. LVDS, CML, HCSL, and Low-Power LVPECL Output Termination

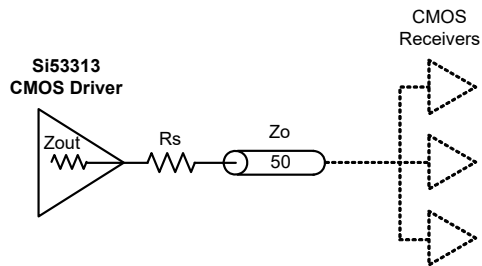


Figure 10. LVC MOS Output Termination

Table 20. Recommended LVC MOS R_S Series Termination

| SFOUTx[1] | SFOUTx[0] | R_S (ohms) | | |
|-----------|-----------|--------------|-------|-------|
| | | 3.3 V | 2.5 V | 1.8 V |
| 0 | 1 | 33 | 33 | 33 |
| 1 | 0 | 33 | 33 | 33 |
| 1 | 1 | 33 | 33 | 0 |
| Open | 0 | 0 | 0 | 0 |

2.8.1. LVC MOS Output Termination To Support 1.5 V and 1.2 V

LVC MOS clock outputs are natively supported at 1.8 V, 2.5 V, and 3.3 V. However, 1.2 V and 1.5 V LVC MOS clock outputs can be supported via a simple resistor divider network that will translate the buffer's 1.8 V output to a lower voltage as shown in Figure 11.

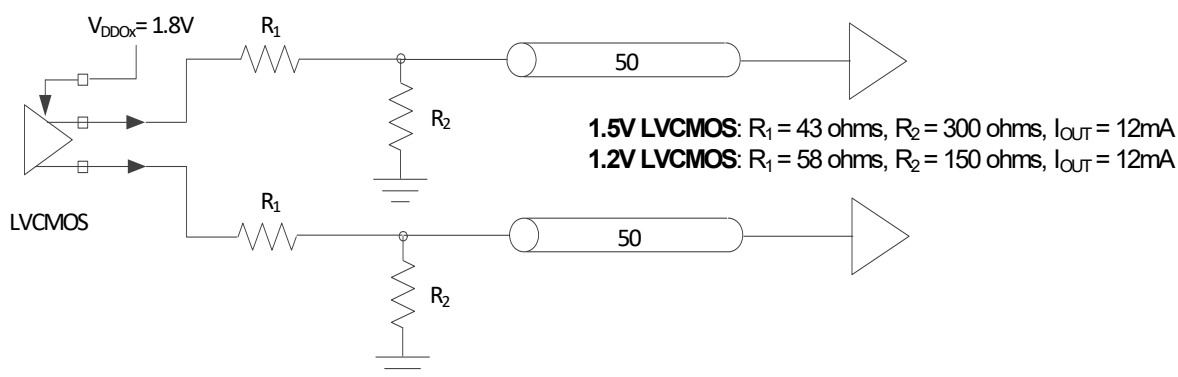


Figure 11. 1.5V and 1.2V LVC MOS Low-Voltage Output Termination

2.9. AC Timing Waveforms

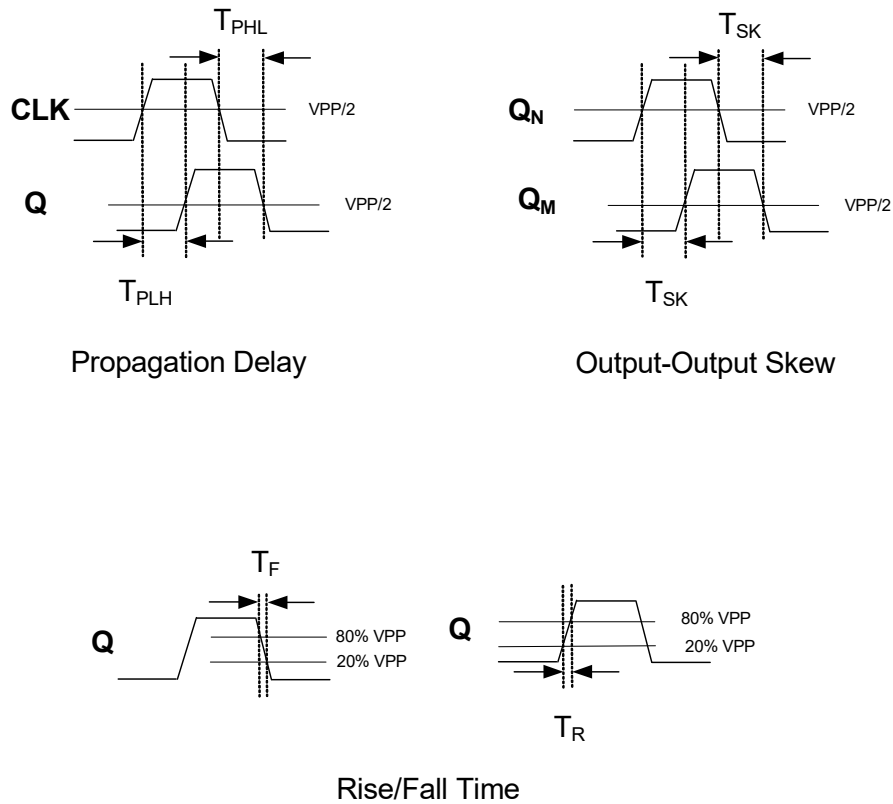


Figure 12. AC Waveforms

2.10. Typical Phase Noise Performance

Each of the following three figures shows three phase noise plots superimposed on the same diagram.

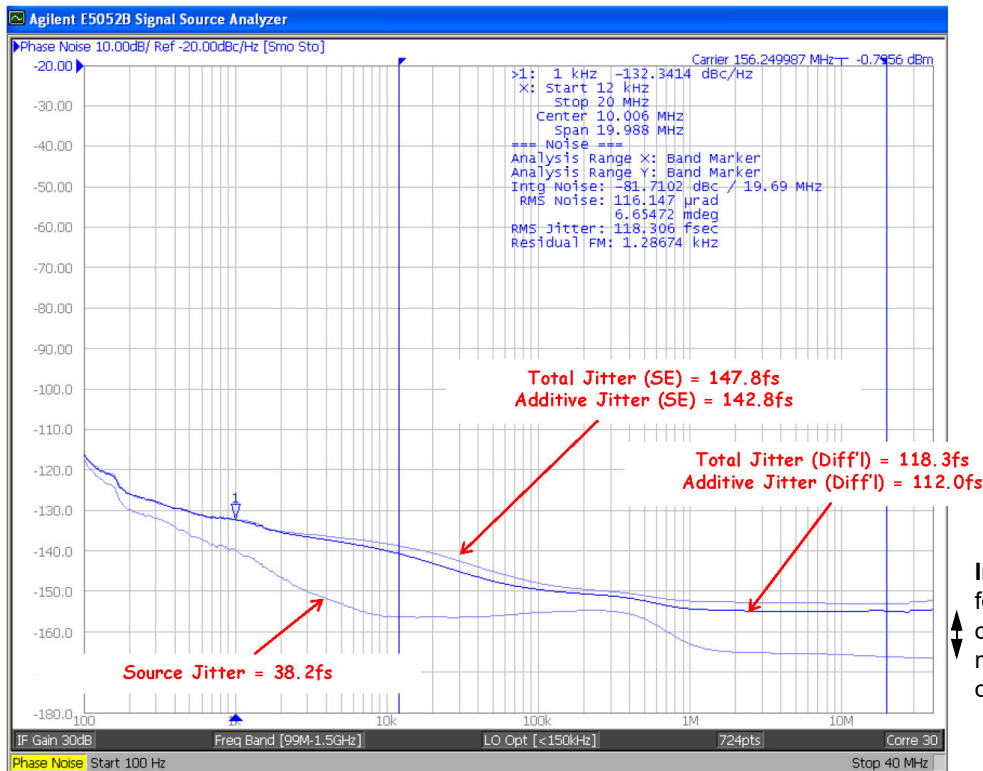
Source Jitter: Reference clock phase noise.

Total Jitter (SE): Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.

Total Jitter (Diff): Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. See Figure 2 on page 9.

Note: To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).



Important: See AN925 for additional information on the dependence of measured additive jitter on the input source jitter.

Figure 13. Source Jitter (156.25 MHz)

Table 21. Source Jitter (156.25 MHz)

| Frequency (MHz) | Diff'l Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Diff'l) (fs) | Additive Jitter (Diff'l) (fs) |
|-----------------|-------------------------------|--------------------|------------------------|---------------------------|----------------------------|-------------------------------|
| 156.25 | 1.0 | 38.2 | 147.8 | 142.8 | 118.3 | 112.0 |

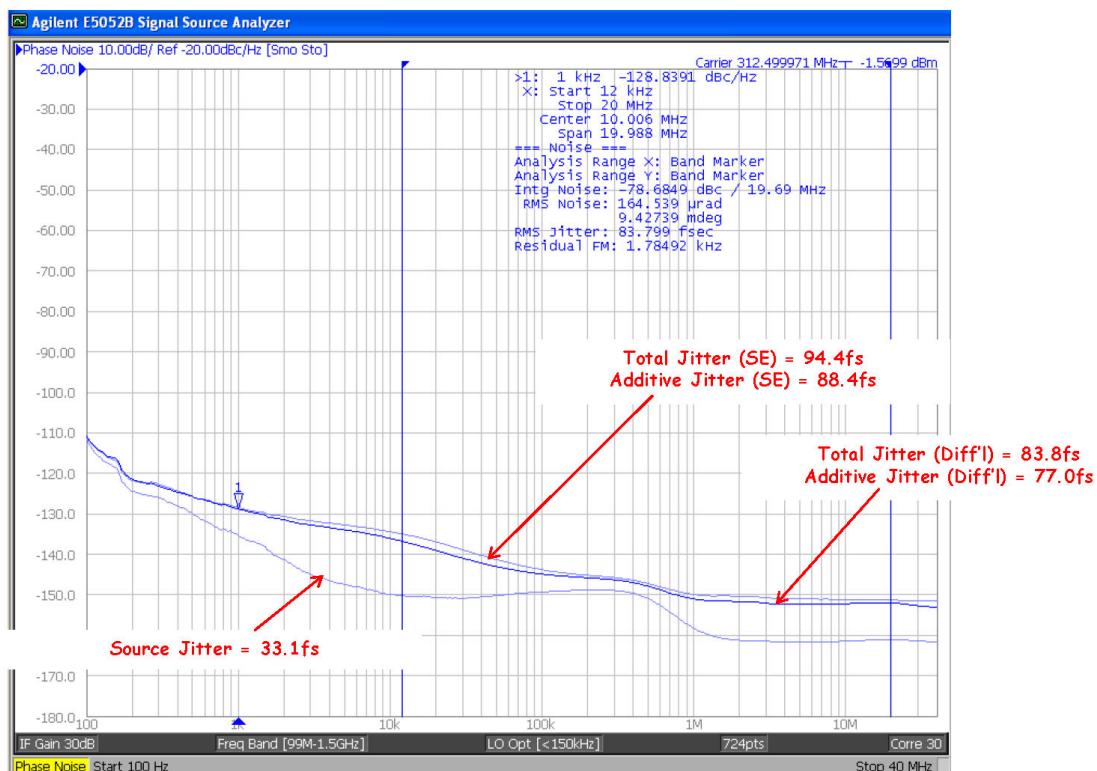


Figure 14. Single-ended Total Jitter (312.5 MHz)

Table 22. Single-ended Total Jitter (312.5 MHz)

| Frequency (MHz) | Diff'l Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Diff'l) (fs) | Additive Jitter (Diff'l) (fs) |
|-----------------|-------------------------------|--------------------|------------------------|---------------------------|----------------------------|-------------------------------|
| 312.5 | 1.0 | 33.10 | 94.39 | 88.39 | 83.80 | 76.99 |

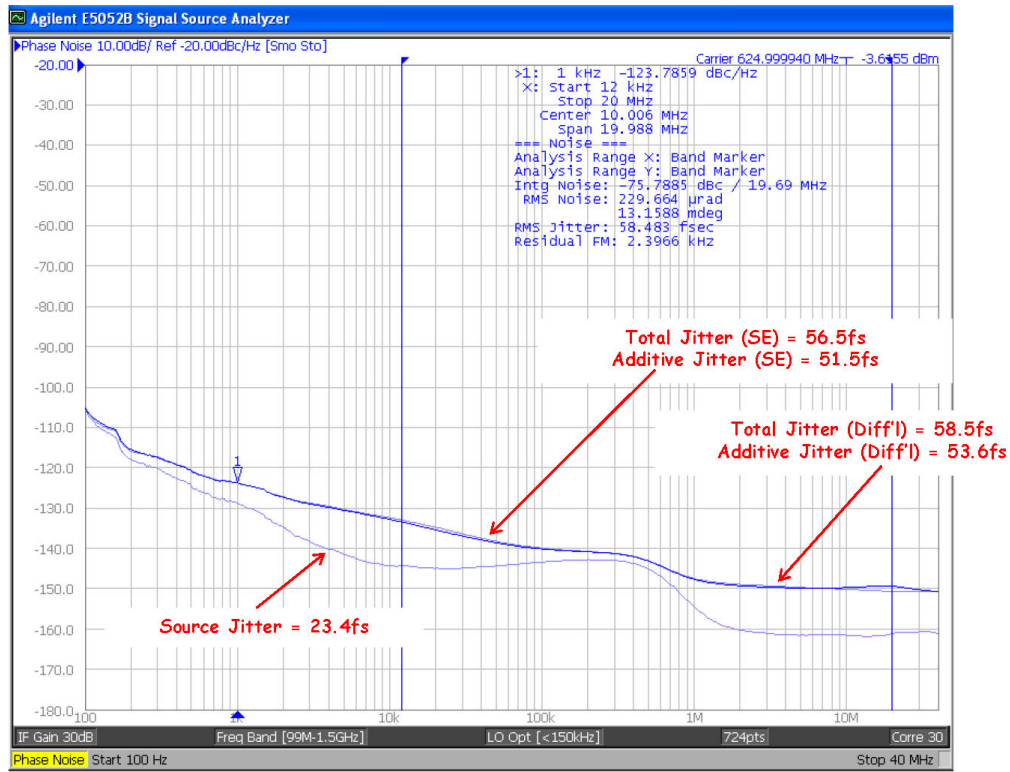


Figure 15. Differential Total Jitter (625 MHz)

Table 23. Differential Total Jitter (625 MHz)

| Frequency (MHz) | Diff'l Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Diff'l) (fs) | Additive Jitter (Diff'l) (fs) |
|-----------------|-------------------------------|--------------------|------------------------|---------------------------|----------------------------|-------------------------------|
| 625 | 1.0 | 23.4 | 56.5 | 51.5 | 58.5 | 53.6 |

2.11. Input Mux Noise Isolation

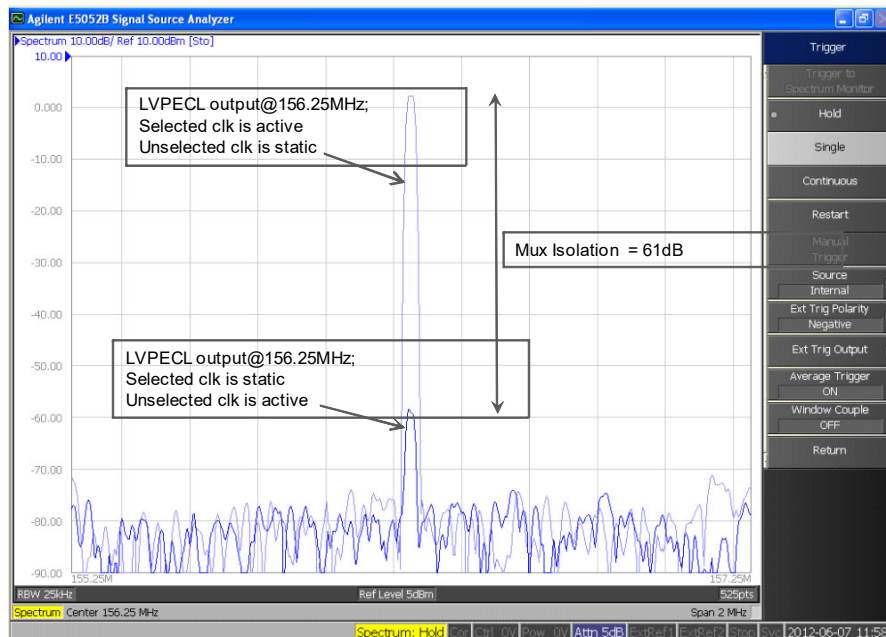


Figure 16. Input Mux Noise Isolation

2.12. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see “AN491: Power Supply Rejection for Low Jitter Clocks”.

3. Pin Description: 44-Pin QFN

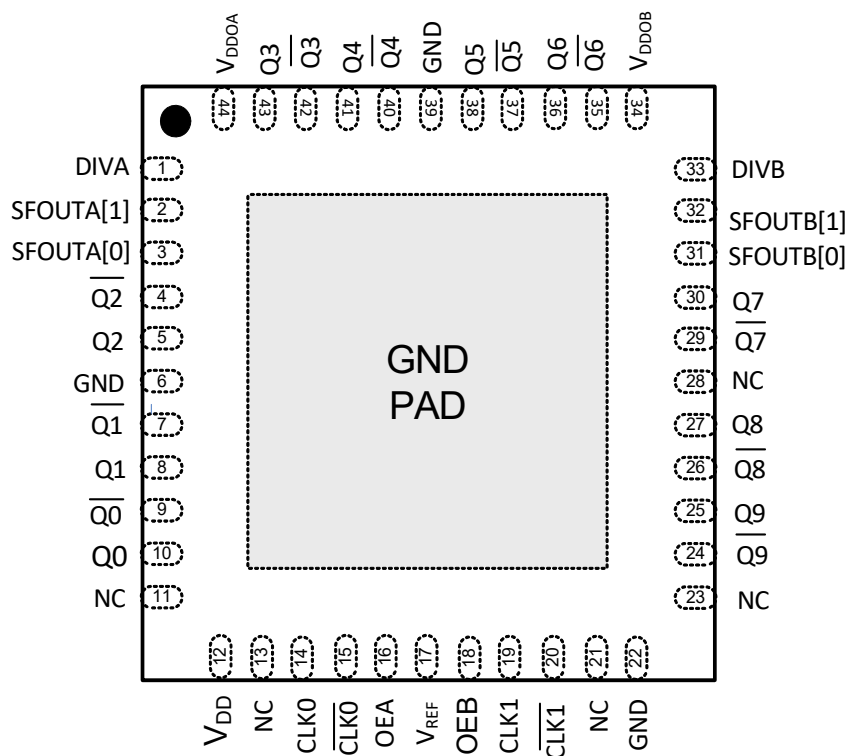


Table 24. Pin Description

| Pin # | Name | Description |
|-------|-----------------|---|
| 1 | DIVA | Output divider control pin for Bank A Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V _{DD} . |
| 2 | SFOUTA[1] | Output signal format control pin for Bank A Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V _{DD} . |
| 3 | SFOUTA[0] | Output signal format control pin for Bank A Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V _{DD} . |
| 4 | $\overline{Q2}$ | Output clock 2 (complement) |
| 5 | Q2 | Output clock 2 |
| 6 | GND | Ground |
| 7 | $\overline{Q1}$ | Output clock 1 (complement) |
| 8 | Q1 | Output clock 1 |

Table 24. Pin Description (Continued)

| Pin # | Name | Description |
|-------|-------------------|--|
| 9 | $\overline{Q0}$ | Output clock 0 (complement) |
| 10 | Q0 | Output clock 0 |
| 11 | NC | No connect |
| 12 | VDD | Core voltage supply Bypass with 1.0 μ F capacitor placed as close to the VDD pin as possible |
| 13 | NC | No connect |
| 14 | CLK0 | Input clock 0 |
| 15 | $\overline{CLK0}$ | Input clock 0 (complement) When the CLK0 is driven by a single-end LVCMOS input, connect CLK0 to VDD/2. |
| 16 | OEA | Output enable—Bank A When OE = high, the Bank A outputs are enabled When OE = low, Q is held low and \overline{Q} is held high for differential formats For LVCMOS, both Q and \overline{Q} are held low when OE is set low OEA contains an internal pull-up resistor |
| 17 | V _{REF} | Reference voltage for single-ended CMOS clocks. V _{REF} is an output voltage and is equal to V _{DD} /2. It can be used to bias the /CLK input for single ended input clocks. See "2.3. Voltage Reference (VREF)" on page 13. |
| 18 | OEB | Output enable—Bank B When OE = high, the Bank B outputs are enabled When OE = low, Q is held low and \overline{Q} is held high for differential formats For LVCMOS, both Q and \overline{Q} are held low when OE is set low OEB contains an internal pull-up resistor. |
| 19 | CLK1 | Input clock 1 |
| 20 | $\overline{CLK1}$ | Input clock 1 (complement) When the $\overline{CLK1}$ is driven by a single-end LVCMOS input, connect $\overline{CLK1}$ to VDD/2. |
| 21 | NC | No connect |
| 22 | GND | Ground |
| 23 | NC | No connect |
| 24 | $\overline{Q9}$ | Output clock 9 (complement) |
| 25 | Q9 | Output clock 9 |
| 26 | $\overline{Q8}$ | Output clock 8 (complement) |
| 27 | Q8 | Output clock 8 |
| 28 | NC | No connect |
| 29 | $\overline{Q7}$ | Output clock 7 (complement) |

Table 24. Pin Description (Continued)

| Pin # | Name | Description |
|---------|-------------------|---|
| 30 | Q7 | Output clock 7 |
| 31 | SFOUTB[0] | Output signal format control pin for Bank B Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V _{DD} . |
| 32 | SFOUTB[1] | Output signal format control pin for Bank B Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V _{DD} . |
| 33 | DIVB | Output divider configuration bit for Bank B Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V _{DD} . |
| 34 | V _{DDOB} | Output Clock Voltage Supply—Bank B (Outputs: Q5 to Q9) Bypass with 1.0 μF capacitor and place close to the V _{DDOB} pin as possible |
| 35 | $\overline{Q6}$ | Output clock 6 (complement) |
| 36 | Q6 | Output clock 6 |
| 37 | $\overline{Q5}$ | Output clock 5 (complement) |
| 38 | Q5 | Output clock 5. |
| 39 | GND | Ground. |
| 40 | $\overline{Q4}$ | Output clock 4 (complement) |
| 41 | Q4 | Output clock 4. |
| 42 | $\overline{Q3}$ | Output clock 3 (complement) |
| 43 | Q3 | Output clock 3 |
| 44 | V _{DDOA} | Output Voltage Supply—Bank A (Outputs: Q0 to Q4) Bypass with 1.0 μF capacitor and place close to the V _{DDOA} pin as possible |
| GND Pad | GND | Ground Pad Power supply ground and thermal relief |

4. Ordering Guide

| Part Number | Package | PB-Free, ROHS-6 | Temperature |
|----------------------------|------------------|-----------------|--------------|
| Si53313-B-GM ¹ | 44-QFN | Yes | -40 to 85 °C |
| Si53301/4-EVB ² | Evaluation Board | Yes | — |

Notes:

1. To buy the Si53313-B-GM, go to <https://www.skyworksinc.com/support-ia#distributors>.
2. The Si53301/4-EVB is used to evaluate the Si53313-B-GM. To buy the Si53301/4-EVB, please go to <https://www.skyworksinc.com/support-ia#distributors>.

5. Package Outline

5.1. 7x7 mm 44-QFN Package Diagram

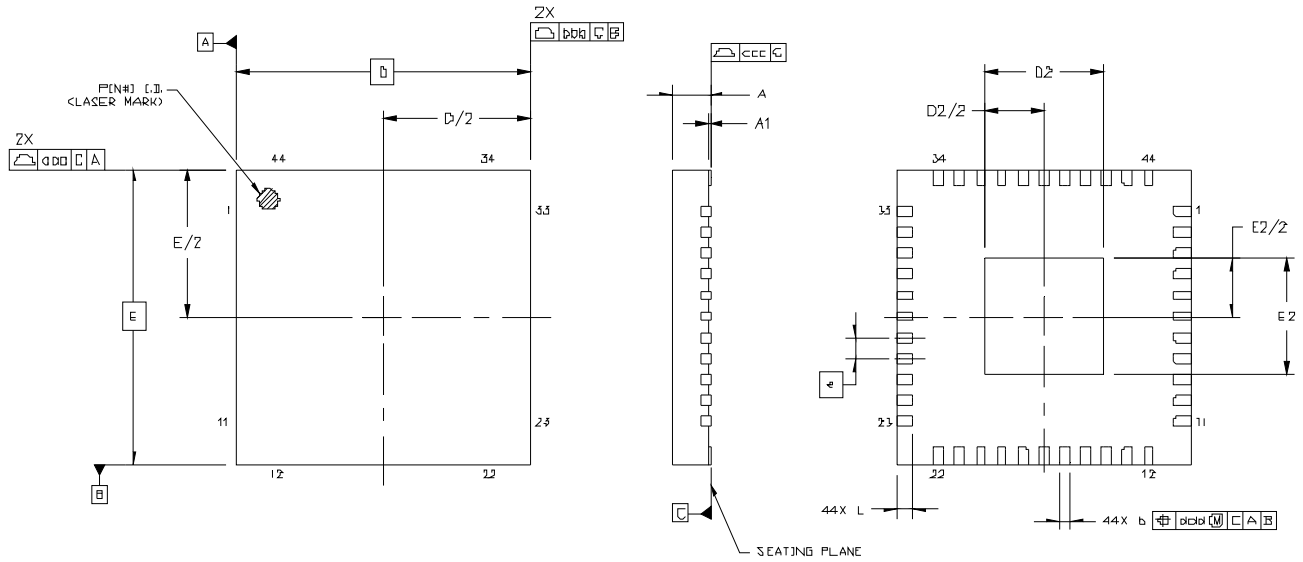


Figure 17. Si53313 7x7 mm 44-QFN Package Diagram

Table 25. Package Diagram Dimensions

| Dimension | Min | Nom | Max |
|---|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 7.00 BSC | | |
| D2 | 2.65 | 2.80 | 2.95 |
| e | 0.50 BSC | | |
| E | 7.00 BSC | | |
| E2 | 2.65 | 2.80 | 2.95 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |
| Notes: | | | |
| <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. This drawing conforms to the JEDEC Solid State Outline MO-220. 4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | | | |

6. PCB Land Pattern

6.1. 7x7 mm 44-QFN Package Land Pattern

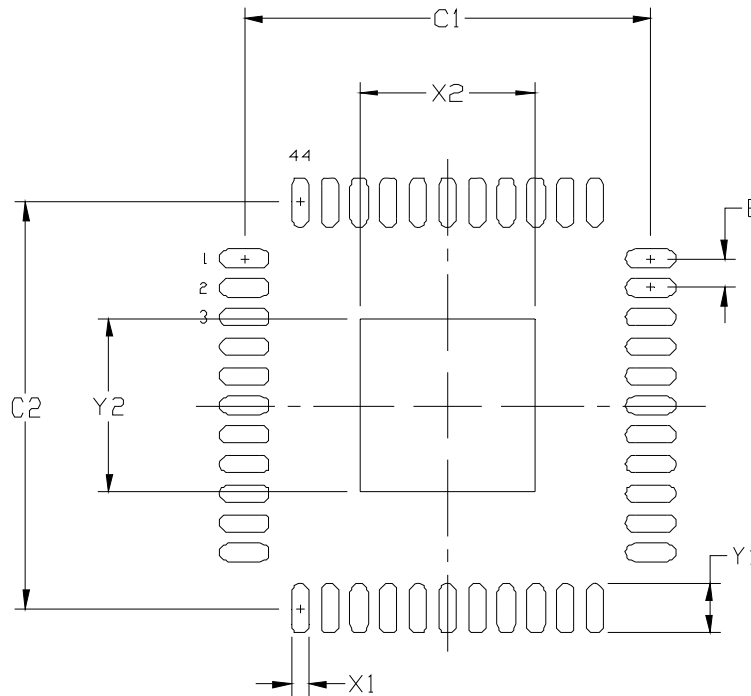


Figure 18. Si53313 7x7 mm 44-QFN Package Land Pattern

Table 26. PCB Land Pattern

| Dimension | Min | Max | Dimension | Min | Max |
|-----------|----------|------|-----------|------|------|
| C1 | 6.80 | 6.90 | X2 | 2.85 | 2.95 |
| C2 | 6.80 | 6.90 | Y1 | 0.75 | 0.85 |
| E | 0.50 BSC | | Y2 | 2.85 | 2.95 |
| X1 | 0.20 | 0.30 | | | |

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

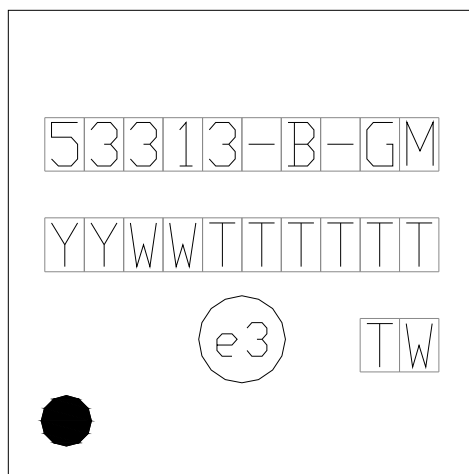
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 1.0 mm square openings on 1.45 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Top Marking

7.1. Si53313 Top Marking



7.2. Top Marking Explanation

| | | |
|------------------------|--|---|
| Mark Method: | Laser | |
| Font Size: | 1.9 Point (26 mils) Right-Justified | |
| Line 1 Marking: | Device Part Number | 53313-B-GM |
| Line 2 Marking: | YY=Year WW=Work Week | Assigned by Assembly Supplier. Corresponds to the year and work week of the mold date. |
| | TTTTTT=Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| Line 3 Marking: | Circle=1.3 mm Diameter Center-Justified | "e3" Pb-Free Symbol |
| | Country of Origin ISO Code Abbreviation | TW |
| Line 4 Marking | Circle = 0.75 mm Diameter Filled | Pin 1 Identification |

DOCUMENT CHANGE LIST

Revision 0.4 to Revision 1.0

- Updated features list.
- Updated tables 1–14 to reflect characterization before Rev 1.0 release.
- Updated sections 2.1, 2.3, 2.4, and 2.7 to add more clarity to description and diagrams.
- Added section 2.8.1 "LVCMOS Output Termination To Support 1.5 V and 1.2 V".
- Update section 2.10 with current phase noise plots.
- Update ordering information and website links.