

Si5340-D EVALUATION BOARD USER'S GUIDE

Description

The Si5340-D-EVB is used for evaluating the Si5340 Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier revision D. The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "SI5340-D-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

Features

- Powered from USB port or external power supply
- Onboard 48 MHz XTAL allows free-run mode of operation on the Si5340 or up to 3 input clocks for synchronous clocking
- Feedback clock input for optional zero delay mode
- ClockBuilder[®] Pro (CBPro) GUI-programmable VDD supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI-programmable VDDO supplies allow each of the 4 outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies.
- Status LEDs for power supplies and control/status signals of Si5340
- SMA connectors for input and output clocks



Si5340-D Evaluation Board

1. Functional Block Diagram

Below is a functional block diagram of the Si5340-D-EB. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See Section "3. Quick Start" or Section "9. Installing ClockBuilder Pro Desktop Software" for more information.





2. Si5340-D-EVB Support Documentation and ClockBuilder Pro Software

All Si5340-D-EVB schematics, BOMs, User's Guides, and software can be found on-line at the following link:

www.skyworksinc.com/en/application-pages/Developers

3. Quick Start

1. Install ClockBuilder Pro desktop software:

www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software

- 2. Connect a USB cable from the Si5340-D-EB to the PC where the software is installed.
- 3. Confirm jumpers are installed as shown in Table 1.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5340-D-EB.
- 6. For Si5340 data sheet go to: www.skyworksinc.com/en/Products/Timing

4. Jumper Defaults

Location	Туре	l = Installed 0 = Open		Location	Туре	l = Installed 0 = Open
JP1	2 pin	I		JP14	2 pin	0
JP2	2 pin	I		JP15	2 pin	0
JP3	2 pin	I		JP16	3 pin	All Open
JP4	2 pin	I		JP17	3 pin	All Open
JP5	3 pin	1 to 2		JP18	2 pin	0
JP6	2 pin	0		JP19	2 pin	0
JP7	2 pin	0		JP20	3 pin	All Open
JP8	2 pin	0		JP21	3 pin	All Open
JP9	2 pin	0		JP22	2 pin	0
JP10	2 pin	0		JP23	2 pin	0
JP11	2 pin	0		JP24	3 pin	All Open
JP12	2 pin	0		JP17	5x2 Hdr	All 5 Installed
JP13	2 pin	0				
*Note: Refer to	the Si534	40-D-EB schematics	for	the functionality a	associated wit	h each jumper.

Table 1. Si5340-D-EB Jumper Defaults*

5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D5	INTRB	Blue	DUT Interrupt
D7	LOLB	Blue	DUT Loss of Lock
D8	LOSXAXBB	Blue	DUT Loss of Reference
D11	+5 V MAIN	Green	Main USB +5 V present
D12	READY	Green	MCU Ready
D13	BUSY	Green	MCU Busy

Table 2. Si5340-D-EB Status LEDs

D11 is illuminated when USB +5V supply voltage is present. D12 and D13 are status LEDs showing on-board MCU activity.



Figure 2. Status LEDs

6. External Reference Input (XA/XB)

An external reference (XTAL) is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. The Si5340-D-EVB can also accommodate an external reference clock instead of a crystal. To evaluate the device with a REFCLK, C93 and C94 must be populated and the XTAL removed (see Figure 3 below). The REFCLK can then be applied to J25 and J26.





7. Clock Input Circuits (INx/INxB and FB_IN/FB_INB)

The Si5340-D-EB has eight SMA connectors (IN0/IN0B – IN2/IN2B and FB_IN/FB_INB) for receiving external clock signals. All input clocks are terminated as shown in Figure 4 below.

Input clocks are ac-coupled and 50 Ω terminated. This represents 4 differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5340 data sheet.



Figure 4. Input Clock Termination Circuit

8. Clock Output Circuits (OUTx/OUTxB)

Each of the eight outputs (four differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in Figure 5 below. The output signal has no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5340-D-EB provides pads for optional output termination resistors and/or low frequency capacitors.

Note: Components with schematic "NI" designation are not normally populated on the Si5340-D-EB and provide locations on the PCB for optional dc/ac terminations by the end user.





9. Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any Windows 7 (or later version) PC, do the following:

1. Go to

www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software

and download ClockBuilder Pro software.

2. Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above. Please follow the instructions as indicated.

10. Using the Si5340-D-EVB

10.1. Connecting the EVB to Your Host PC

Once the ClockBuilder Pro software in installed, connect the PC to the EVB with a USB cable as illustrated in Figure 6.





10.2. Overview of ClockBuilder Pro Applications

The ClockBuilder Pro installer installs two main applications: the ClockBuilder Pro Wizard and the EVB GUI. Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.



Figure 7. Application #1: ClockBuilder Pro Wizard

Use the CBPro Wizard to do the following:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming

CB Si5340A Rev D EV	/B - ClockBuilder Pro					
ile Help						
Info DUT SPI I	DUT Settings Editor	DUT Register Editor	Regulators	All Voltages	GPIO	Status Registers
		Voltage	Curren	t Power	r	
VDD	1.80V 🗧 🖸	Dn V	/ /	۰ ۱	w	Read
VDDA	3.30V	Dn V	/ /	۹ ۱	w	Read
VDDO0	2.50V	Dn V	/ /	۰ ۱	w [Read
VDDO1	2.50V	Off 0 V	/ 0 r	nA 0r	mW [Read
VDDO2	2.50V	Off 0 V	/ 0 r	nA 0r	mW [Read
VDDO3	2.50V	Off 0 V	/ 0 r	nA Or	mW [Read
All Output	Select Voltage	Total	0 1	nA O	w	Read All
Supplies	Power On Po	wer Off	Compare Desig	n Estimates to	Measu	rements

Figure 8. Application #2: EVB GUI

Use the EVB GUI to do the following:

- Download configuration to EVB's DUT (Si5340)
- Control the EVB's regulators
- Monitor voltage, current, and power on the EVB

10.3. Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5340-D-EVB. These workflow scenarios are as follows:

- Workflow Scenario #1: Testing a Skyworks-created default configuration
- Workflow Scenario #2: Modifying the default Skyworks-created device configuration
- Workflow Scenario #3: Testing a user-created device configuration

Each workflow scenario is described in more detail in the following sections.

10.3.1. Workflow Scenario #1: Testing a Skyworks-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows:

1. Once the PC and EVB are connected, launch ClockBuilder Pro by clicking this icon on your PC's desktop:



Figure 9. ClockBuilder Pro Desktop Icon

2. If an EVB is detected, click on the **Open Default Plan** button on the Wizard's main menu. CBPro automatically detects the EVB and device type.



Figure 10. Open Default Plan

3. Once you open the default plan (based on your EVB model number), a popup window appears.

Write Design to EVB? The EVB may be out-of-sync with your design. Would you like to write your design to the EVB? Yes No	CB Cl	ockBuilder Pro v4.1	—		х
	0	Write Design to EVB? The EVB may be out-of-sync with your design. Would your design to the EVB?	ld you li	ke to wr	ite

Figure 11. Write Design to EVB Dialog

4. Select **Yes** to write the default plan to the Si5340 device mounted on your EVB. This ensures the device is completely reconfigured per the Skyworks default plan for the DUT type mounted on the EVB.



Figure 12. Writing Design Status

5. After CBPro writes the default plan to the EVB, click on **Open EVB GUI** as shown in Figure 13.



Figure 13. Open EVB GUI

6. The EVB GUI opens.

Note: All power supplies are set to the values defined in the device's default CBPro project file created by Skyworks, as shown in Figure 14.

CB Si5340A Rev D EV	B - ClockBuilder Pro						
File Help				_			
Info DUT SPI D	OUT Settings Editor	DUT Register Edito	or Regulators	All Voltages	GPIO	Status Registers	
		Voltag	e Currer	nt Powe	r		
VDD	1.80V)n	V	A	w	Read	
VDDA	3.30V)n	V	A 1	w	Read	
VDDO0	2.50V)n	V	A 1	w	Read	
VDDO1	2.50V	Off 0	V 0	mA 0	mW [Read	
VDDO2	2.50V	Off 0	V 0	mA 0	mW 🗌	Read	
VDDO3	2.50V	Off 0	V 0	mA 0	mW [Read	
All Output	Select Voltage	Tota	al O	mA 0	w	Read All	
Supplies	Power On Po	wer Off	Compare Desig	gn Estimates to	Measur	rements	



Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the **Read All** button (the bottom-right of Figure 14) and then reviewing the voltage, current, and power readings for each VDDx supply.

Note: Shutting the VDD and VDDA power supplies "Off" and then "On" will power-down and reset the DUT. Every time you do this, to reload the Skyworks-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select **Write Design to EVB**:



Figure 15. Write Design to EVB

Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Skyworks for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running in free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on **View Design Report** as highlighted in Figure 16.



Figure 16. View Design Report

Si5340-D-EVB

Your configuration's design report appears in a new window, shown in Figure 17. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

Design Report				
** Engineerin	a Mode Design Peno	n+ **		_
rugineer in	B House pesign kepo			
Overview				
	5153404 B			
Part:	515340A Rev	U		
Created By:	ClockBuilde	n Pro v4 1 [2021-09-22]		
Timestamp:	2021-11-12	11:19:22 GMT-05:00		
Decign Rule (hack			
Design noie ei				
Errors:				
- No errors				
Warnings:				
- No warnings				
Device Grade				
evice drade				
laximum Output	t Frequency: 622.0	8 MHz		
requency Synt	tnesis Mode: Fract	10na1		
finimum Base (n orade: A OPN: Si534	0A*		
Base Out	tput Clock	Supported Frequency Synthesis Modes		
PN Grade Fre	equency Range	(Typical Jitter)		
15340A* 100	0 Hz to 1.028 GHz	Integer (< 100 fs) and fractional (< 150 fs)		
i5340B 100	0 Hz to 350 MHz			
i5340C 100	0 Hz to 1.028 GHz	Integer only (< 100 fs)		
15340D 10	0 Hz to 350 MHz			
* Based on you	ur calculated freq	uency plan, a Si5340A grade device is		
required for	your design. See t	he datasheet Ordering Guide for more		
information.				
)esign				
lost Interface	e:			
I/O Power	Supply: VDD (Core)			
SPI Mode: 4	4-Wire s Bange: 116d to 1	19d / 0x74 to 0x77 (selected via A0/A1 pins)		
TEC HUUI CS:	- inter itor co i	The former of the former of the bolist bring to		
inputs:	0-			
- 40 M	nz tal Mode			
TNO: Unuse	ed			
IN1: Unus	ed			
IN2: Unuse	ed			
FB_IN: Unuse	ed			
Outputs:				
00To. 161.1	1328125 MHz			
Enab	led, LVDS 2.5 V			
OUT1: 622.0	08 MHz			
Enab.	led, LVDS 2.5 V			
0012: 218.	/5 mHZ T3*1 / 1			
Enabi	led. IVDS 2.5 V			
			_	
Copy to Clipboa	ard Save Repor	t Ask for Help	Clo	se

Figure 17. Design Report Window

Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

10.3.2. Workflow Scenario #2: Modifying the Default Skyworks-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on Edit Configuration with Wizard.



Figure 18. Edit Configuration with Wizard

You are then taken to the Wizard's step-by-step menus which allow you to change any of the default plan's operating configurations.

ep 1 of 11 - De	sign ID & Notes	Configuring Si5340
Design ID The device has 8 r	egisters, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/r	evision identifier.
Design ID:	5340EVB1 (optional; max 8 characters)	
	The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN	ID7.
Padding Mode:	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pad character).	ded with 0x00 bytes (aka NL
	Space Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be pad	ded with 0x20 bytes (space
Design Notes	character).	
Design Notes Enter anything you While the text is w	character). u want here. The text is stored in your project file and included in design reports and custom p ord wrapped in reports, you can use newlines to start a new paragraph.	art number datasheet adder
Design Notes Enter anything you While the text is w	character). u want here. The text is stored in your project file and included in design reports and custom p ord wrapped in reports, you can use newlines to start a new paragraph.	art number datasheet adder
Design Notes Enter anything you While the text is w	character). u want here. The text is stored in your project file and included in design reports and custom p rord wrapped in reports, you can use newlines to start a new paragraph.	art number datasheet adder
Design Notes Enter anything you While the text is w	character). u want here. The text is stored in your project file and included in design reports and custom p rord wrapped in reports, you can use newlines to start a new paragraph.	art number datasheet adder
Design Notes Enter anything you While the text is w	character). u want here. The text is stored in your project file and included in design reports and custom p rord wrapped in reports, you can use newlines to start a new paragraph.	art number datasheet adder
Design Notes Enter anything you While the text is w	character). u want here. The text is stored in your project file and included in design reports and custom p ord wrapped in reports, you can use newlines to start a new paragraph.	art number datasheet adder
Design Notes Enter anything you While the text is w	character). u want here. The text is stored in your project file and included in design reports and custom p ord wrapped in reports, you can use newlines to start a new paragraph.	art number datasheet adder

Figure 19. Design Wizard

Note: You can click on the icon on the lower left hand of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on **Write to EVB** to update the DUT to reconfigure your device in real-time. The Design Write status window opens each time you make a change.

Writing Si5	340 Design to EVB	
Address 0x	010B	

Figure 20. Writing Design Status

10.3.3. Workflow Scenario #3: Testing a User-Created Device Configuration

1. To test a previously-created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting **Open Design Project File**.

ClockBuilder Pro Wizzard ClockBuilder Pro Wizzard We Make Timing Simple	SKYWORKS
Work With a Design	Quick Links
Create New Project	Skyworks Timing Solutions
Open Project	Custom Part Number Lookup
Convert Existing Project/NVM File	Applications Documentation 10/40/100G Line Card Whitepaper
ex Open Sample Project	Clock Generators for Cloud Data Centers Optimizing Si534x Jitter Performance
Evaluation Board Detected SIS340A Rev D EVB Open Default Plan EVB GUI	Selecting the registric locks for limiting synchronolization Applications PCIE Gen 4.0 litter Requirements Selecting a PCIE Reference Clock Source Making Accurate Clock litter Measurements
	ClockBuilder Pro Documentation
	CBPIn Overview CBPIn Tools & Support for In-System Programming CLI User's Guide Release Notes
0,	Version 4.1 Built on 9/22/2021

Figure 21. Open Design Project File

2. Locate your CBPro design file in the Windows file browser.

CB Open CBPro Project File					×
← → × ↑ 📙 « Jui <u>-</u>	Tharwal > User_Guide_Images_Rebr	anding > Si5340	✓ O Search Si5	340	Q
Organize 👻 New folder				•== •	•
Quick access Desktop Documents Downloads Pictures COGSWORTH_FW-{ Keysight_25Oct21 Si5340	Name A Si5340-RevD-5340EVB1-Project	Date modified	I Type :26 Skyworks Timi	Size	10 KB
Transfer_data					
🛄 This PC	Figure 22. Bro	wse for Proiec	t Files		

3. Select Yes when the Write Design to EVB popup appears.



Figure 23. Write Design to EVB Dialog

4. The progress bar is launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

10.4. Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting **Export** as shown in Figure 24.

CB Si5340 EVB Default Configuration - ClockBuilder Pro	- 🗆 X
ClockBuilder Pro v4.1 🍫 (standard frequency planner) (no se	tting overrides) SKYWORKS
Design Dashboard 🔻	Configuring Si5340A Rev D
You have made edits to the EVB design. You can also save your new con Design to Project File" link.	figuration to a project file for future use by clicking the "Save
Edit Configuration with Wizard Design ID & Notes · Revision · Host Interface · Input Clocks & ZDM · Input Clock Select · Output Clocks · DCO · Planner · I/O Skew · LOS · INTR	Evaluation Board Detected Si5340A Rev D EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in Clockbuilder Pro at a later time. In engineering mode, you can save this project unencrypted.	Export You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a design report (text) or create a draft datasheet addendum (PDF) for your design.	Documentation Si5341/40 Rev D Family Reference Manual Si5341/40 Rev D Datasheet Si5340 Rev D EVB User's Guide
You can create a custom part number for your design, which can be used to order factory pre-programmed devices. Or request a phase noise report for this design.	Ask for Help Have a question about your design? Click here to get assistance.
Frequency Plan Valid O Design OK Typical Pd 934 mW, Tj 42 °	C Home Close

Figure 24. Export Register Map File

Si5340-D-EVB

You can now write your device's complete configuration to file formats suitable for in-system programming.

				· · · ·		
About Regi	ster Export	o registers that	t nood to be written to the C	5240 to achie	we vour design	
configuratio	on.	e registers tria	theed to be written to the 5	5540 to acrite	eve your design	
A command command p	l line version c prompt to learn	of this tool is av n more.	ailable. Type CBProProjectR	egistersExpo	rthelp from	a
Options						
Export Type	2					
Comr Each and c	na Separated ' line in the file lata fields.	Values (CSV) Fi is an address,d	le ata pair in hexadecimal forn	at. A comma	separates the	address
C Coo The n used Include	de Header File egister write se directly in firm summary heac ed. an informa	equence is exp ware code. Jer tional header v	ressed in C code via an array	of address,di	ata pairs. This	can be
prefixed	by the # char	acter. The head	der will contain some basic i	formation ab	out the design	n, tool, ar
prefixed a timest Include Certain This ens the dow this pro	by the # char amp. pre- and post- control registe ures the devic rnload is comp cess already.	acter. The head write control r ers must be wri e is stable duri lete. You can t	win be included at the top of der will contain some basic i egister writes tten before and after writing ng configuration download urn inclusion of this sequence	the volatile of the volatile of and resumes i e off if your h	configuration re normal operations is n	egisters. ion after managing
prefixed a timest Include Certain This ens the dow this pro	I by the # char amp. pre- and post- control registe ures the devic rnload is comp cess already. geting pre-pro	acter. The head write control r ers must be wri e is stable duri ilete. You can t oduction samp	will be included at the top of lear will contain some basic i egister writes tten before and after writing ng configuration download urn inclusion of this sequenc les	the volatile c ind resumes i e off if your h	configuration r normal operat	egisters. ion after managin <u>o</u>
prefixed a timest Include Certain This ens the dow this pro	I by the # char amp. pre- and post- control registe ures the device unes the device inload is comp cess already. rgeting pre-pro	acter. The head write control r rs must be wri e is stable duri lete. You can t oduction samp	will be included at the top of ger will contain some basic i egister writes tten before and after writing ng configuration download urn inclusion of this sequenc les	the volatile c ind resumes i e off if your h	configuration r normal operat lost system is r	egisters. ion after managing
prefixed a timest ✓ Include Certain This ens the dow this pro	l by the # char amp. pre- and post- control registe unload is comp cess already. geting pre-pro	acter. The head write control r rs must be wri e is stable duri lete. You can t oduction samp	will be included at the top of egister writes tten before and after writing ng configuration download urn inclusion of this sequenc les	the volatile c ind resumes e off if your h	configuration r normal operat loost system is i	egisters. ion after managing
prefixec a timest Include Certain This ens the dow this pro	I by the # char amp. pre- and post- control registe ures the devic rnload is comp cess already. geting pre-pro	acter. The head write control r rs must be wri e is stable duri ilete. You can t oduction samp	egister writes egister writes tten before and after writing ng configuration download urn inclusion of this sequenc les	formation ab the volatile c and resumes e off if your h	configuration r normal operat	egisters. ion after managing

Figure 25. Export Settings

11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device's non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5340 using ClockBuilder Pro on the Si5340-D-EB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5340 RAM space and can be done virtually unlimited number of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device datasheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of two times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

12. Serial Device Communications (Si5340 <--> MCU)

12.1. On-Board SPI Support

The MCU on-board the Si5340-D-EB communicates with the Si5340 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5340 device is the SPI slave. The Si5340 device can also support a 2-wire I2C serial interface, although the Si5340-D-EB does NOT support the I2C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I2C.

12.2. External I2C Support

I²C can be supported if driven from an external I²C controller. The serial interface signals between the MCU and Si5340 pass through shunts loaded on header J17. These jumper shunts must be installed in J17 for normal EVB operation using SPI with CBPro. If testing of I²C operation via external controller is desired, the shunts in J17 can be removed thereby isolating the on-board MCU from the Si5340 device. The shunt at JP1 (I2C SEL) must also be removed to select I²C as Si5340 interface type. An external I2C controller connected to the Si5340 side of J17 can then communicate to the Si5340 device. (For more information on I²C signal protocol, please refer to the Si5340 data sheet.)

Figure 26 below illustrates the J17 header schematic. J17 even numbered pins (2, 4, 6, etc.) connect to the Si5340 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J17 and JP1, I²C operation should use J17 pin 4 (DUT SDA SDIO) as the I²C SDA and J17 pin 8 (DUT SCLK) as the I²C SCLK. Please note the external I²C controller will need to supply its own I²C signal pull-up resistors.



Figure 26. Serial Communications Header J17

13. Si5340-D-EVB Schematic and Bill of Materials (BOM)

The Si5340-D-EVB Schematic and Bill of Materials (BOM) can be found online at:

www.skyworksinc.com/support-ia

Please be aware the Si5340-D-EB schematic is in OrCad Capture hierarchical format and not in a typical "flat" schematic format.

18 Skyworks Solutions, Inc. • Phone [781] 376-3000 • Fax [781] 376-3100 • sales@skyworksinc.com • www.skyworksinc.com Rev. 1.0 • Skyworks Proprietary Information • Products and Product Information are Subject to Change Without Notice • December 2, 2021