UG362: Si5348-E Evaluation Board User's Guide

The Si5348-E-EVB is used for evaluating the Si5348 Network Synchronizer Clock for SyncE/1588 and Stratum 3/3E applications. The device revision is distinguished by a white 1 inch x 0.187 inch label with the text “SI5348-E-EB” in the lower left-hand corner of the board. (For ordering purposes only, the terms “EB” and “EVB” refer to the board and the kit respectively. In this document, the terms are synonymous in context.) The Si5348 contains three independent DSPLLs in a single IC with programmable jitter attenuation bandwidth on a per DSPLL basis. The Si5348-E-EVB supports three independent differential input clocks, two independent CMOS input clocks, and seven independent output clocks via onboard SMA connectors. The Si5348-E-EVB can be controlled and configured via a USB connection to a host PC running Silicon Labs’ next generation Clock Builder Pro™ (CBPro™) software tool. Test points are provided on-board for external monitoring of supply voltages.

The device revision is distinguished by a white 1 inch x 0.187 inch label with the text “SI5348-E-EB” installed in the lower left hand corner of the board. (For ordering purposes only, the terms “EB” and “EVB” refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.

This kit comes with an OCXO board SiOCXO1-EB as well as a TCXO board SiTCXO1-EB. The OCXO or the TCXO are used on the reference input (REF) of the Si5348 to evaluate the holdover stability of the network synchronizer clock. Both boards are not needed at the same time, but they are both included in the kit to provide a comparison of the resulting performance.

EVB FEATURES

- Powered from USB port or external +5 V power supply via screw terminals
- Included SiOCXO1-EB reference OCXO board allows for evaluation in standalone and holdover mode.
- Included SiTCXO1-EB reference TCXO board allows for evaluation in standalone and holdover mode.
- CBPro™ GUI programmable VDD supply allows device supply voltages from 3.3, 2.5, or 1.8 V
- CBPro™ GUI programmable V_{DDO} supplies allow each of the seven outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro™ GUI allows control and measurement of voltage, current, and power of VDD and all 8 VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5348
- SMA connectors for input clocks, output clocks and optional external timing reference clock

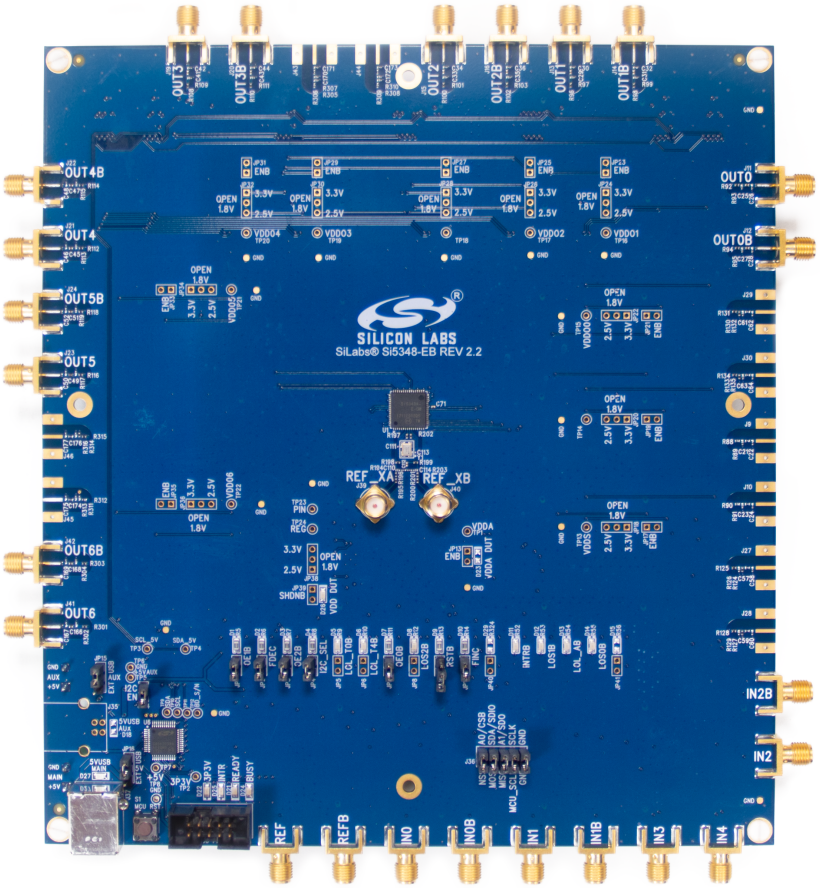

Figure .1. Si5348-E-EVB

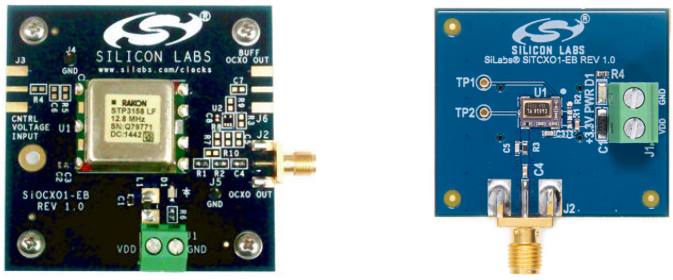

Figure .2. SiOCXO1-EB (left) SiTCXO1-EB (right)

1. Si5348-E-EVB Functional Block Diagram, Support Documentation, and ClockBuilderPro™ Software

Below is a functional block diagram of the Si5348-E-EVB. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See 2. Quick Start and Jumper Defaults for more information.

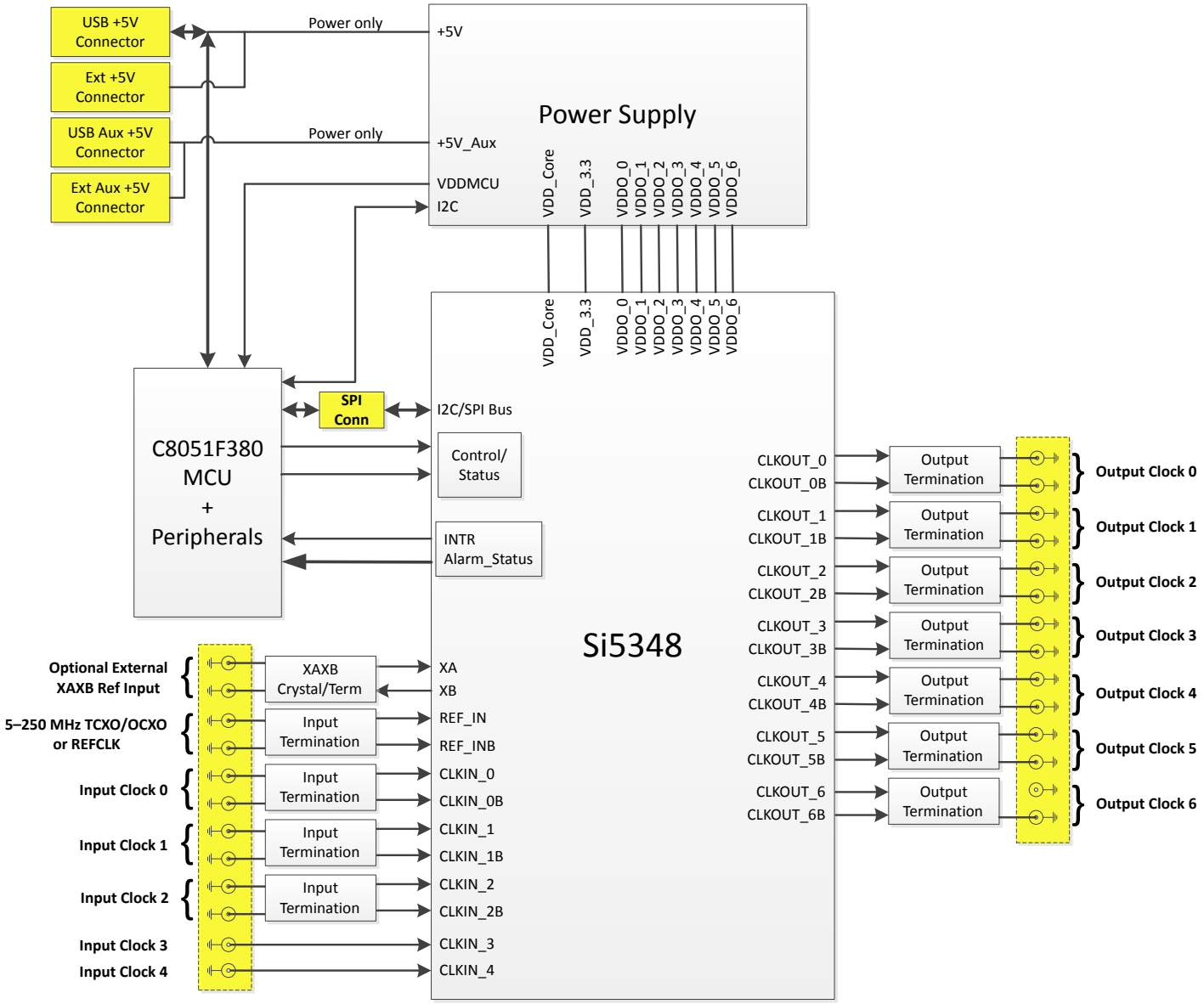

Figure 1.1. Si5348-E-EVB Functional Block Diagram

All Si5348 schematics, BOMs, User's Guides, and software can be found online at the following link: http:www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

The SiOCXO1-EB User's Guide is located at: https://www.silabs.com/documents/public/user-guides/UG123.pdf

The SiTCXO1-EB User's Guide is located at: https://www.silabs.com/documents/public/user-guides/ug364-sitcxo1-evb-ug.pdf

2. Quick Start and Jumper Defaults

1. Install ClockBuilderPro desktop software from EVB support web page given in Section 2.
2. Connect USB cable from Si5348-E-EVB to PC with ClockBuilderPro software installed.
3. Connect the SIOCXO1-EB or SiTCXO1-EB to the reference input (REF) on the Si5348 using the included SMA connector.
4. Leave the jumpers as installed from the factory, and launch the ClockBuilderPro software.
5. You can use ClockBuilderPro to create, download, and run a frequency plan on the Si5348-E-EVB.
6. For the Si5348 data sheet, go to https://www.silabs.com/documents/public/data-sheets/si5348-e-datasheet.pdf.
7. For the Si5348 reference manual, go to http://www.silabs.com/documents/public/reference-manuals/si5348-e-family.pdf.

Table 2.1. Si5348-E EVB Jumper Defaults*

Location	Type	I = Installed O = Open		Location	Type	I = Installed O = Open
JP1	2 pin	I		JP23	2 pin	O
JP2	2 pin	I		JP24	2 pin	O
JP3	2 pin	I		JP25	2 pin	O
JP4	2 pin	I		JP26	2 pin	O
JP5	2 pin	O		JP27	2 pin	O
JP6	2 pin	O		JP28	2 pin	O
JP7	2 pin	I		JP29	2 pin	O
JP8	2 pin	O		JP30	2 pin	O
JP9	2 pin	O		JP31	2 pin	O
JP10	2 pin	I		JP32	2 pin	O
JP13	2 pin	O		JP33	2 pin	O
JP14	2 pin	I		JP34	2 pin	O
JP15	3 pin	1 to 2		JP35	2 pin	O
JP16	3 pin	1 to 2		JP36	2 pin	O
JP17	2 pin	O		JP38	3 pin	All open
JP18	2 pin	O		JP39	2 pin	O
JP19	2 pin	O		JP40	2 pin	O
JP20	2 pin	O		JP41	2 pin	O
JP21	2 pin	O				
JP22	2 pin	O		J36	5x2 Hdr	All 5 installed

Note: Refer to the Si5348-E-EVB schematics for the functionality associated with each jumper.

3. Status LEDs

Table 3.1. Si5348-E EVB Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD Core voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy
D5	LOL_T0B	Blue	Loss of Lock - DSPLL C
D6	LOL_T4B	Blue	Loss of Lock - DSPLL D
D8	LOS2B	Blue	Loss of Signal at IN2
D11	INTRB	Blue	Si5348 Interrupt Active
D12	LOS1B	Blue	Loss of Signal at IN1
D13	LOL_AB	Blue	Loss of Lock DSPLL A
D14	LOS0B	Blue	Loss of Signal at IN0

D27, D22, and D26 are illuminated when USB +5 V, Si5348-E-EVB +3.3 V, and Si5348 VDD or supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity. LEDs D14, D12, and D8 indicate loss of signal at clock inputs IN0, IN1, and IN2, respectively. LEDs D13, D5, and D6 indicate loss of lock for one of three internal DSPLLs (A, C, and D) respectively. D11 indicates Si5348 interrupt output is active (as configured by Si5348 register programming). LED locations are highlighted below with LED function name indicated on board silkscreen.

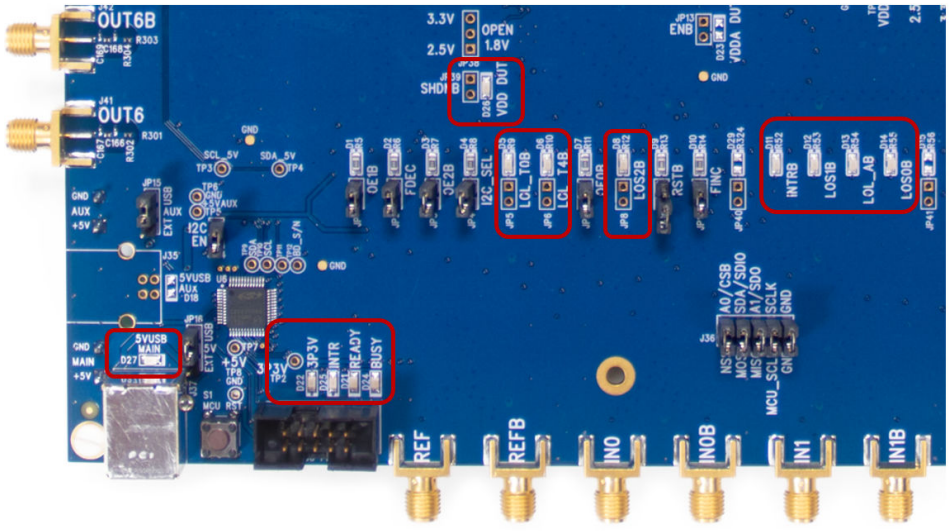

Figure 3.1. Si5348-E-EVB LED Locations

4. External Reference Input (XA/XB)

An external timing reference (48 MHz XTAL) is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. The Si5348-E-EVB can also accommodate an external reference clock instead of a crystal. To evaluate the device with an external REFCLK, C111 and C113 must be populated and XTAL Y1 removed (see figure below). The REFCLK can then be applied to SMA connectors J39 and J40.

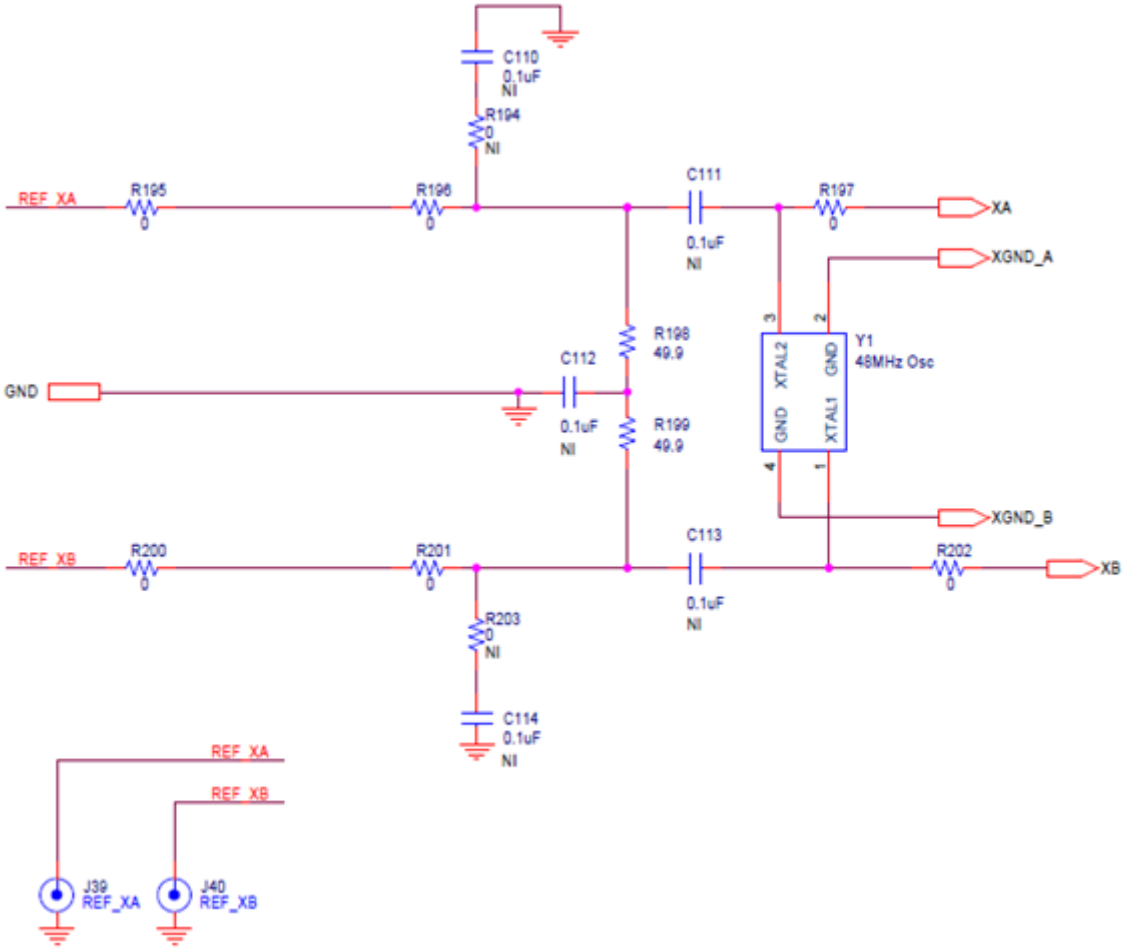

Figure 4.1. External Reference Input Circuit

5. Clock Input and Output Circuits

5.1 Clock Input Circuits (REF/REFB, IN0/IN0B-IN2/IN2B, IN3, IN4)

The Si5348-E-EVB has eight SMA connectors (REF/REFB, IN0/IN0B–IN2/IN2B) for receiving external differential clock signals. The REF/REFB differential input clock is intended to support a TCXO or OCXO, such as the included SiOCXO1-EB or the included SiTCXO1-EB, which determines the Si5348's wander performance. (Please note that this input clock is different from the optional reference clock that may be applied at XA/XB.) All differential input clocks are terminated as shown in the figure below. The only exception is that the terminating 49.9 Ω resistor for REF is not installed. This is R84 corresponding to IN0's R76 in the figure below. The reason for this exception is that single-ended TCXOs and OCXOs typically cannot drive a 50 Ω load. Note that input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5348 data sheet or reference manual.

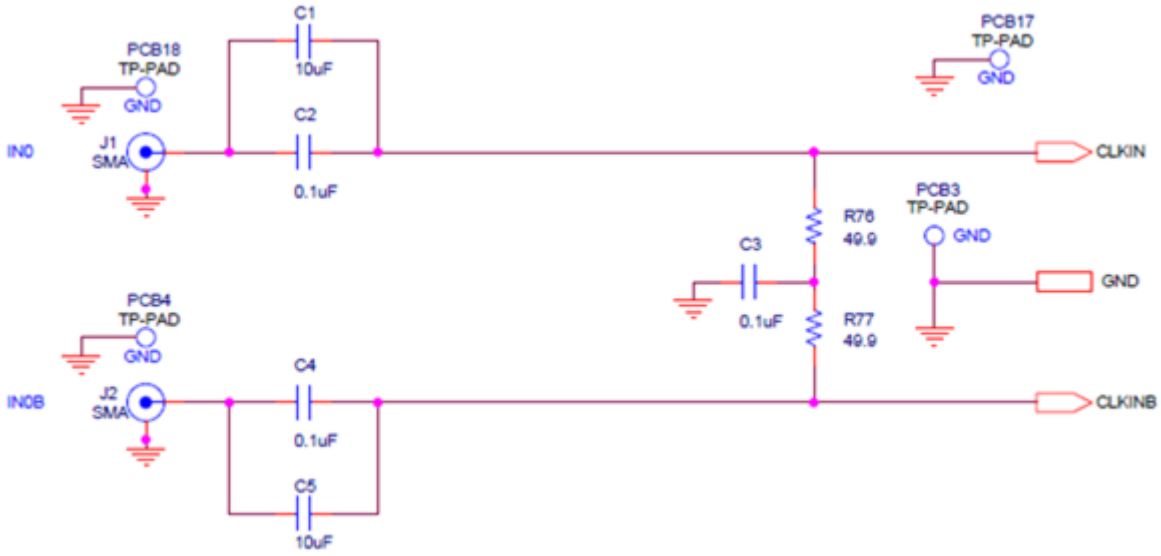

Figure 5.1. Differential Input Clock Termination Circuit

In addition, the Si5348-E-EVB supports two SMA connectors (IN3, IN4) for receiving external single-ended LVCMOS clocks. Each of these clocks connects to its respective Si5348 pins via a single installed 0 Ω resistor. There are no other termination components on the EVB.

5.2 Clock Output Circuits (OUTx/OUTxB)

Each of the 14 output drivers (seven differential pairs, OUT0/OUT0B—OUT6/OUT6B) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in the figure below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. In particular, if differential pair OUT6/OUT6B is configured for 1 Hz output, then the AC coupling output capacitors, C166 and C168, each need to be replaced by a 0 Ω resistor. (These capacitors are the respective counterparts of the OUT0/OUT0B output capacitors, C25 and C27, in the figure below.) The Si5348-E-EVB provides pads for optional output termination resistors and/or low-frequency capacitors. Note that components with schematic “NI” designation are not normally populated on the Si5348-E-EVB and provide locations on the PCB for optional dc/ac terminations by the end user.

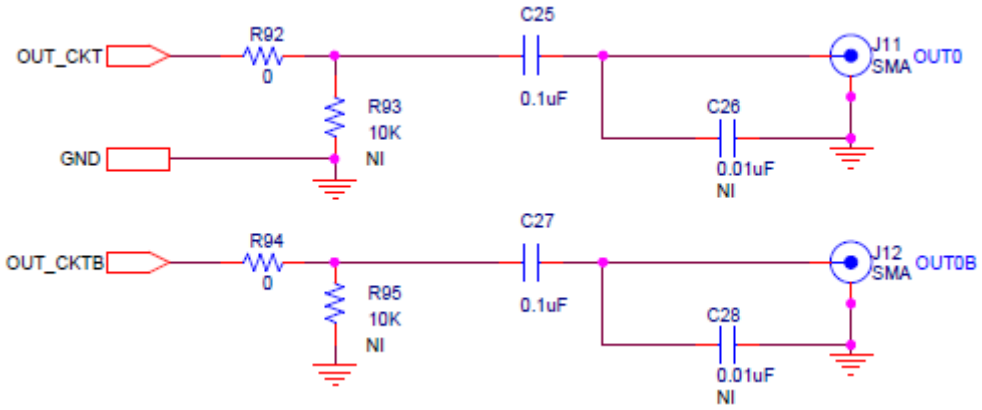

Figure 5.2. Output Clock Termination Circuit

6. Using the Si5348-E-EVB and Installing ClockBuilderPro (CBPro) Desktop Software

6.1 Installing ClockBuilderPro (CBPro) Desktop Software

To install the CBPro software on any Windows 7 (or above) PC:

Go to http://www.silabs.com/CBPro and download ClockBuilderPro software.

Installation instructions and User's Guide for ClockBuilder can be found at the download link shown above. Please follow the instructions as indicated.

6.2 Connecting the EVB to Your Host PC

Once ClockBuilderPro software is installed, connect to the EVB with a USB cable as shown below.

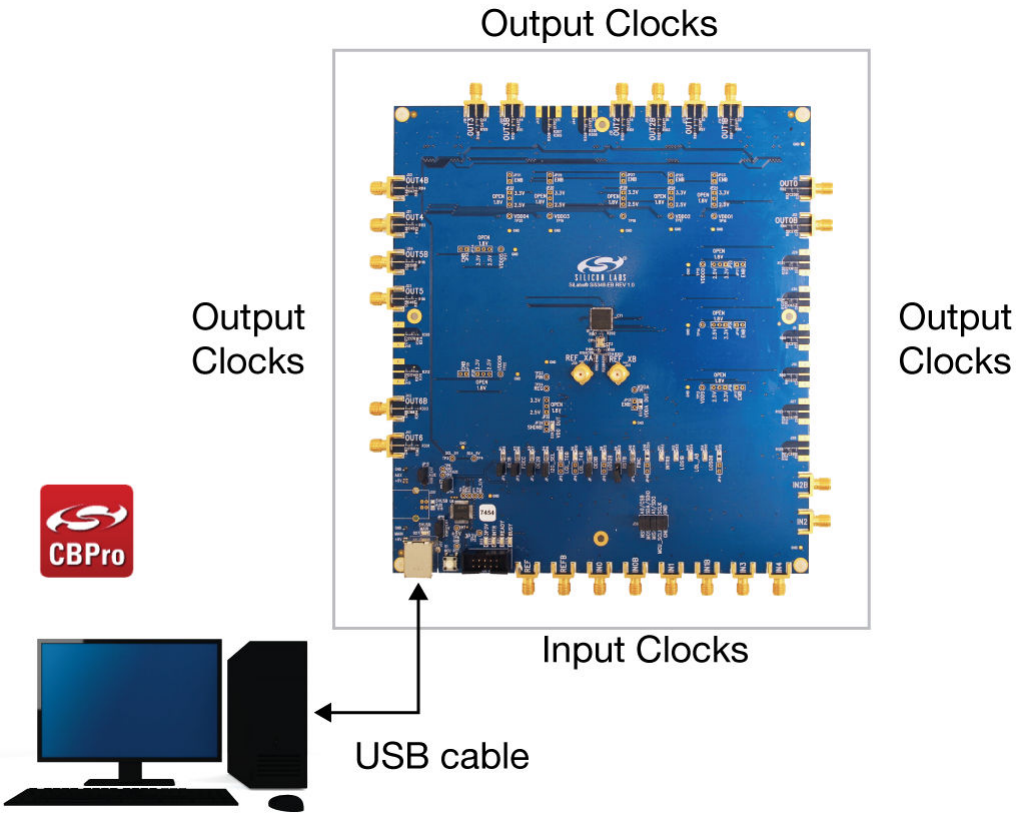

Figure 6.1. EVB Connection Diagram

6.3 Additional Power Supplies

The Si5348-EB comes pre-configured with jumpers installed at JP15 and JP16 (pins 1–2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

The general guidelines for single USB power supply operation are listed below:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA respectively at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤ 470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current limited and need all output clock drivers enabled, re-configure the EVB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
  - Connect external +5 V power supply to terminal block J33 on the back side of the PCB.
  - Move the jumper at JP15 from pins 1–2 USB to pins 2–3 EXT.

6.4 Overview of ClockBuilderPro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro.

The ClockBuilderPro installer will install two main applications:

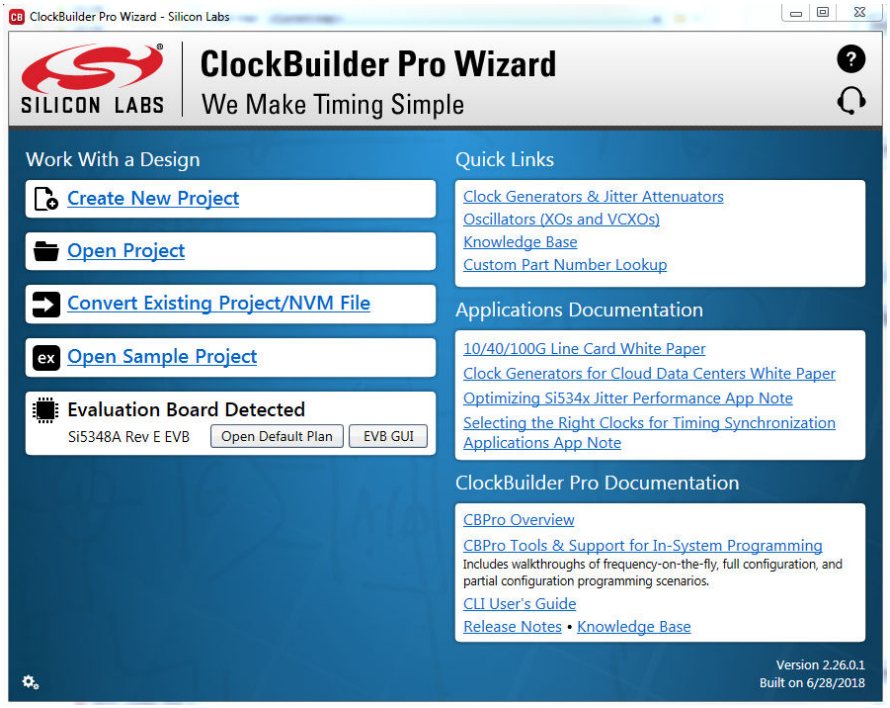

Figure 6.2. Application #1: ClockbuilderPro Wizard

Use the CBPro Wizard to:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming files

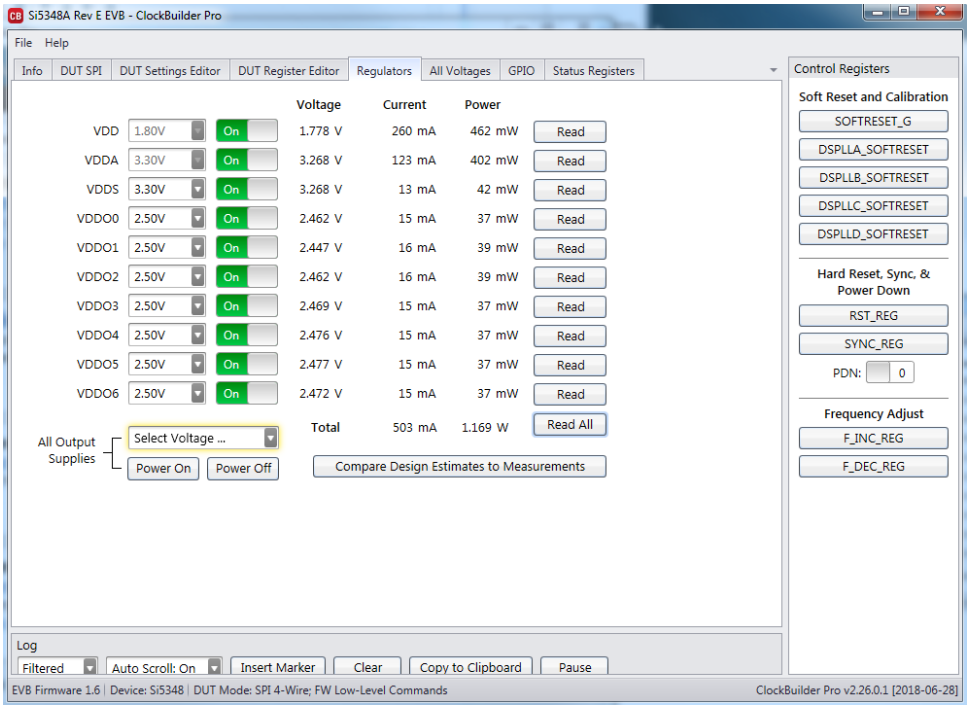

Figure 6.3. Application #2: EVB GUI

Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5348)
- Control the EVB's regulators
- Monitor voltage, current, and power on the EVB

6.5 Common ClockBuilderProWork Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5348-E EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration
- Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration

Each is described in more detail in the following sections.

6.6 Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch ClockBuilder Pro by clicking on this icon on your PC's desktop.

Figure 6.4. ClockBuilderPro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

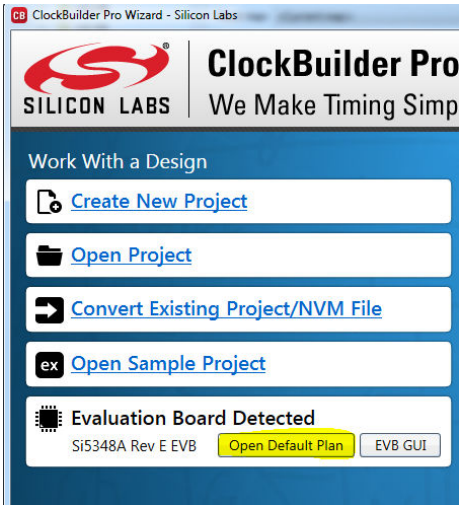

Figure 6.5. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.

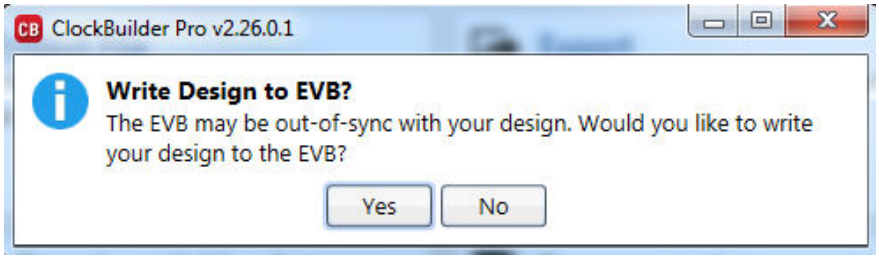

Figure 6.6. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5348 device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

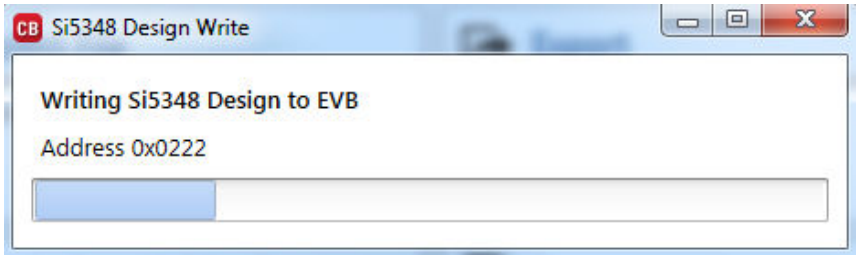

Figure 6.7. Writing Design Status

After CBPro writes the default plan to the EVB, click on “Open EVB GUI” as shown below.

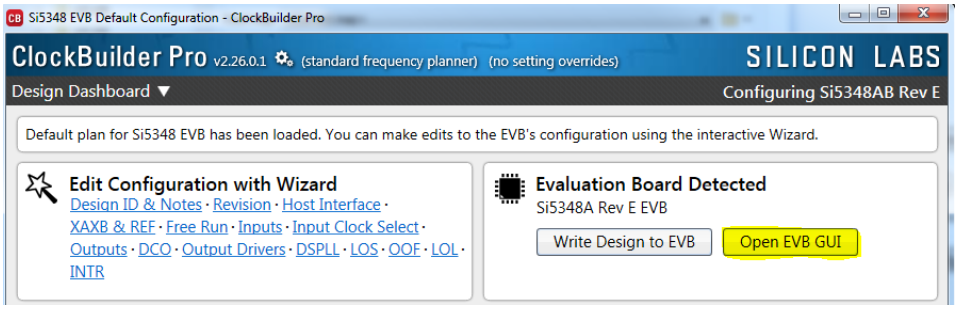

Figure 6.8. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the nominal values defined in the device’s default CBPro project file created by Silicon Labs, as shown in the example session window below.

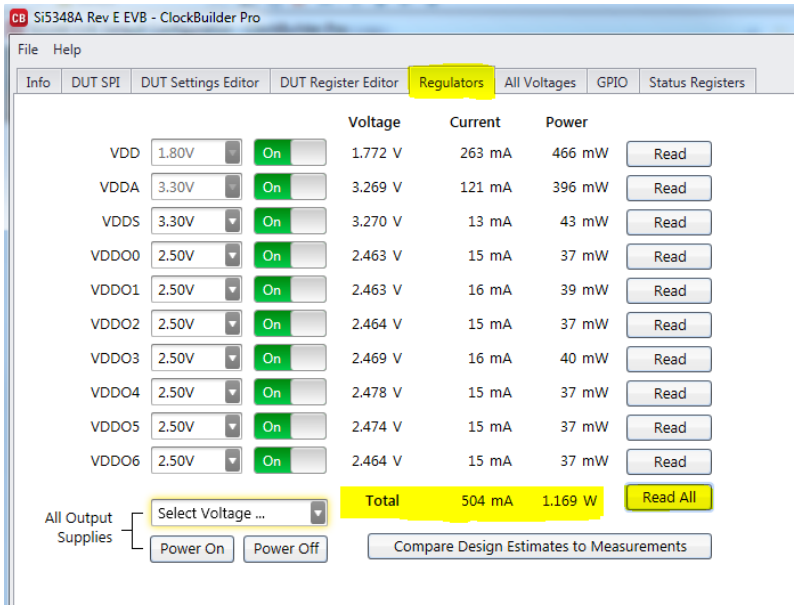

Figure 6.9. EVB GUI Window

6.6.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled “INx/INxB”) located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting “Off” then “On” of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT’s register space, you must go back to the Wizard’s main menu and select “Write Design to EVB”:

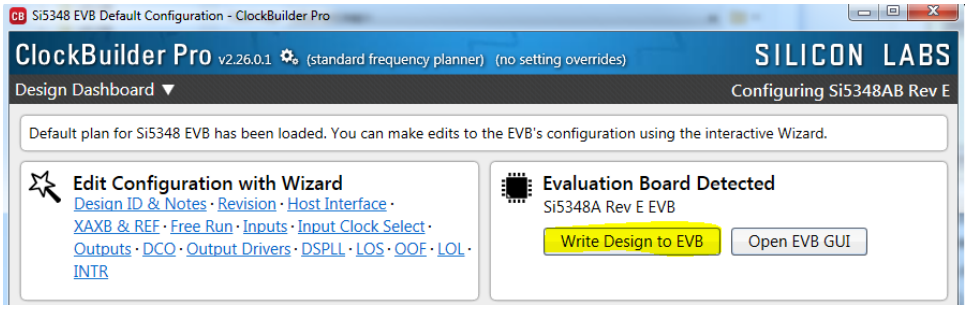

Figure 6.10. Write Design to EVB

Failure to do the step above will cause the device to read in a preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

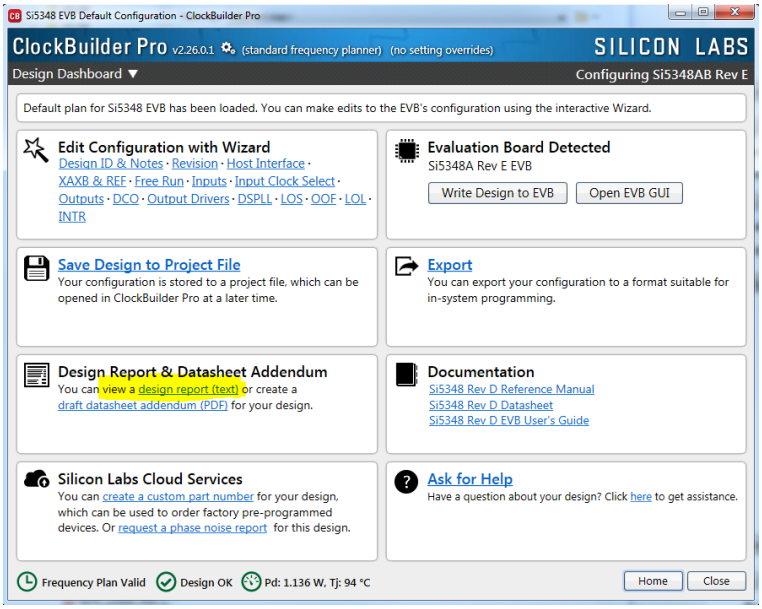

Figure 6.11. View Design Report

Your configuration’s design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project’s Design Report.

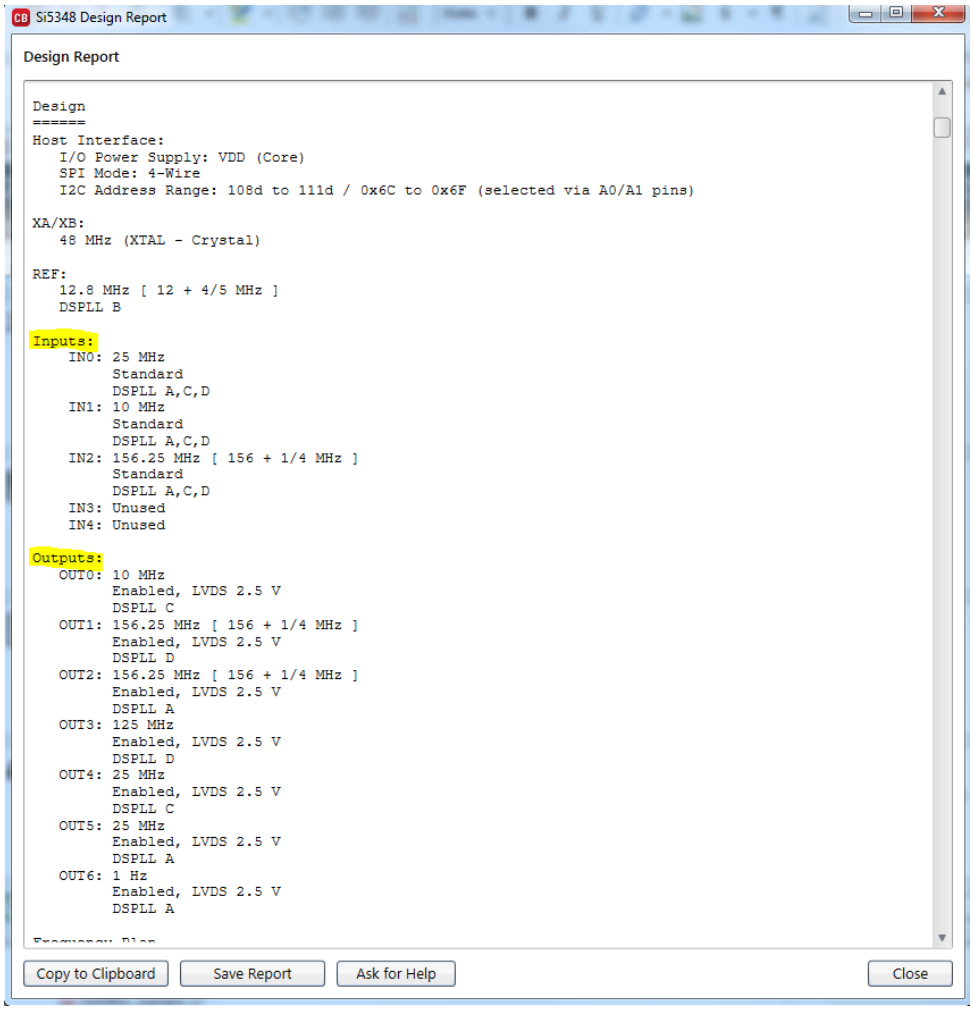

Figure 6.12. Design Report Window

6.6.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in “locked” mode.

6.7 Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the “default” configuration using the CBPro Wizard, click on any of the underlined fields below the header "Edit Configuration with Wizard". You can also pull down on the "Design Dashboard" menu and select a design step.

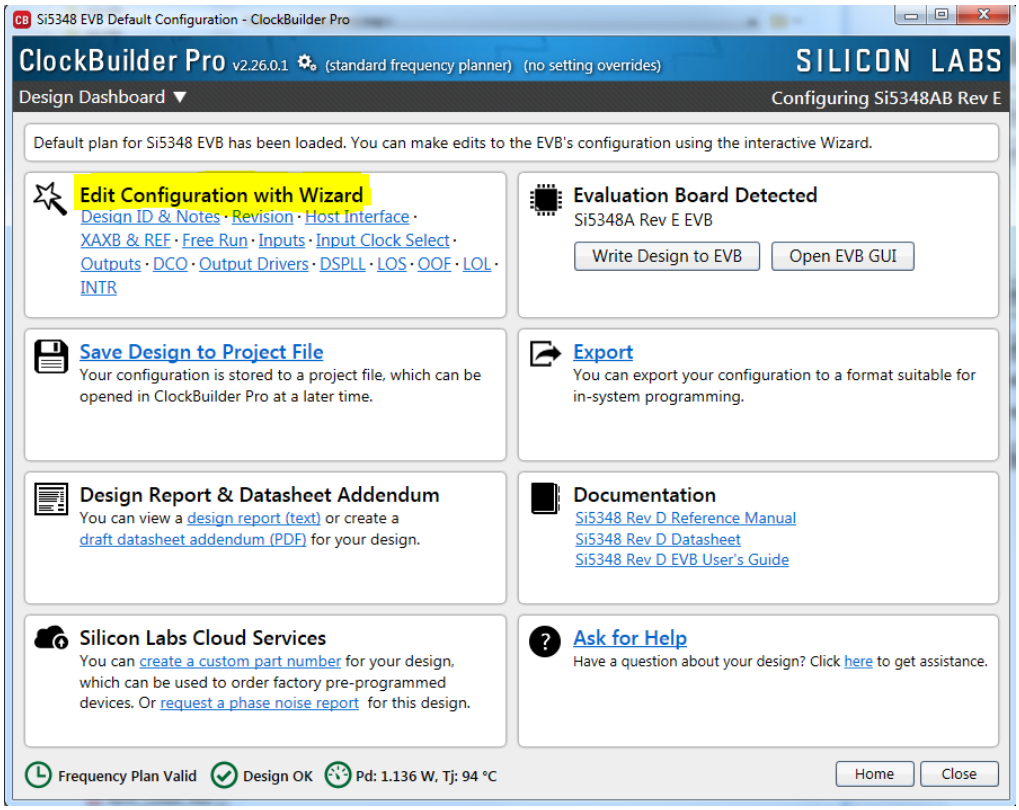

Figure 6.13. Edit Configuration with Wizard

You will now be taken to the Wizard’s step-by-step menus to allow you to change any of the default plan’s operating configurations.

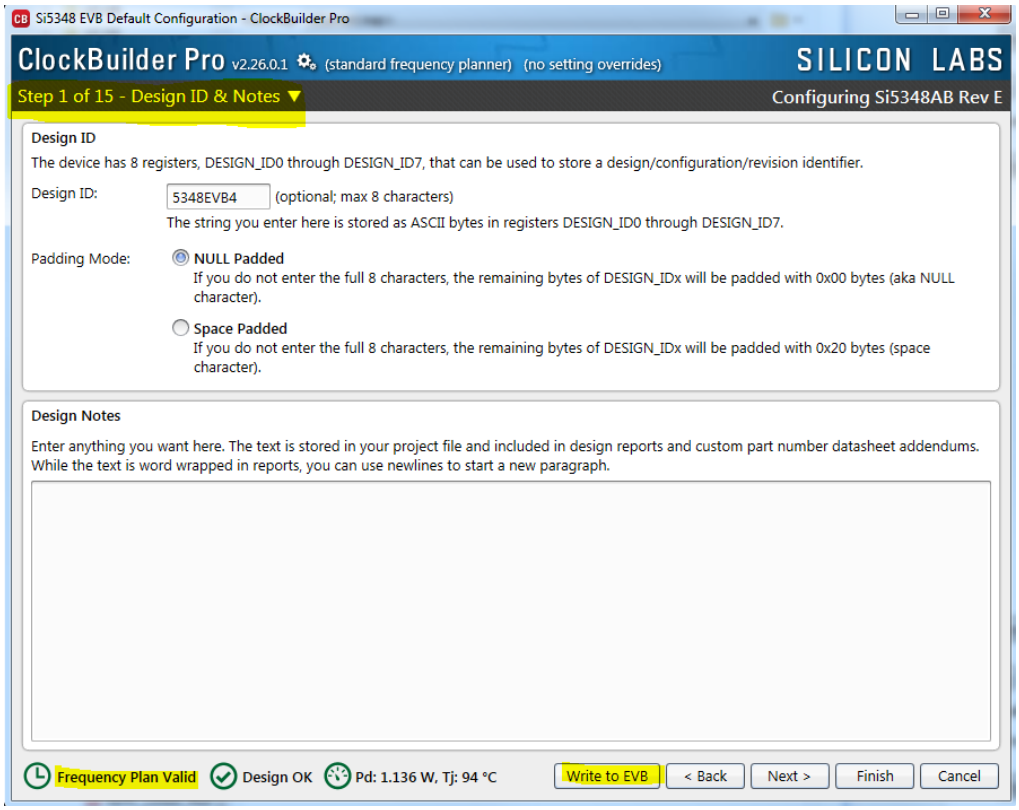

Figure 6.14. Design ID and Notes

Note you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on "Write to EVB" to update the DUT to reconfigure your device in real time. The Design Write status window will appear each time you make a change.

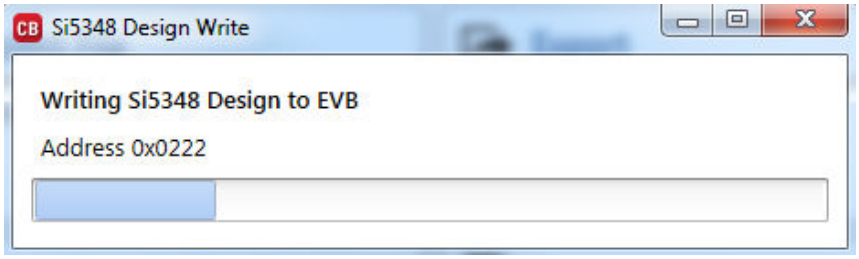

Figure 6.15. Writing Design Status

6.8 Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting "Open Design Project File".

Figure 6.16. Open Design Project File

Locate your CBPro design file (*.slabtimeproj or *.sitproj file) in the Windows file browser.

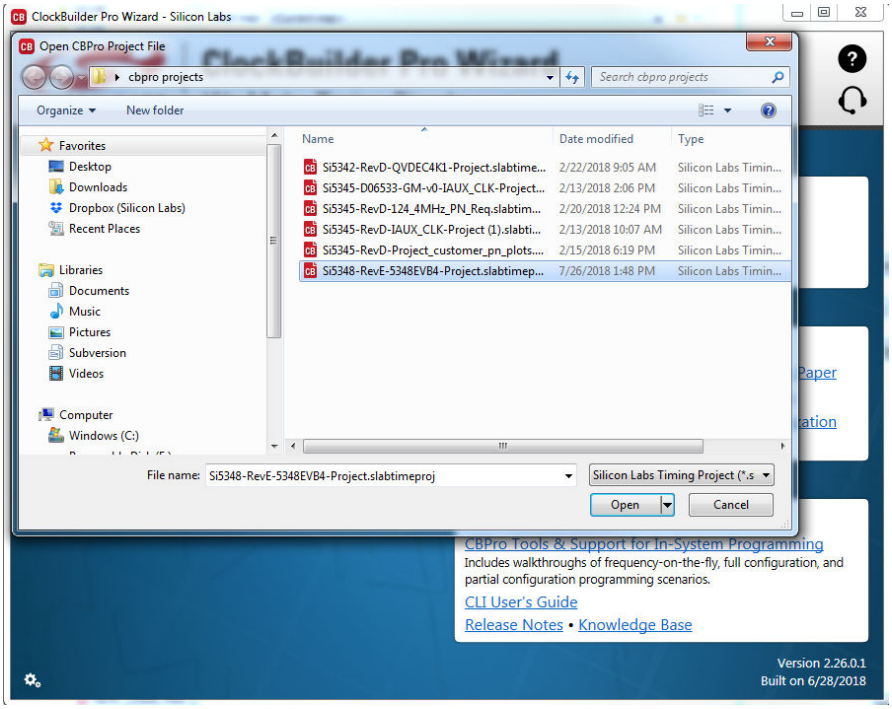

Figure 6.17. Browse to Project File

Select "Yes" when the WRITE DESIGN to EVB popup appears:

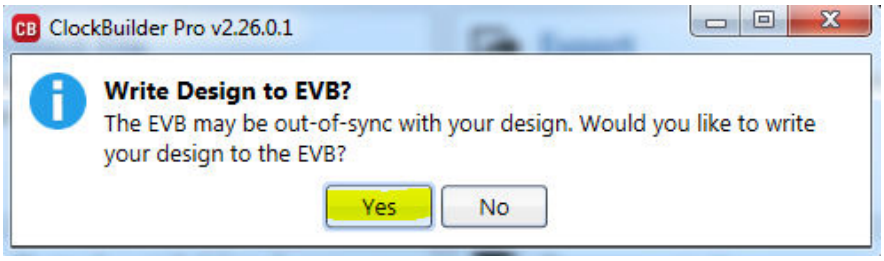

Figure 6.18. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

6.9 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:

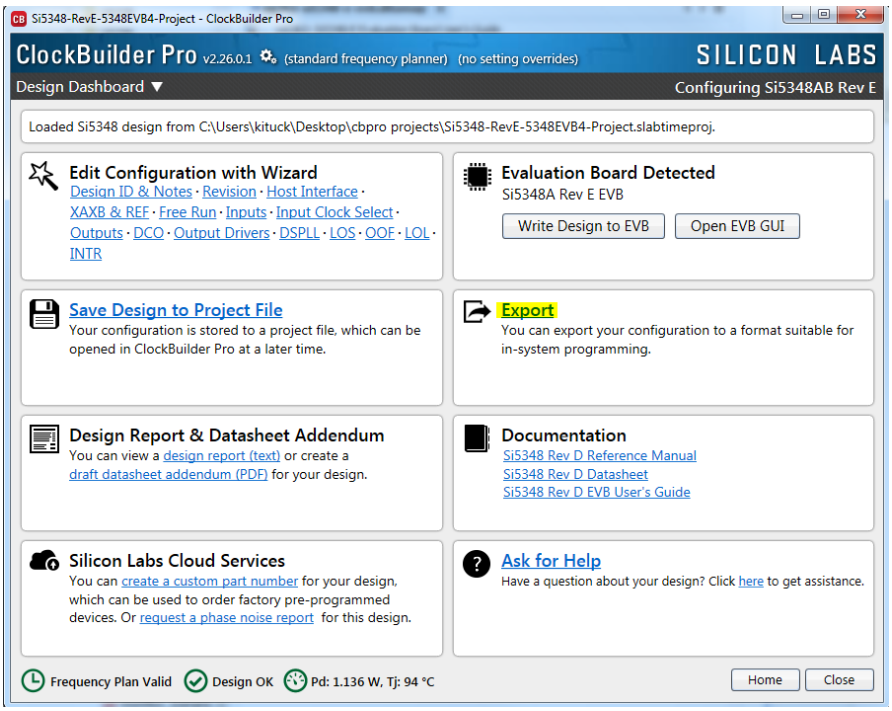

Figure 6.19. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

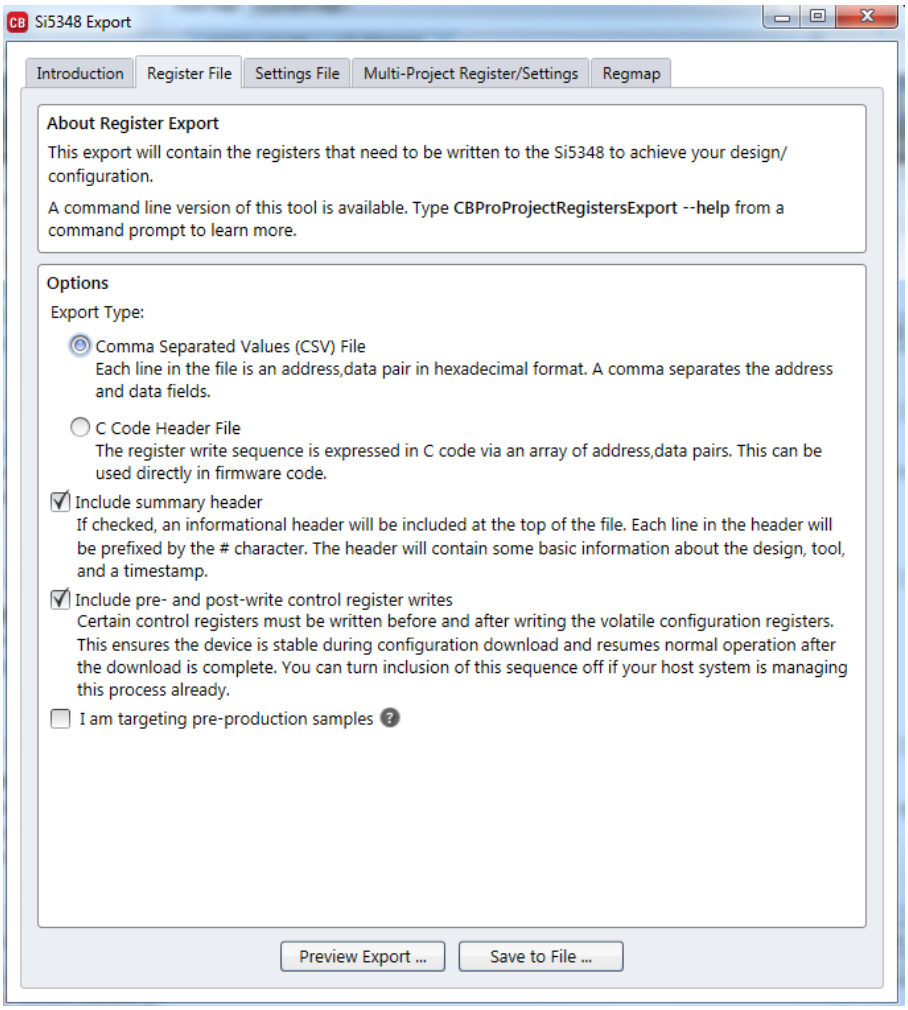

Figure 6.20. Export Settings

7. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP is **NOT** the same as writing a configuration into the Si5348 using ClockBuilder-PRo on the Si5348-E EVB). Writing a configuration into the EVB from ClockBuilderPro is done using Si5348 RAM space and can be done a virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of two times only. Care must be taken to ensure the desired configuration is valid when choosing to write to OTP

8. Serial Device Communications (Si53848 <-> MCU)

8.1 Onboard SPI Support

The MCU onboard the Si5348-E-EVB communicates with the Si5348 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5348 device is the SPI slave. The Si5348 device can also support a 2-wire I^2C serial interface, although the Si5348-E-EVB does NOT support the I^2C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I^2C.

8.2 External I^2C Support

I^2C can be supported if driven from an external I^2C controller. The serial interface signals between the MCU and Si5348 pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I^2C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the on-board MCU from the Si5348 device. The shunt at J4 (I2C_SEL) must also be removed to select I^2C as Si5348 interface type. An external I^2C controller connected to the Si5348 side of J36 can then communicate to the Si5348 device. *(For more information on I^2C signal protocol, please refer to the Si5348 data sheet.)*

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5348 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J36 and J4, I^2C operation should use J36 pin 4 (DUT_SDA_SDIO) as the I^2C SDA and J36 pin 8 (DUT_SCLK) as the I^2C SCLK. Please note the external I^2C controller will need to supply its own I^2C signal pull-up resistors.

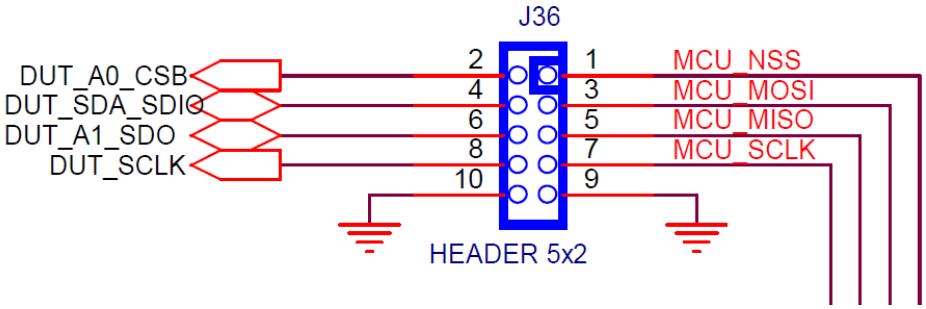

Figure 8.1. Serial Communications Header J36

9. Si5348-E-EVB Schematic and Bill of Materials (BOM)

The Si5348-E-EVB Schematic and Bill of Materials (BOM) can be found online at:

http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

Note: Please be aware that the Si5348-E-EVB schematic is in **OrCad Capture** *hierarchical format* and not in a typical “flat” schematic format.