UG334: Si5394 Evaluation Board User's Guide

The Si5394 EVB is used for evaluating the Si5394 Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier. There are four different EVBs for the Si5394. There is a Grade A and Grade P board which both require an external reference. There is also a Grade J and Grade E board which have a reference internal to the chip. This user guide is intended for all versions of the Si5394 EVBs. The term Si5394 EVB is inclusive of all four different evaluation boards. The device grade and revision is distinguished by a white 1 inch x 0.187 inch label installed in the lower left hand corner of the board. In the example below, the label "SI5394A-A-EB" indicates the evaluation board has been assembled with an Si5394 device, Grade A, Revision A, installed. (For ordering purposes only, the terms “EB” and “EVB” refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

KEY FEATURES

- Si5394A-A-EVB for evaluating external reference versions Si5394A/B/C/D
- Si5394J-A-EVB for evaluating internal reference versions Si5394J/K/L/M
- Si5394P-A-EVB for evaluating external reference (precision grade)
- Si5394E-A-EVB for evaluating internal reference (precision grade)
- Powered from USB port or external power supply
- Onboard 48 MHz XTAL or Reference SMA Inputs allow holdover mode of operation on the Si5394 Grade A and P
- ClockBuilder Pro® (CBPro) GUI programmable VDD supply allows device to operate from 3.3 V, 2.5 V, or 1.8 V
- CBPro GUI programmable VDDO supplies allow each of the 4 outputs to have its own power supply voltage selectable from 3.3V, 2.5V, or 1.8 V
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5394
- SMA connectors for input clocks, output clocks, and optional external timing reference clock to be used on external reference grades only

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1. Functional Block Diagram

Below is a functional block diagram of the Si5394 EVB. Keep in mind that the Grade J and Grade E do not use an external XTAL or reference and do not use the XA/XB pins. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See 3. Quick Start or 10.2 Overview of ClockBuilder Pro Applications for more information.

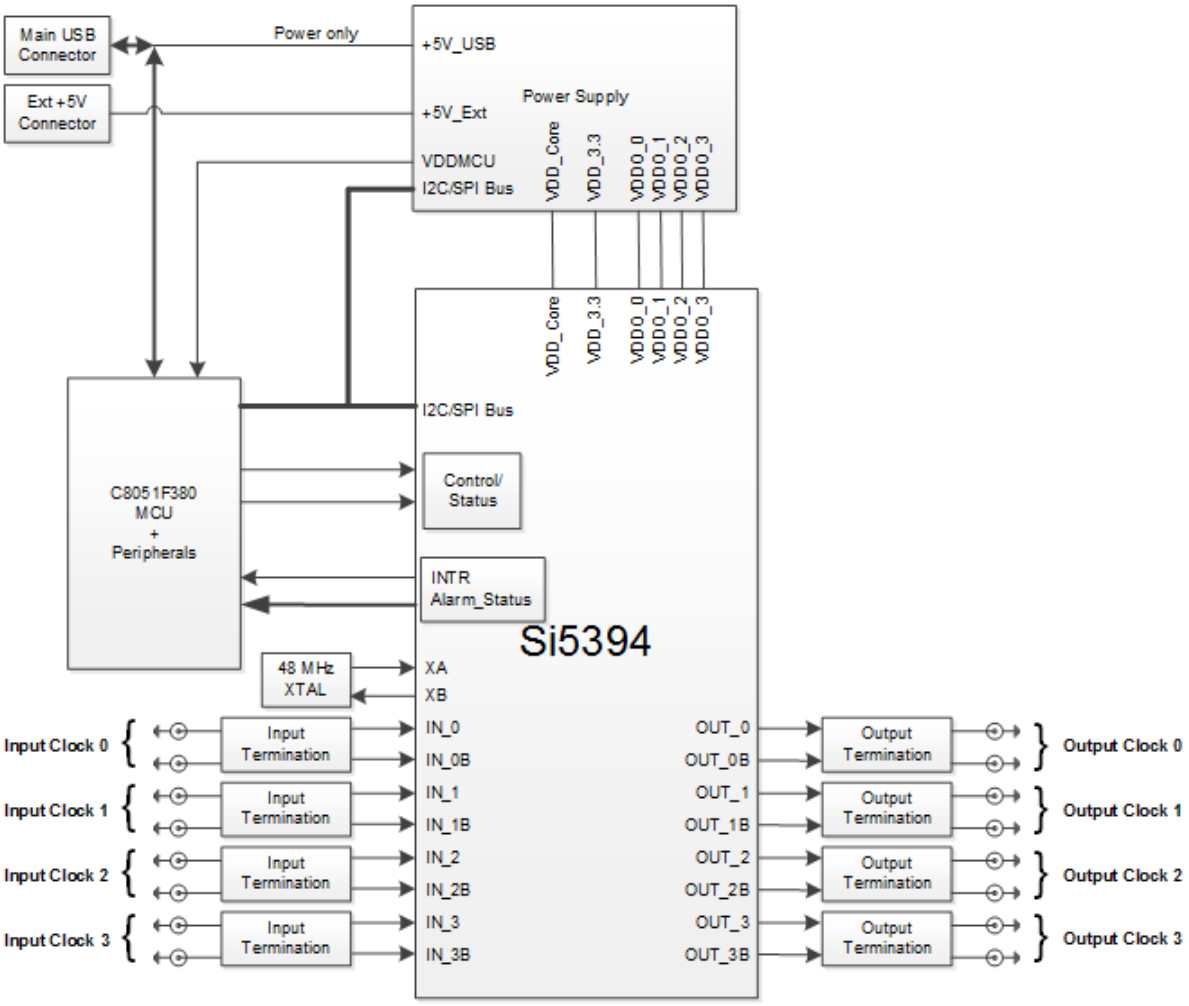

Figure 1.1. Si5394 EVB Functional Block Diagram

2. Si5394 EVB Support Documentation and ClockBuilder Pro Software

All Si5394 EVB schematics, BOMs, User's Guides, and software can be found online at: www.silabs.com/documents/public/schematic-files/si539x-design-files.zip

3. Quick Start

1. Install the ClockBuilder Pro desktop software from http://www.silabs.com/CBPro.
2. Connect a USB cable from Si5394 EVB to the PC where the software was installed.
3. Confirm jumpers are installed as shown in Table 4.1 Si5394 EVB Jumper Defaults[1] on page 6.
4. Launch the ClockBuilder Pro Software.
5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5394 EVB.
6. Find the datasheet: https://www.silabs.com/documents/public/data-sheets/si5395-94-92-a-datasheet.pdf

4. Jumper Defaults

Table 4.1. Si5394 EVB Jumper Defaults[1]

Location	Type	I= Installed 0 = Open	Location	Type	I = Installed 0 = Open
JP1	2-pin	I	JP23	2-pin	O
JP2	2-pin	I	JP24	2-pin	O
JP3	2-pin	I	JP25	2-pin	all open
JP4	2-pin	I	JP26	2-pin	all open
JP5	2-pin	1 to 2	JP27	2-pin	O
JP6	2-pin	O	JP28	2-pin	O
JP7	2-pin	O	JP29	2-pin	all open
JP8	2-pin	O	JP30	2-pin	all open
JP9	2-pin	O	JP31	2-pin	O
JP10	2-pin	O	JP32	2-pin	O
JP11	2-pin	O	JP33	2-pin	all open
JP12	2-pin	O	JP17	5x2 Hdr	All 5 installed
JP13	2-pin	O			

Note:

1. Refer to the Si5394 EVB schematics for the functionality associated with each jumper.

5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D5	INTRB	Blue	Dut Interrupt
D7	LOLB	Blue	DUT Loss of Lock
D8	LOSXAXBB	Blue	DUT Loss of Reference
D11	+5V MAIN	Green	Main USB +5V present
D12	READY	Green	MCU Ready
D13	BUSY	Green	MCU Busy

D11 is illuminated when USB +5V supply voltage is present. D12 and D13 are status LEDs showing onboard MCU activity.

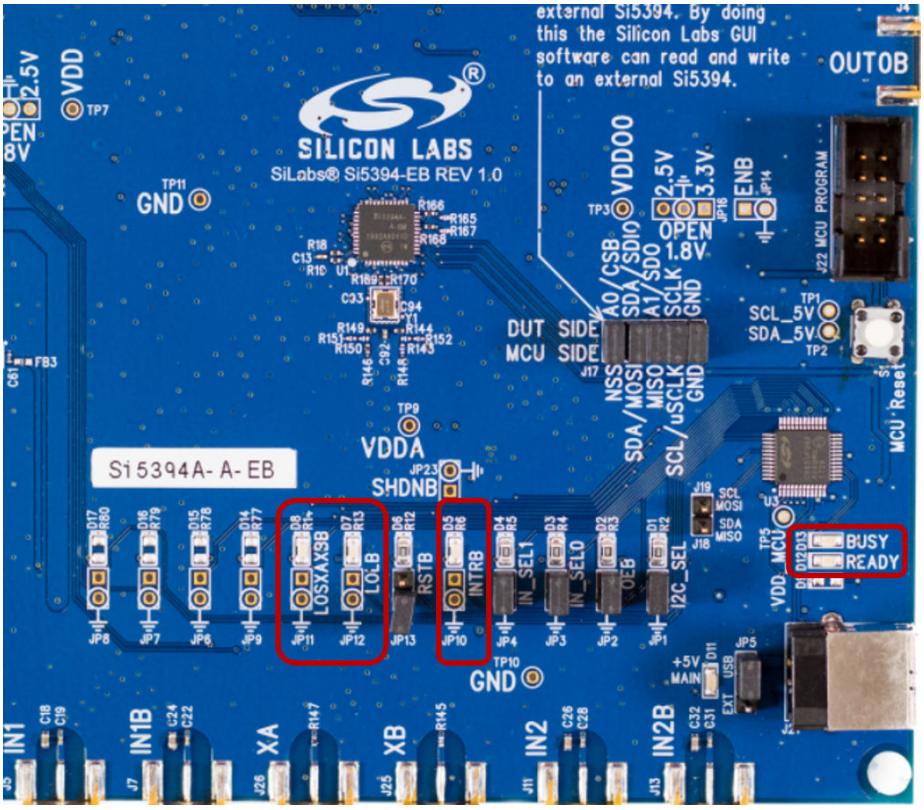

Figure 5.1. Status LEDs

6. External Reference Input (XA/XB)

An external reference (XTAL) is required for Grades A and P and is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL and for providing a stable reference for the free-run and holdover modes. The Si5394P EVB must use a XTAL. See datasheet for specifications to meet performance.To evaluate the device with a REFCLK, C93 and C94 must be populated and the XTAL removed (see Figure 3). The REFCLK can then be applied to J25 and J26. **In the case of the Si5394J-A or Si5394E-A, which are the grades with the XTAL internal to the device, there will be no external XTAL supplied on the board and no input from Ref_XA and Ref_XB. In this case, it is advised that R169 and R170 be removed.**

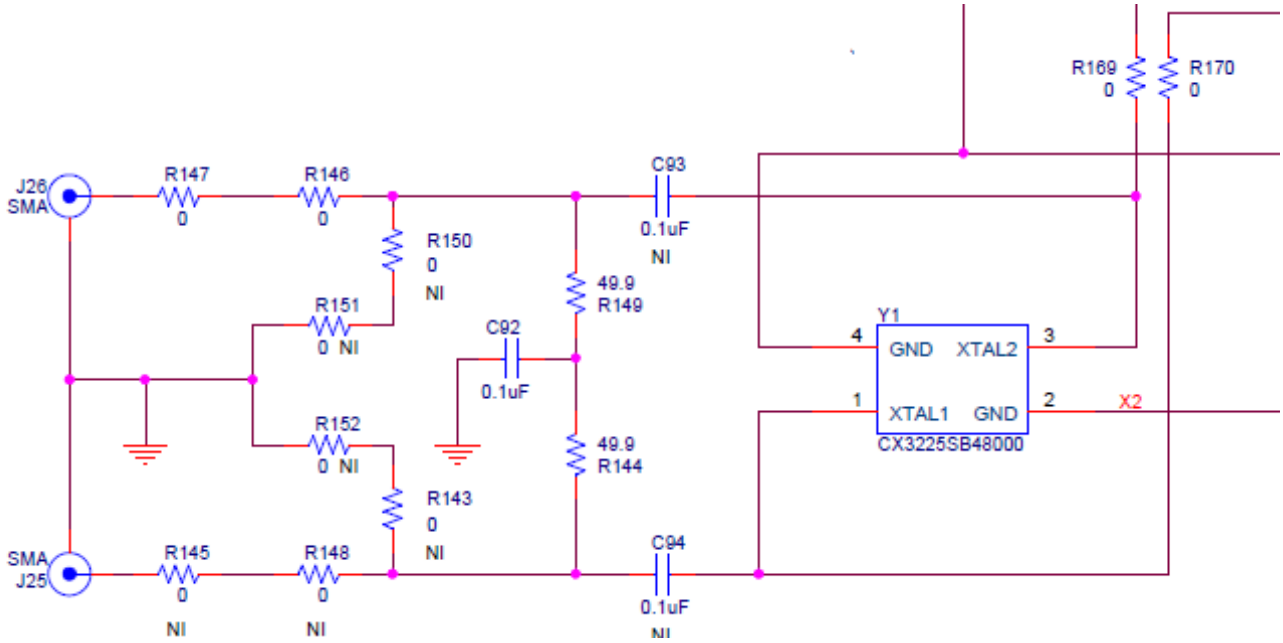

Figure 6.1. External Reference Input Circuit

7. Clock Input Circuits (INx/INxB)

The Si5394 EVB has eight SMA connectors (IN0, IN0B – IN3, IN3B) for receiving external clock signals. All input clocks are terminated as shown below. Note input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, refer to the Si5394 data sheet.

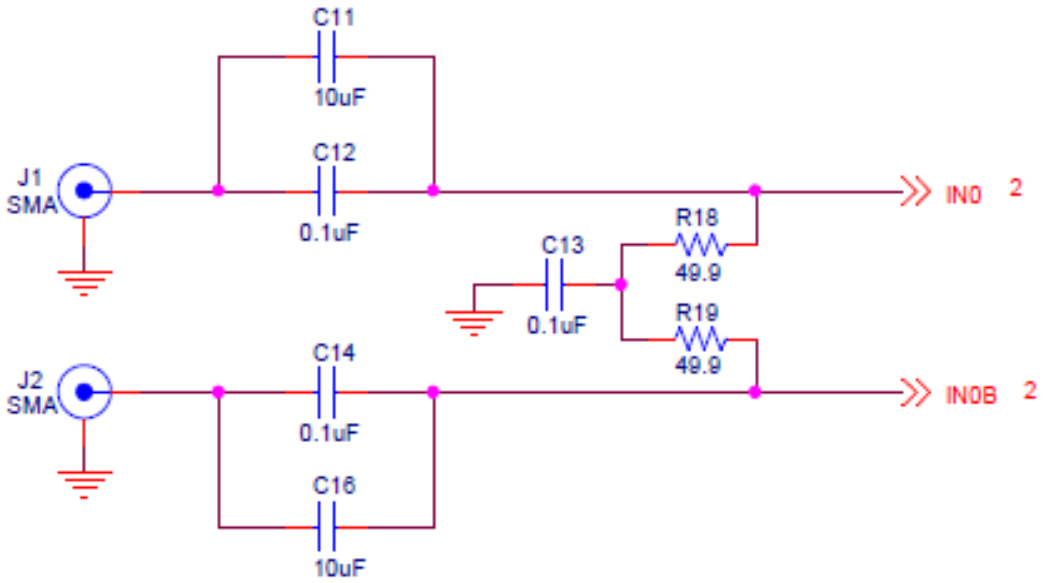

Figure 7.1. Input Clock Termination Circuit

8. Clock Output Circuits (OUTx/OUTxB)

Each of the eight output drivers (4 differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5394 EVB provides pads for optional output termination resistors and/or low-frequency capacitors. Note that components with schematic “NI” designation are not normally populated on the Si5394 EVB and provide locations on the PCB for optional dc/ac terminations by the end user.

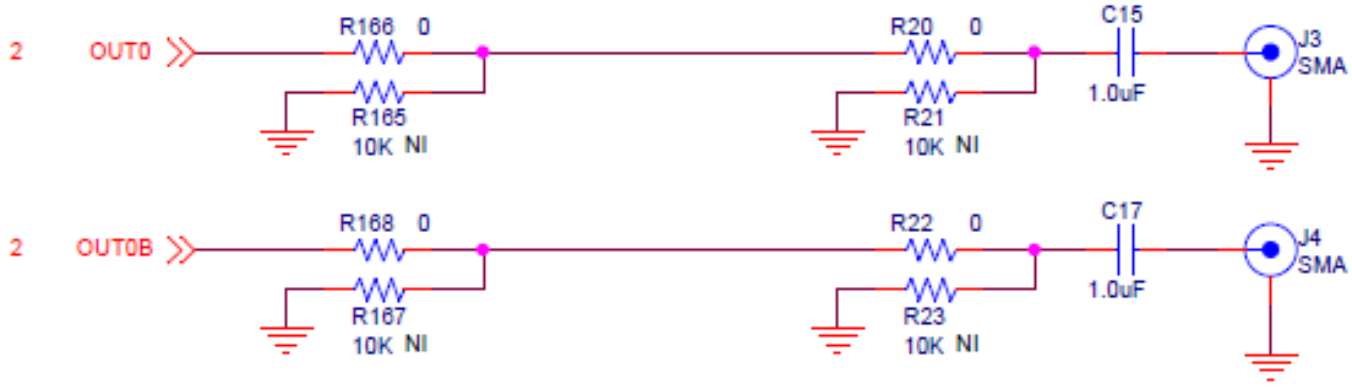

Figure 8.1. Output Clock Termination Circuit

9. Installing ClockBuilder Pro Desktop Software

To install the CBOPro software on any **Windows 7** (or above) PC, go to http://www.silabs.com/CBPro and download the ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above.

10. Using the Si5394 EVB

10.1 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the EVB with a USB cable as shown in the figure below:

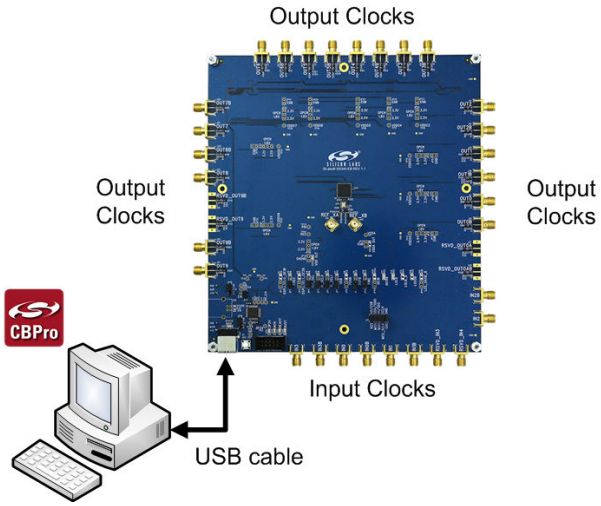

Figure 10.1. EVB Connection Diagram

10.2 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on the grade of your device and your version of ClockBuilder Pro. (The screen captures below were taken for a board labeled "SI5394A-A-EB".) The ClockBuilder Pro installer will install **two** main applications:

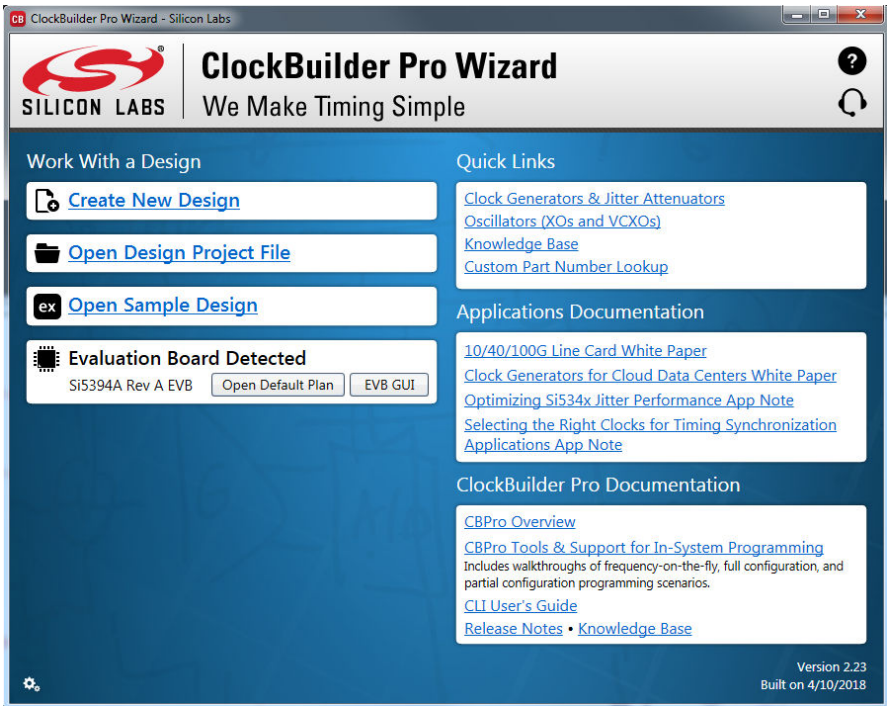

Figure 10.2. Application #1: ClockBuilder Pro Wizard

Use the CBPro wizard to:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming

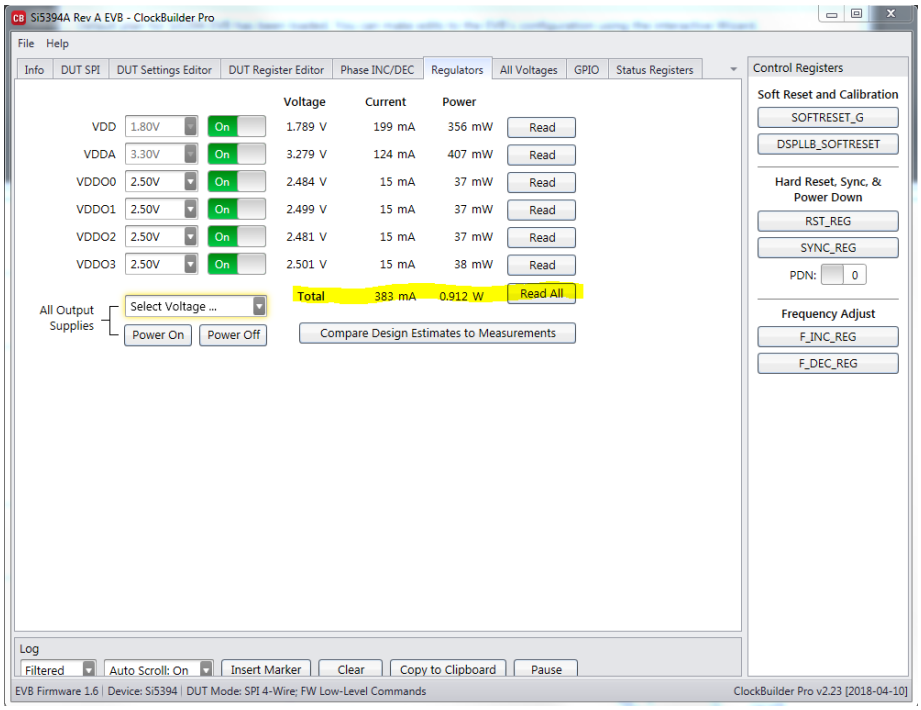

Figure 10.3. Application #2: EVBGUI

Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5394)
- Control the EVB's regulators
- Monitor voltage, current, power on theEVB

10.3 Common ClockBuilder Pro Workflow Scenarios

There are three common workflow scenarios when using CBPro and the Si5394 EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration
- Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration

Each is described in more detail in the following sections.

10.4 Workflow Scenario 1: Testing a Silicon Labs Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch **ClockBuilder Pro** by clicking on this icon on your PC's desktop:

Figure 10.4. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

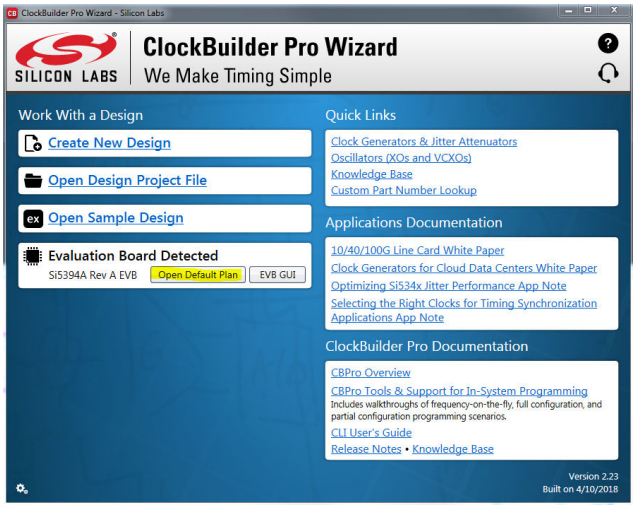

Figure 10.5. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear

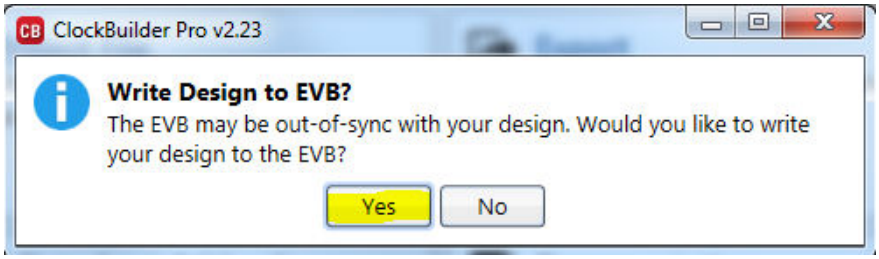

Figure 10.6. Write Design to EVB Dialog

Select “Yes” to write the default plan to the Si5394 device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

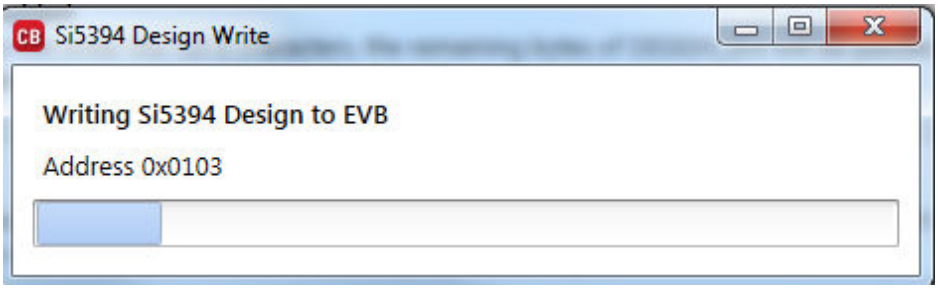

Figure 10.7. Writing Design Status

After CBPro writes the default plan to the EVB, click on “Open EVB GUI” as shown below:

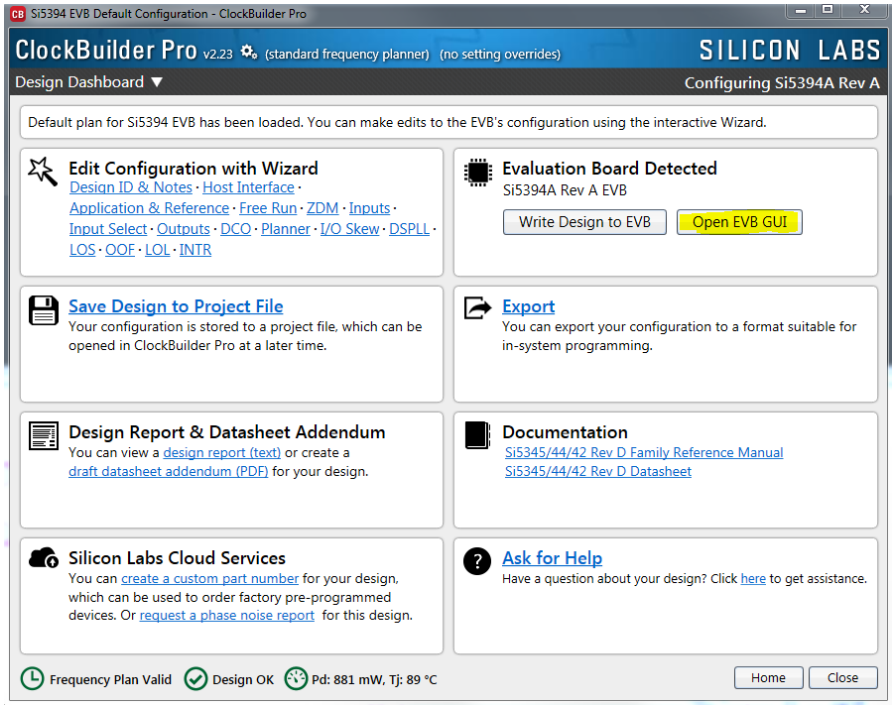

Figure 10.8. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the values defined in the device’s default CBPro project file created by Silicon Labs, as shown below:

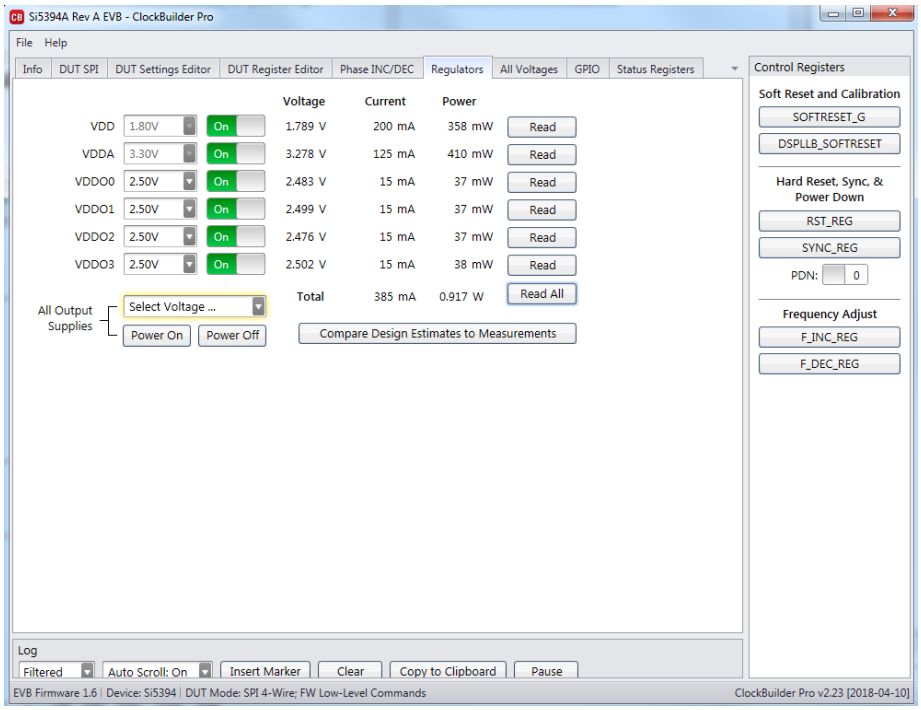

Figure 10.9. EVB GUI Window

10.4.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled “INx/INxB”) located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run aquick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting the VDD and VDDA supplies “Off” then “On” will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT’s register space, you must go back to the Wizard’s main menu and select “Write Design to EVB” as shown below.

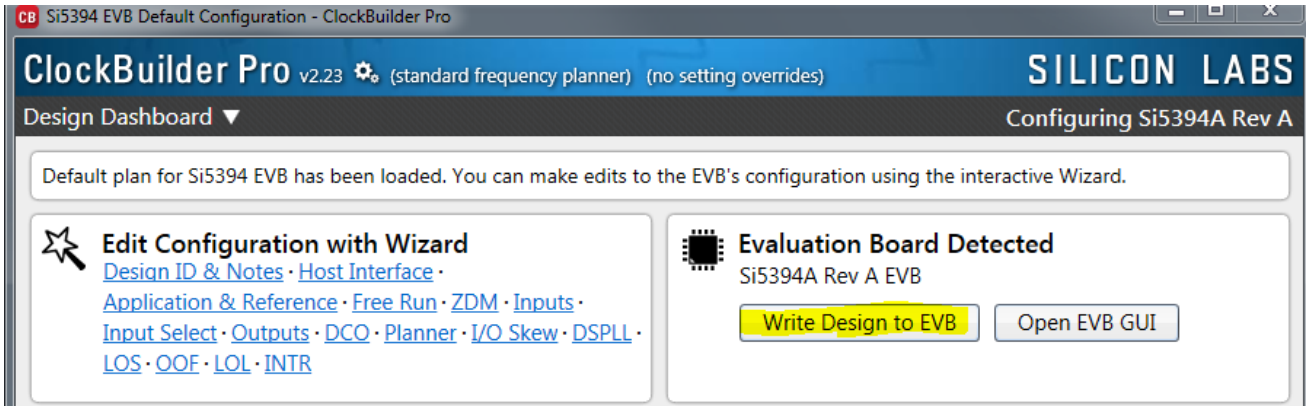

Figure 10.10. Write Design to EVB

Failure to perform the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

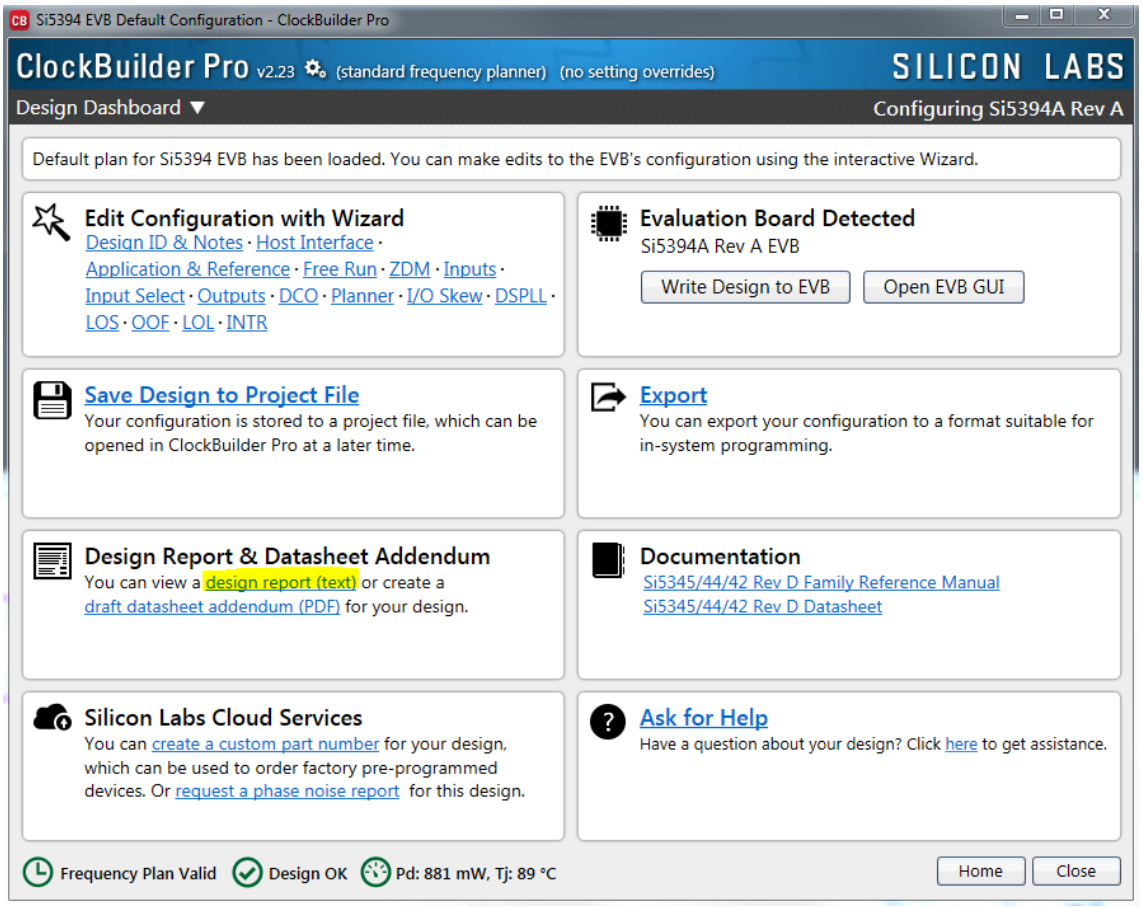

Figure 10.11. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

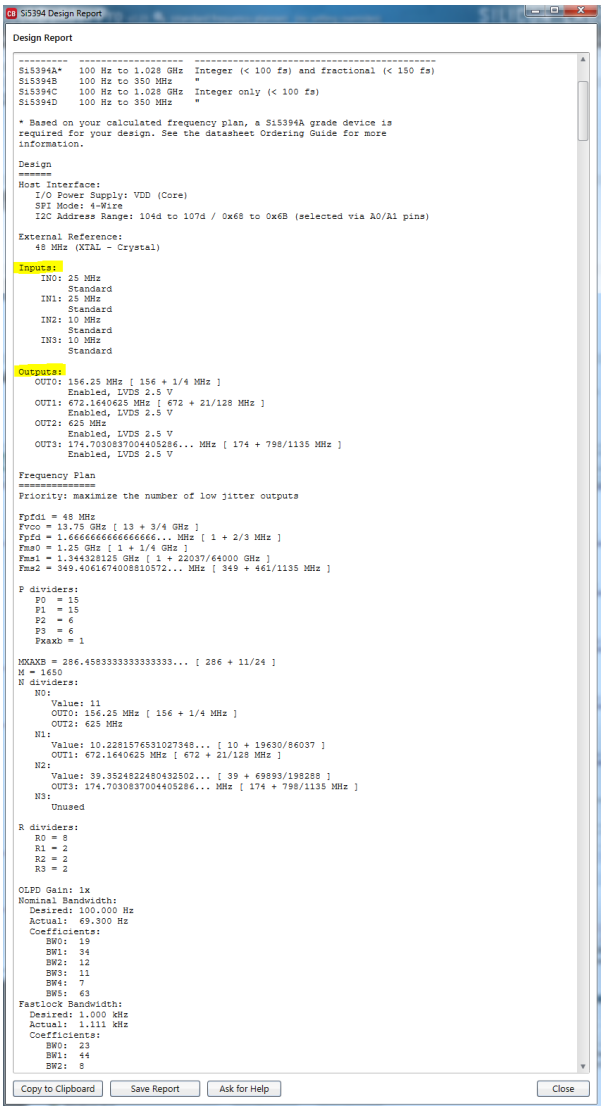

Figure 10.12. Design Report Window

10.4.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in “locked” mode.

10.5 Workflow Scenario 2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the “default” configuration using the CBPro Wizard, click on the links below under “Edit Configuration with Wizard”.

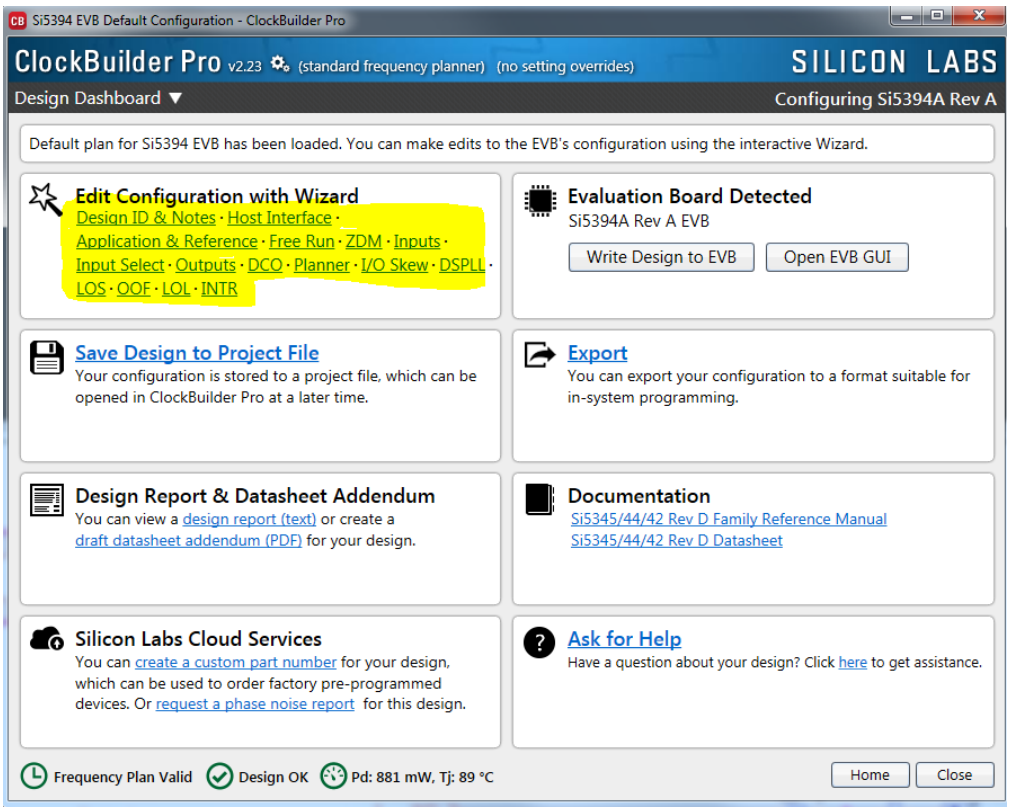

Figure 10.13. Edit Configuration with Wizard

You will now be taken to the Wizard’s step-by-step menus to allow you to change any of the default plan’s operating configurations.

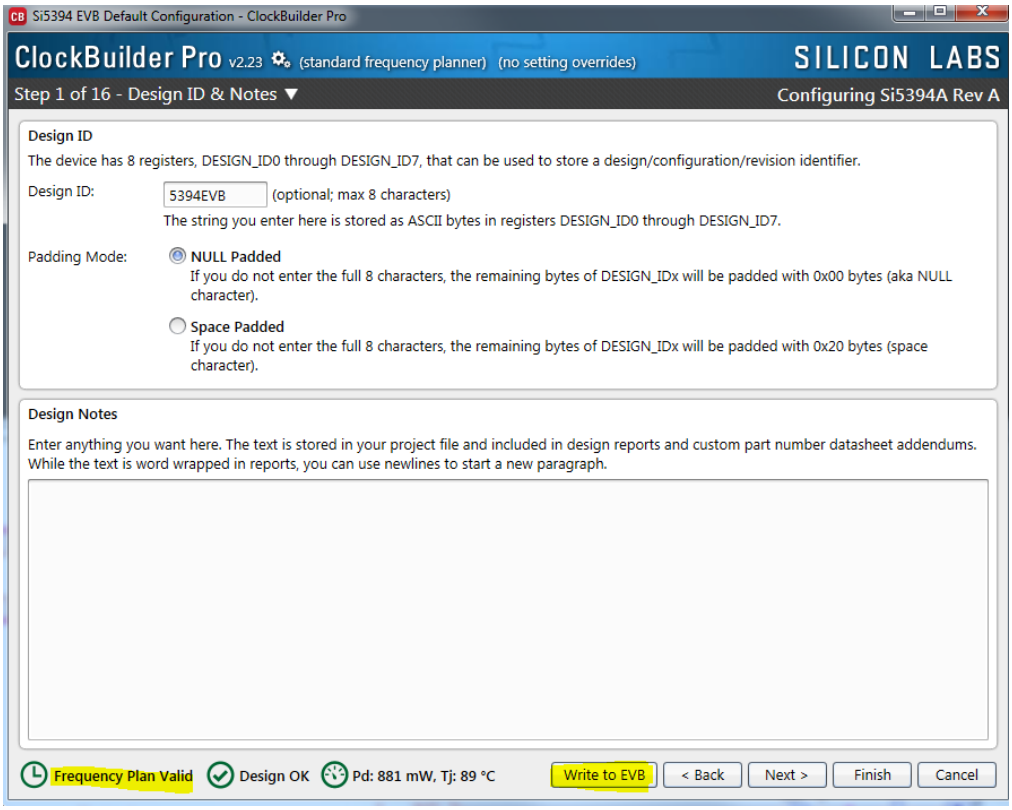

Figure 10.14. Design Wizard

Note that you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

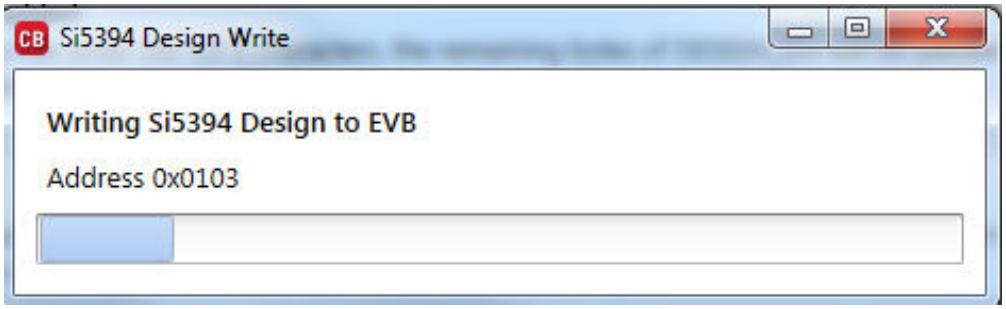

Figure 10.15. Writing Design Status

10.6 Workflow Scenario 3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.

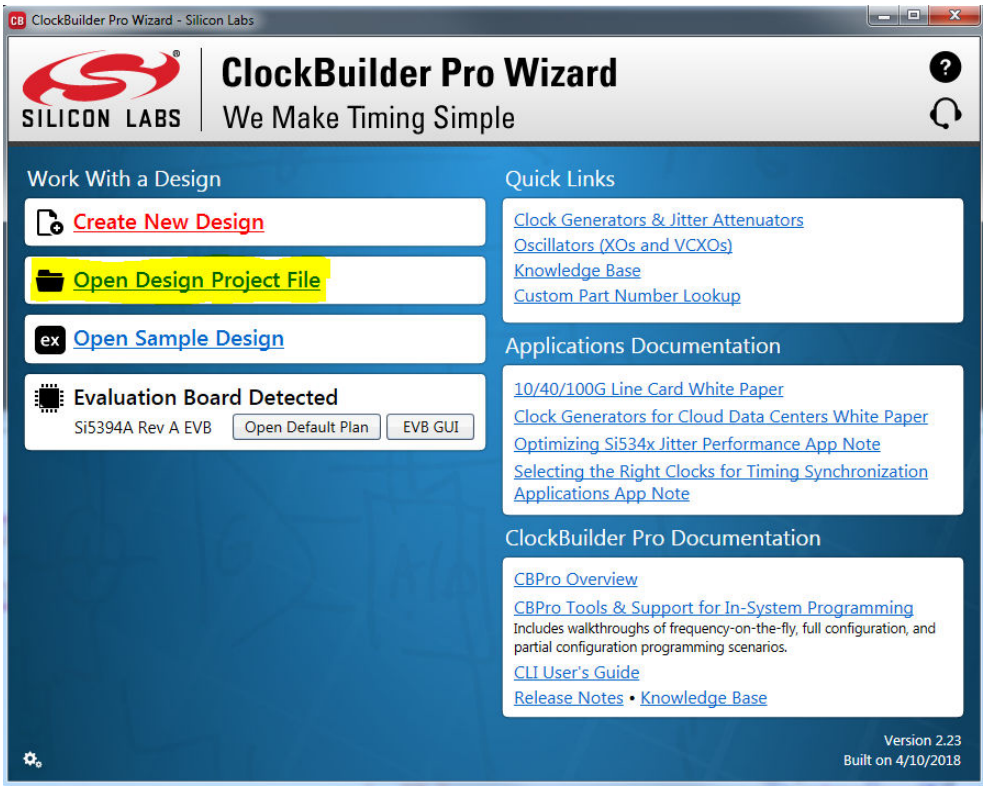

Figure 10.16. Open Design Project File

Locate your CBPro design file (*.slabtimeproj or *.sitproj file).design file in the Windows file browser.

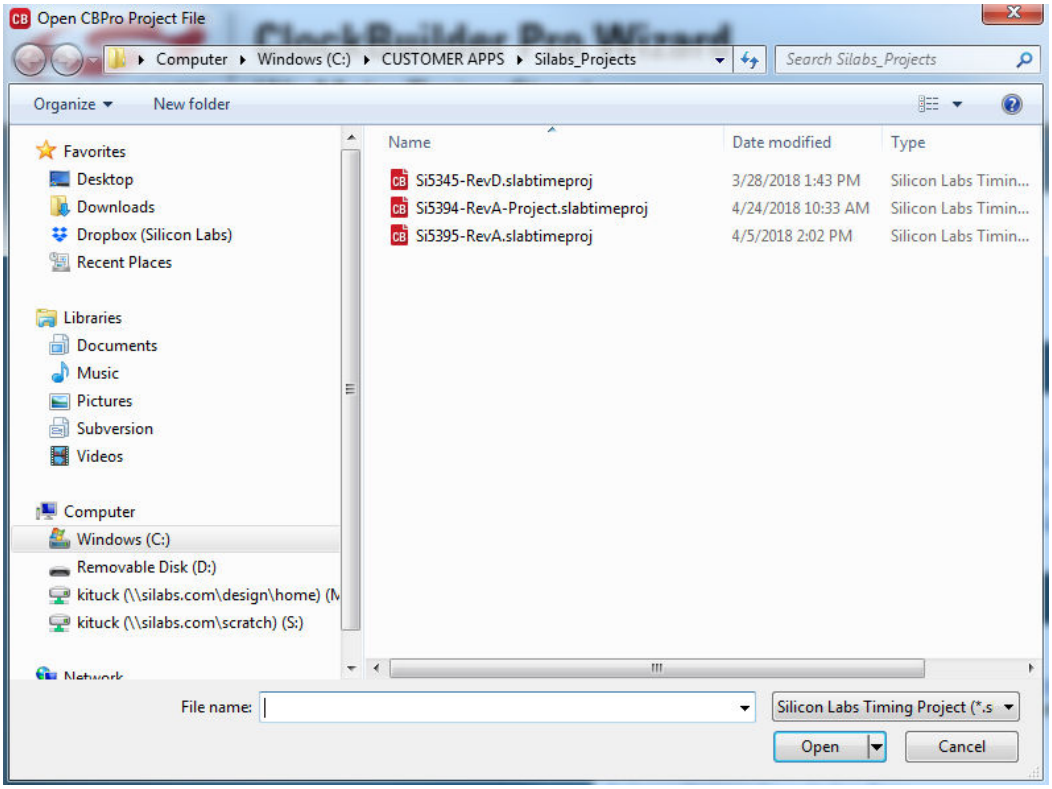

Figure 10.17. Browse to Project File

Select "Yes" when the WRITE DESIGN to EVB popup appears:

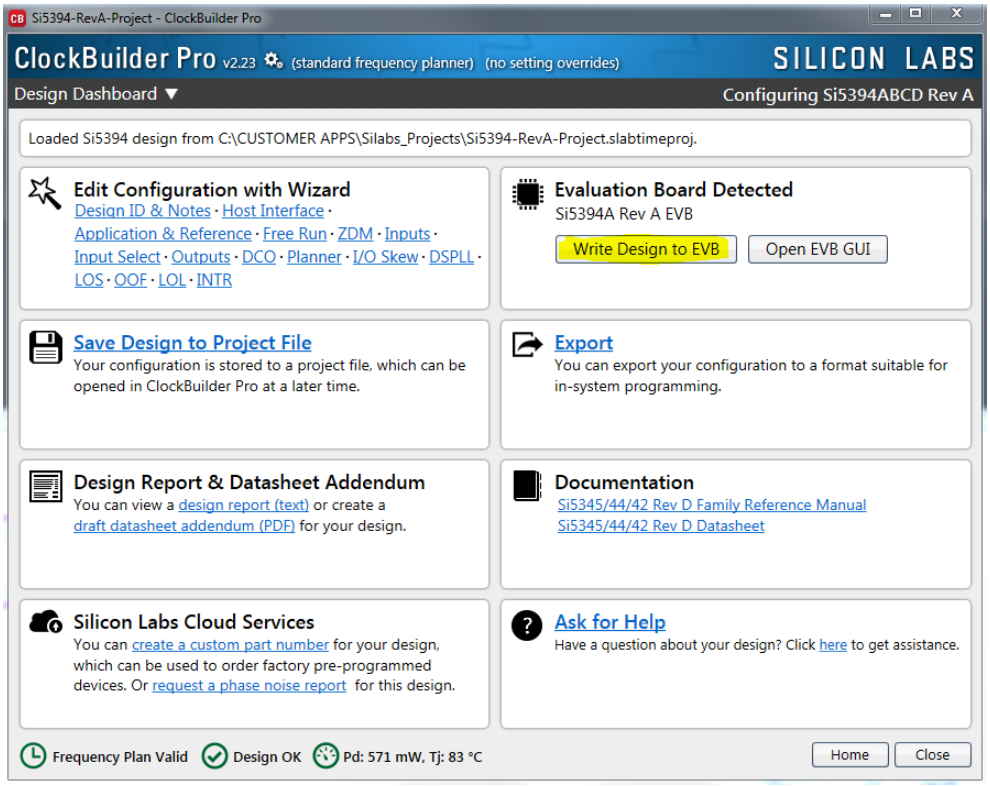

Figure 10.18. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

10.7 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:

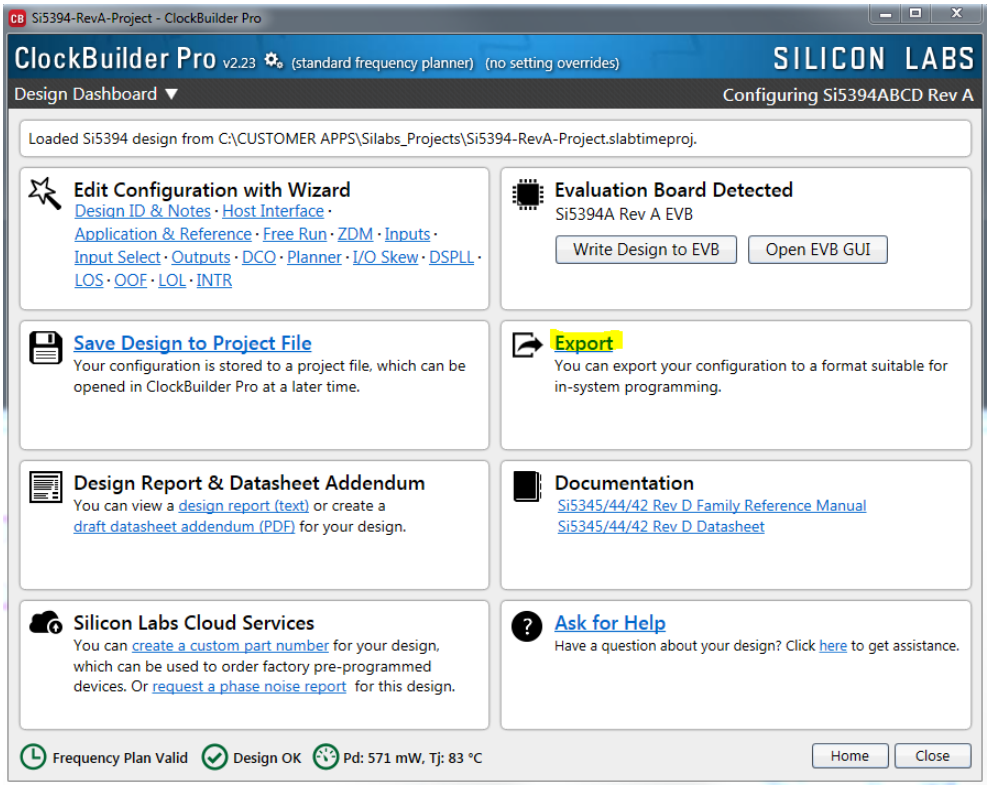

Figure 10.19. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming:

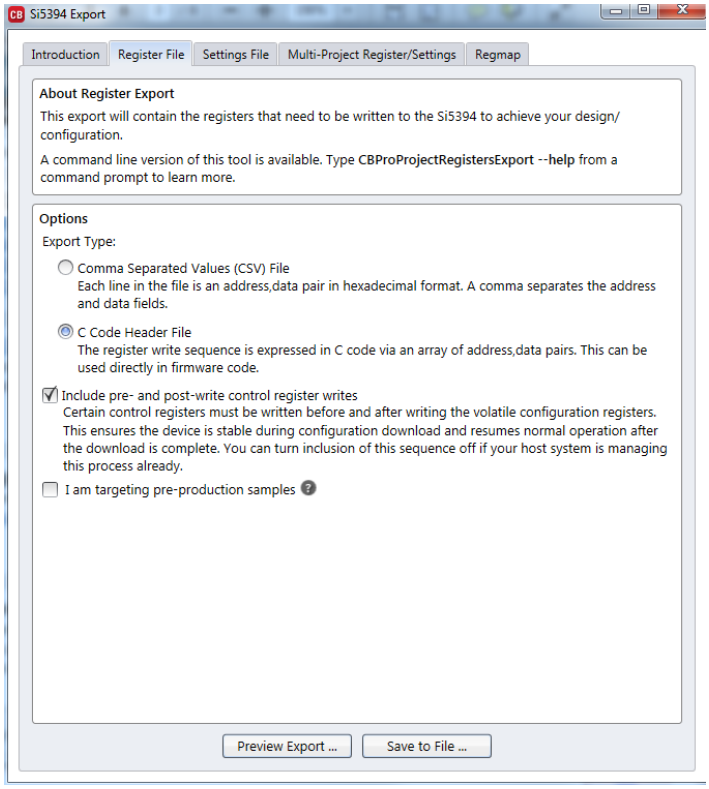

Figure 10.20. Export Settings

11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is **NOT** the same as writing a configuration into the Si5394 using ClockBuilder Pro on the Si5394 EVB. Writing a configuration into the EVB from ClockBuilderPro is done using Si5394 RAM space and can be done virtually unlimited numbers of times. Writing to OTP is limited as described below:

Refer to the Si5394 Family Reference Manual and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

12. Serial Device Communications

12.1 Onboard SPI Support

The MCU onboard the Si5394 EVB communicates with the Si5394 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5394 device is the SPI slave. The Si5394 device can also support a 2-wire I^2C serial interface, although the Si5394 EVB does NOT support the I^2C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I^2C.

12.2 External I^2C Support

I^2C can be supported if driven from an external I^2C controller. The serial interface signals between the MCU and Si5394 pass through shunts loaded on header J17. These jumper shunts must be installed in J17 for normal EVB operation using SPI with CBPro. If testing of I^2C operation via external controller is desired, the shunts in J17 can be removed thereby isolating the on-board MCU from the Si5394 device. The shunt at JP1 (I2C_SEL) must also be removed to select I^2C as Si5394 interface type. An external I^2C controller connected to the Si5394 side of J17 can then communicate to the Si5394 device. (For more information on I^2C signal protocol, please refer to the Si5394 data sheet.)

The figure below illustrates the J17 header schematic. J17 even numbered pins (2, 4, 6, etc.) connect to the Si5394 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J17 and JP1, I^2C operation should use J17 pin 4 (DUT_SDA_SDIO) as the I^2C SDA and J17 pin 8 (DUT_SCLK) as the I^2C SCLK. Please note the external I^2C controller will need to supply its own I^2C signal pull-up resistors.

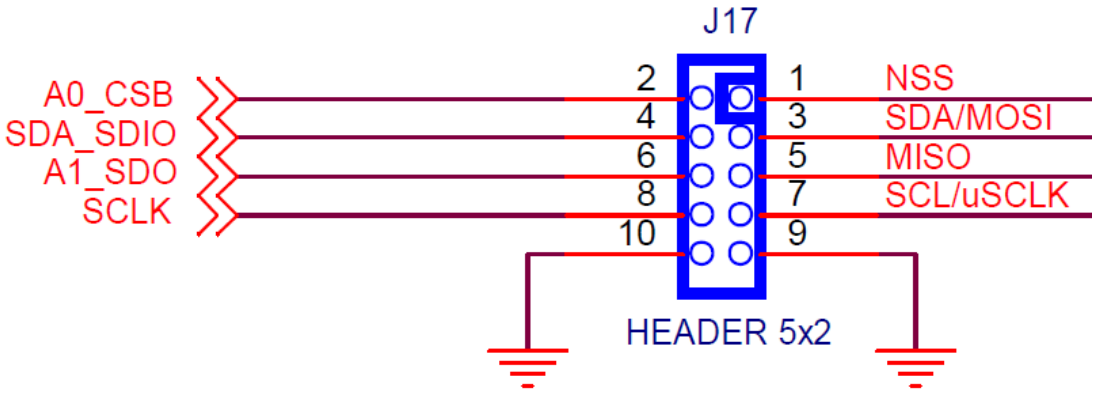

Figure 12.1. Serial Communications Header J17

13. Si5394 EVB Schematic, Layout, and Bill of Materials (BOM)

The Si5394 EVB Schematic, Layout, and Bill of Materials (BOM) can be found online: www.silabs.com/documents/public/schematic-files/si539x-design-files.zip

Note: Please be aware that the Si5394 EVB schematic is in **OrCad Capture** *hierarchical format* and not in a typical "flat" schematic format.

This document supports the evaluation board silkscreened Si5394 EVB for the following configurations as described in the table below. The data sheet documents the different Si5394 grades.

Table 13.1. Evaluation Board Configurations[1]

Config #	Eval Board Label	Si5394		Notes
		Grade	Revision	
1	Si5394A-A-EB	A	A	Crystal and related components installed.
2	Si5394P-A-EB	P	A	Crystal and related components installed. Only the DUT and label differ versus Si5394A-A-EB.
3	Si5394J-A-EB	J	A	No Crystal or related components installed. DUT and label also differ versus Si5394A-A-EB.
4	Si5394E-A-EB	E	A	No Crystal or related components installed. DUT and label also differ versus Si5394A-A-EB.

Note:

1. Note that it is not possible to load a Si5394A project onto an Si5394P-A-EB or an Si5394P project onto an Si5394A-A-EB. Use Si5394A/B/C/D plans for Si5394A-A-EB and Si5394P plans for Si5394P-A-EB. The same applies for the embedded reference parts. Use Si5394JKLM plans for Si5394J-A-EB and Si5394E plans for Si5394E-A-EB.