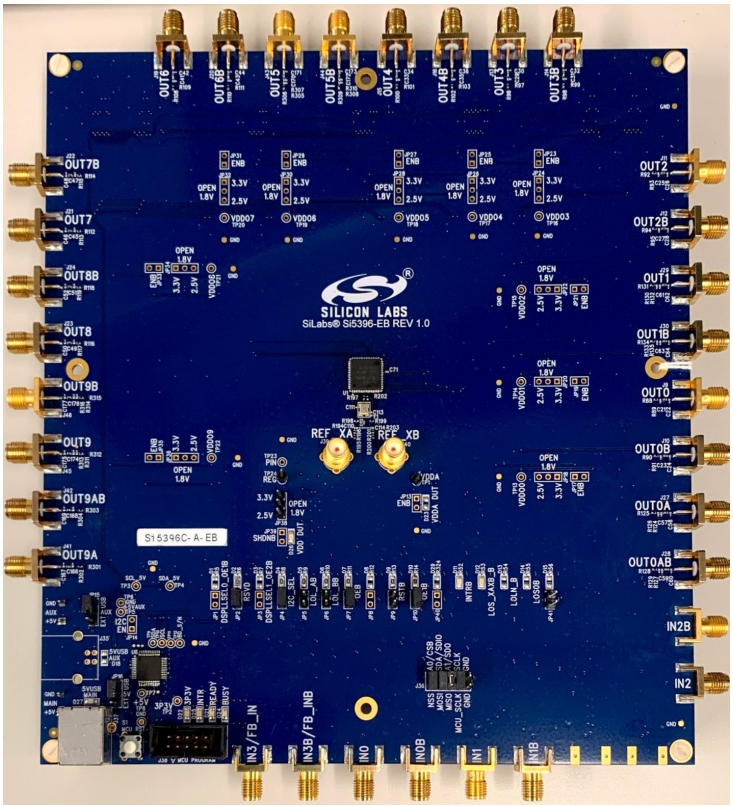
UG467: Si5396C/L Evaluation Board User's Guide

The Si5396C/L -EVB is used for evaluating the Si5396C/L Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier. The Grade C board requires an external reference. The Grade L board does not require a reference because it is internal to the chip. This user guide is intended for both the Si5396C and Si5396L EVBs. The device grade and revision is distinguished by a white 1 x 0.187 inch label installed in the lower left corner of the board. In the example below, the label, "SI5396C-A-EB", indicates the evaluation board has been assembled with an Si5396 device, Grade C, Revision A, installed. (For ordering purposes only, the terms “EB” and “EVB” refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.). Note that the Si5396A/B/J/K are all 4-output, 2 PLL devices in a 44-pin package, while the Si5396C/D/L/M are 12-output devices in a 64-pin package. This user guide is for the Si5396C/D/L/M grade 12-output, 2 PLL devices.



KEY FEATURES

- Si5396C-A-EVB for evaluating external reference versions Si5396C/D
- Si5396L-A-EVB for evaluating internal reference versions Si5396L/M
- Powered from USB port or external power supply
- Onboard 48 MHz XTAL or Reference SMA Inputs allow holdover mode of operation on the Si5396C
- ClockBuilder Pro® (CBPro) GUI programmable VDD supply allows device to operate from 3.3 V, 2.5 V, or 1.8 V
- CBPro GUI programmable VDDO supplies allow each of the outputs to have its own power supply voltage selectable from 3.3 V, 2.5 V, or 1.8 V
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5396C/L
- SMA connectors for input clocks, output clocks, and optional external timing reference clock to be used on external reference grades only

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1. Functional Block Diagram

Below is a functional block diagram of the Si5396C EVB. Keep in mind that the Grade L board does not use an external XTAL or reference and does not use the XA/XB pins. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See 3. Quick Start or 10.3 Overview of ClockBuilder Pro Applications for more information.

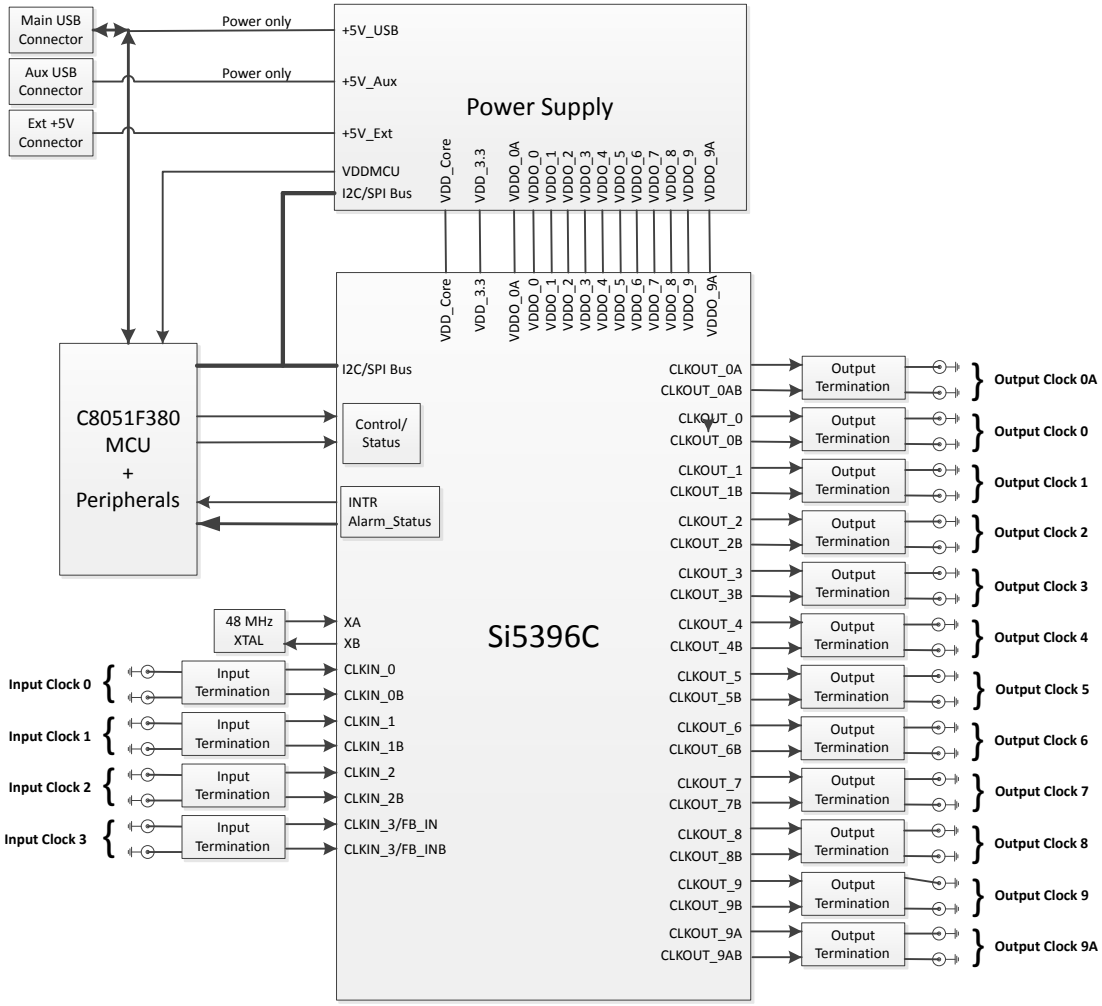


Figure 1.1. Si5396C EB Functional Block Diagram

2. Si5396C/L EVB Support Documentation and ClockBuilder Pro Software

Si5396C/L EVB schematics, BOMs, user’s guides, and software can be found online www.silabs.com/documents/public/schematic-files/si539x-design-files.zip

3. Quick Start

1. Install the ClockBuilder Pro desktop software from http://www.silabs.com/CBPro.
2. Connect a USB cable from Si5396C/L EVB to the PC where the software was installed.
3. Confirm jumpers are installed as shown in Table 4.1 Si5396C/L EVB Jumper Defaults[1] on page 6.
4. Launch the ClockBuilder Pro Software.
5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5396C/L EVB.
6. Find Si5396 data sheet: https://www.silabs.com/documents/public/data-sheets/si5397-96-a-datasheet.pdf

4. Jumper Defaults

Table 4.1. Si5396C/L EVB Jumper Defaults[1]

Location	Type	I= Installed 0 = Open	Location	Type	I = Installed 0 = Open
JP1	2-pin	O	JP23	2-pin	O
JP2	2-pin	I	JP24	3-pin	All Open
JP3	2-pin	O	JP25	2-pin	O
JP4	2-pin	I	JP26	3-pin	All Open
JP5	2-pin	I	JP27	2-pin	O
JP6	2-pin	I	JP28	3-pin	All Open
JP7	2-pin	I	JP29	2-pin	O
JP8	2-pin	O	JP30	3-pin	All Open
JP9	2-pin	O	JP31	2-pin	O
JP10	2-pin	I	JP32	3-pin	All Open
JP13	2-pin	O	JP33	2-pin	O
JP14	2-pin	I	JP34	3-pin	All Open
JP15	3-pin	1 to 2	JP35	2-pin	O
JP16	3-pin	1 to 2	JP36	3-pin	All Open
JP17	2-pin	O	JP38	3-pin	All Open
JP18	3-pin	All Open	JP39	2-pin	O
JP19	2-pin	O	JP40	2-pin	O
JP20	3-pin	All Open	JP41	2-pin	O
JP21	2-pin	O	J36	5 x 2 Hdr	All 5 installed
JP22	3-pin	All Open			

Note:

1. Refer to the Si5396C/L EVB schematics for the functionality associated with each jumper.

5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy

D27, D22, and D26 are illuminated when USB +5 V, Si5396 +3.3 V, and Si5396 VDD supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity.

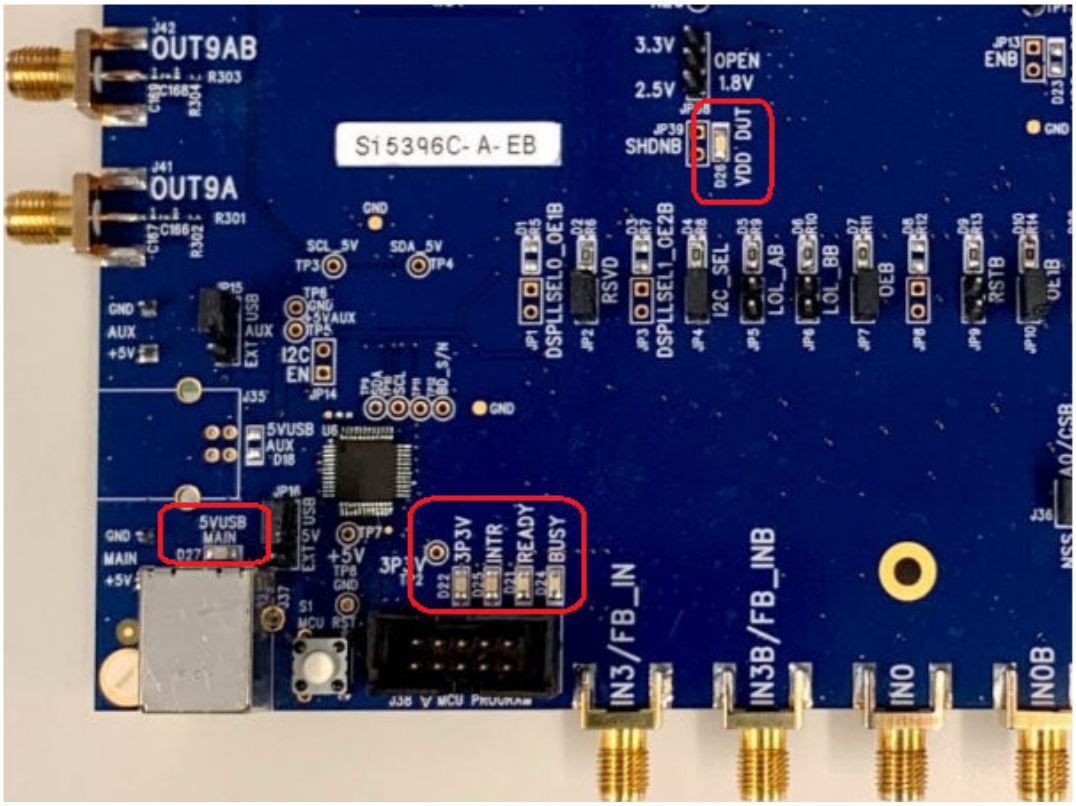


Figure 5.1. Status LEDs

6. External Reference Input (XA/XB)

An external reference (XTAL) is required in grade C in combination with the internal oscillator to produce an ultra-low-jitter reference clock for the DSPLL and to provide a stable reference for the free-run and holdover modes. To evaluate the device with a REFCLK, C111 and C113 must be populated and the XTAL removed (see the figure below). Also, R197 and R202 must be populated. The REFCLK can then be supplied to J39 and J40.

Note: For the Si5396L-A, which is the grade with the XTAL internal to the device, there will be no external XTAL supplied on the board and no input from Ref_XA and Ref_XB. In this case, it is advised that R197 and R202 are removed.

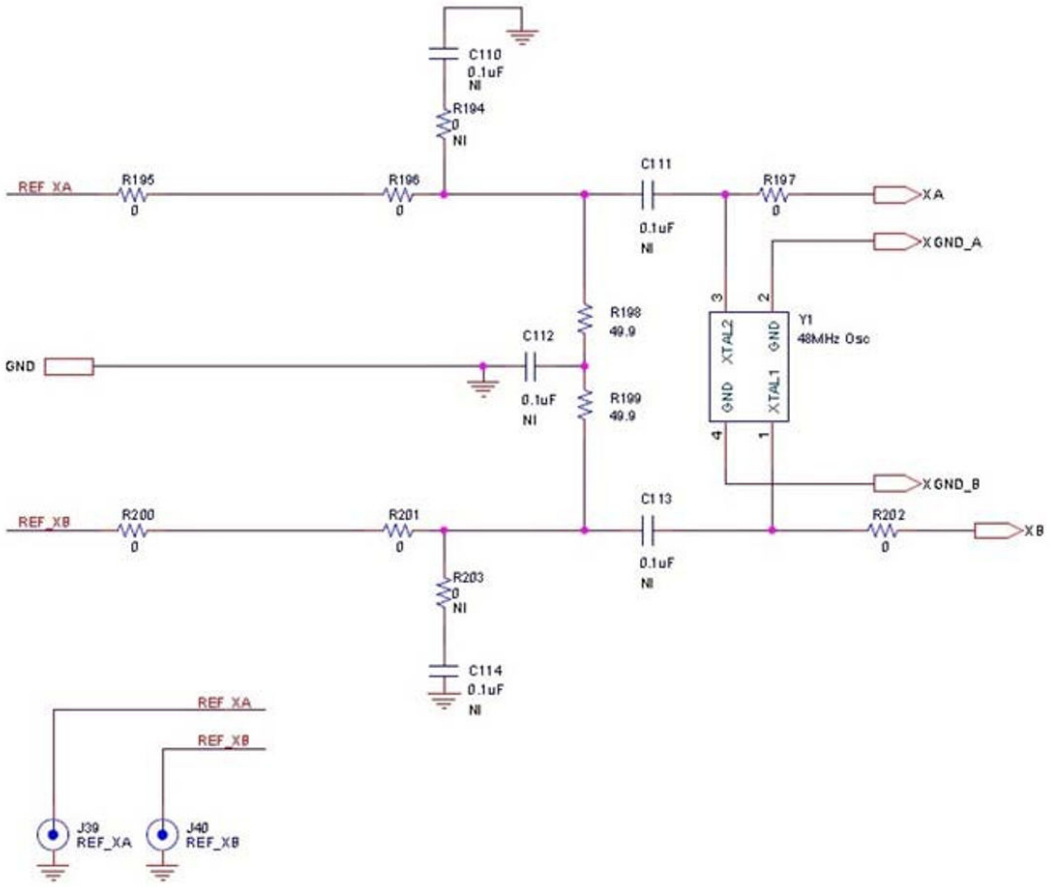


Figure 6.1. External Reference Input Circuit

7. Clock Input Circuits (INx/INxB)

The Si5396C/L EVB has eight SMA connectors (IN0, IN0B – IN3, IN3B) for receiving external clock signals. All input clocks are terminated as shown below. Note that input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, refer to the Si5396 reference manual.

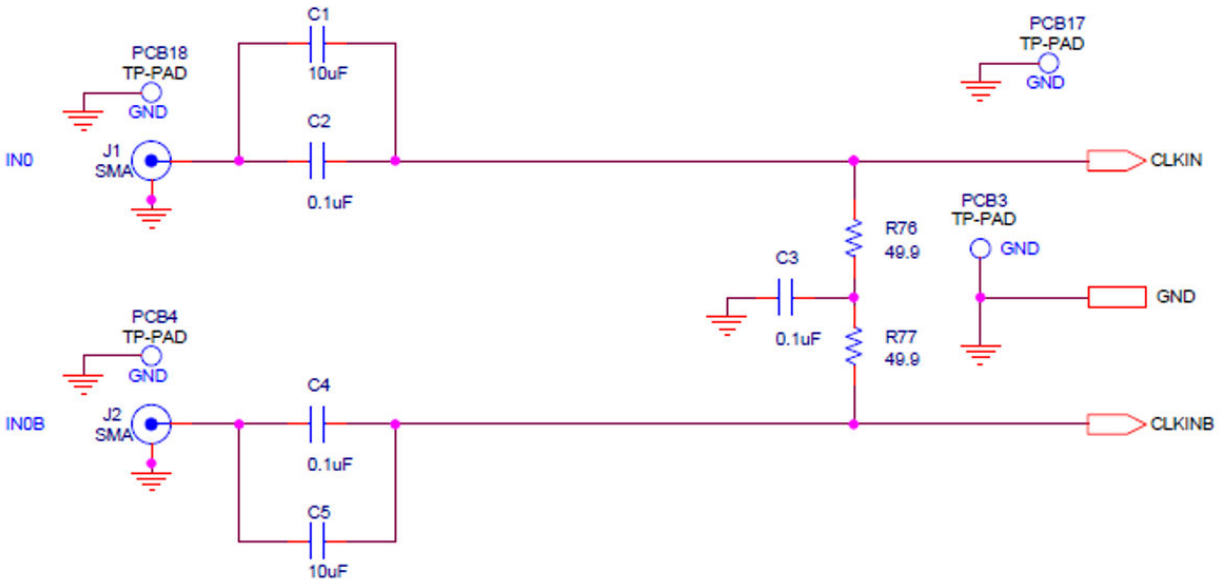


Figure 7.1. Input Clock Termination Circuit

8. Clock Output Circuits (OUTx/OUTxB)

Each of the 24 output drivers (12 differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5396C/L EVB provides pads for optional output termination resistors and/or low-frequency capacitors. Note that components with the schematic “NI” designation are not normally populated on the Si5396C/L EVB and provide locations on the PCB for optional dc/ac terminations by the end user.

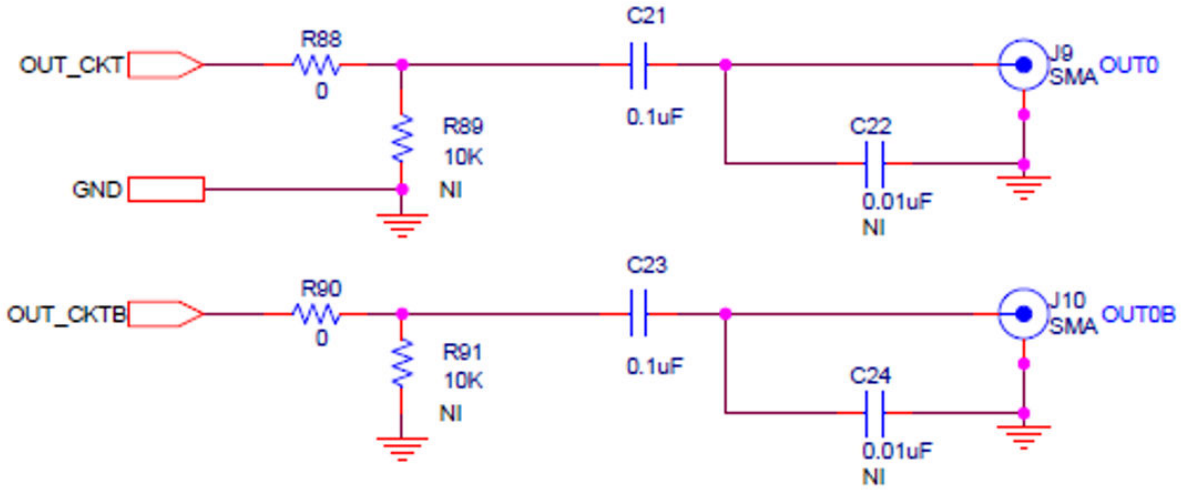


Figure 8.1. Output Clock Termination Circuit

9. Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any **Windows 7** (or above) PC, go to http://www.silabs.com/CBPro and download the ClockBuilder Pro software. Installation instructions and a user's guide for ClockBuilder Pro are available at the download link shown above.

10. Using the Si5396C/L EVB

10.1 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the EVB with a USB cable as shown in the figure below:

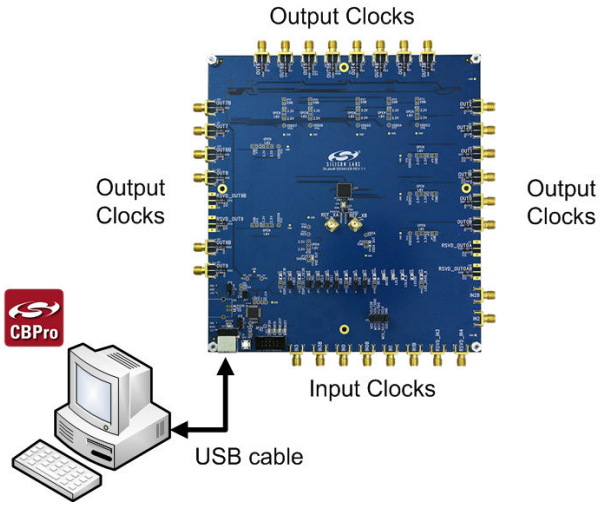


Figure 10.1. EVB Connection Diagram

10.2 Additional Power Supplies

Although additional power (besides the power supplied by the host PC's USB port) is not needed for most configurations, two additional +5 VDC power supplies (MAIN and AUX) can be connected to J33 and J34 (located on the bottom of the board, near the USB connector). Refer to the Si5396C/L EVB schematic for details.

The Si5396C/L EVB comes pre-configured with jumpers installed at JP15 and JP16 (pins 1–2 in both cases) to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

The following figure shows the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

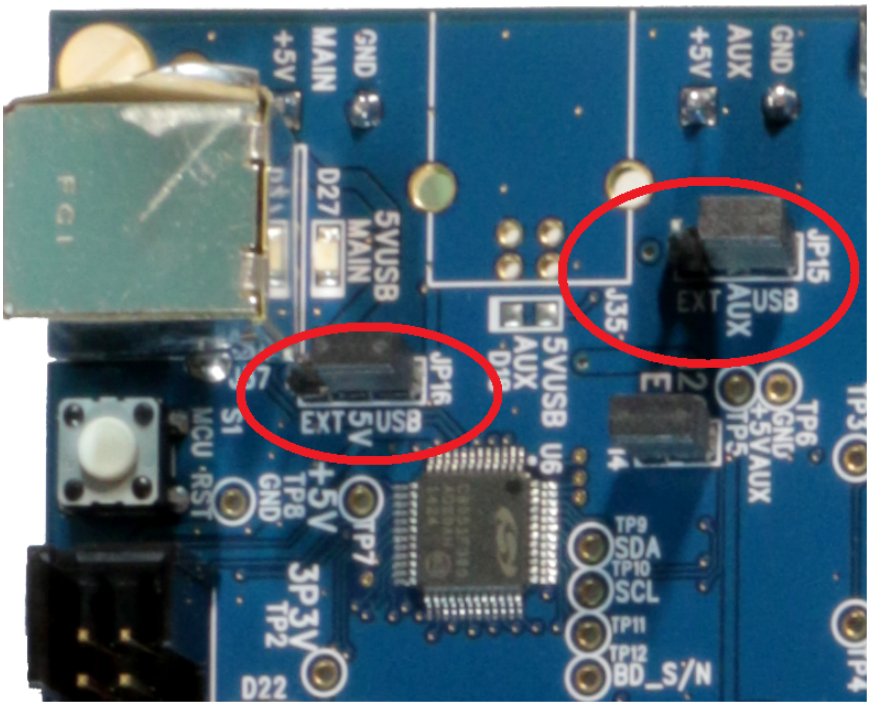


Figure 10.2. JP15–JP16 Standard Jumper Shunt Installation

The general guidelines for single USB power supply operation are as follows:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA, respectively, at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current-limited and need all output clock drivers enabled, reconfigure the EVB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
  - Connect an external +5 V power supply to terminal block J33 on the back side of the PCB.
  - Move the jumper at JP15 from pins 1–2 USB to pins 2–3 EXT.

10.3 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on the grade of your device and your version of ClockBuilder Pro. (The screen captures below were taken for a board labeled "SI5396C-A-EB".) The ClockBuilder Pro installer will install **two** main applications:

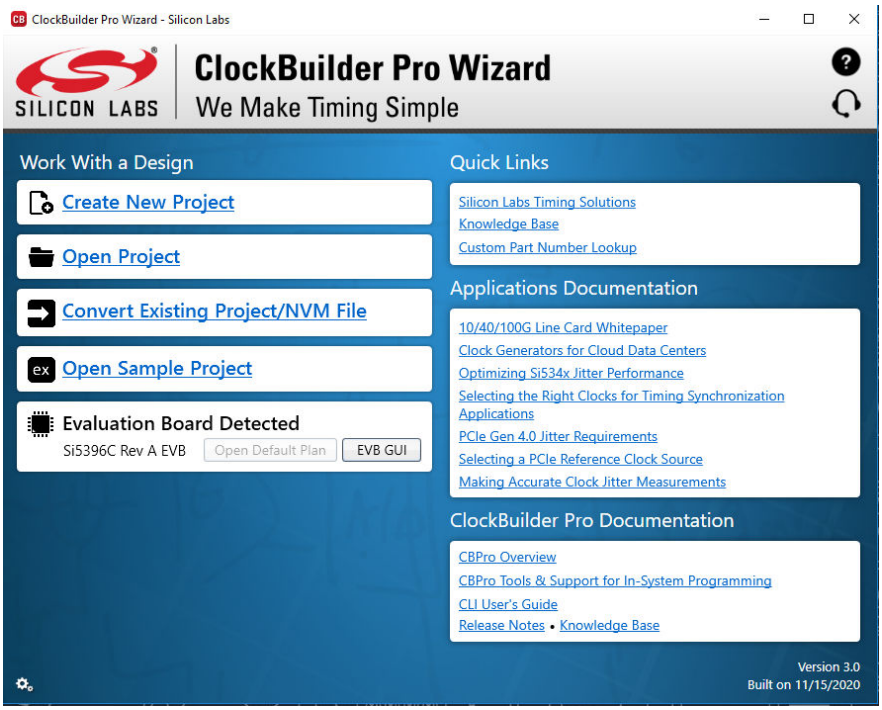


Figure 10.3. Application #1: ClockBuilder Pro Wizard

Use the CBPro wizard to:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming

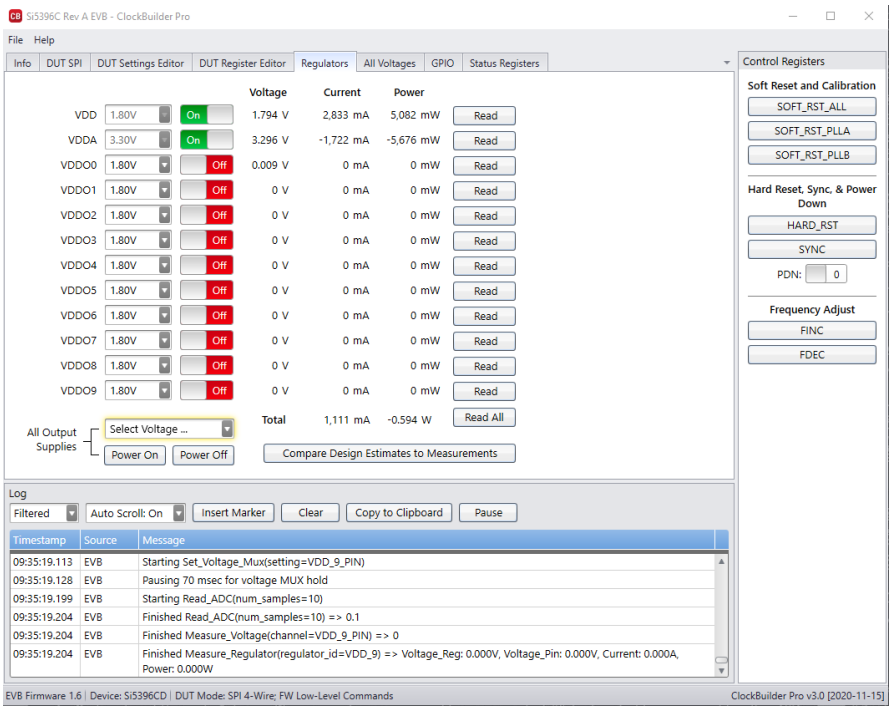


Figure 10.4. Application #2: EVBGUI

Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5396C)
- Control the EVB's regulators
- Monitor voltage, current, and power on the EVB

10.4 Common ClockBuilder Pro Workflow Scenarios

Three common workflow scenarios when using CBPro and the Si5396C/L EVB are:

- Workflow Scenario 1: Testing a Silicon Labs-Created Default Configuration
- Workflow Scenario 2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario 3: Testing a User-Created Device Configuration

Each workflow scenario is described in more detail in the following sections.

10.5 Workflow Scenario 1: Testing a Silicon Labs Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows:

Once the PC and EVB are connected, launch **ClockBuilder Pro** by clicking this icon on your PC's desktop:

Figure 10.5. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

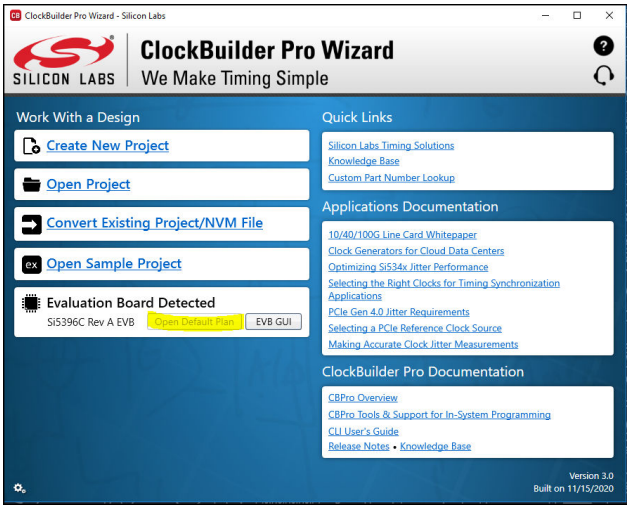


Figure 10.6. Open Default Plan

When you open the default plan (based on your EVB model number), a pop-up will appear:

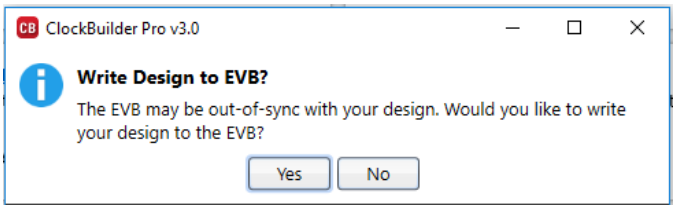


Figure 10.7. Write Design to EVB Dialog

Select “Yes” to write the default plan to the Si5396C/L device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

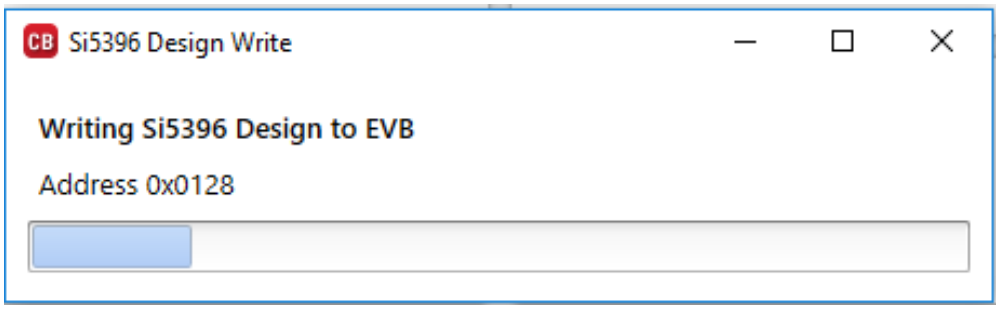


Figure 10.8. Writing Design Status

After CBPro writes the default plan to the EVB, click on “Open EVB GUI” as shown below:

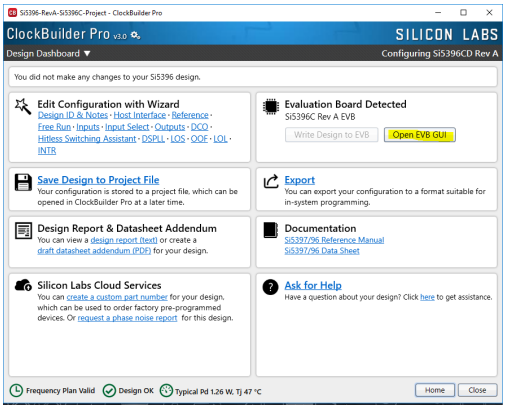


Figure 10.9. Open EVB GUI

The EVB GUI will appear. Note that all power supplies will be set to the values defined in the device's default CBPro project file created by Silicon Labs, as shown in the following figure:

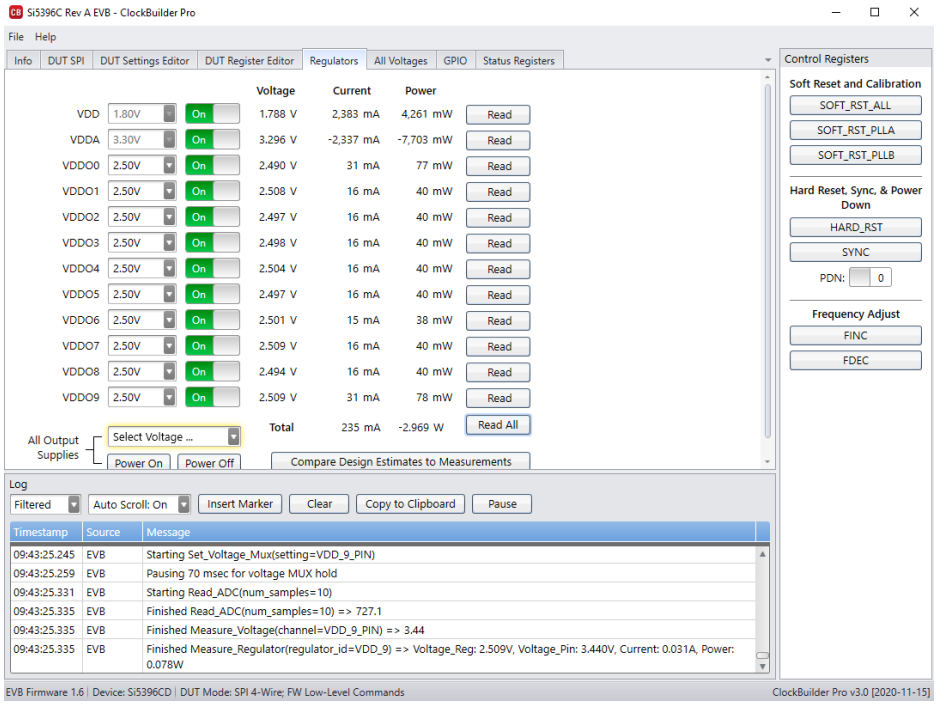


Figure 10.10. EVB GUI Window

10.5.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled “INx/INxB”) located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the highlighted "Read All" button and then reviewing the voltage, current, and power readings for each VDDx supply.

Note: Switching the VDD and VDDA supplies “Off” and then “On” will power-down and reset the DUT. Each time this is done, you must go back to the Wizard’s main menu and select “Write Design to EVB” to reload the Silicon Labs default plan into the DUT’s register space, as shown below.

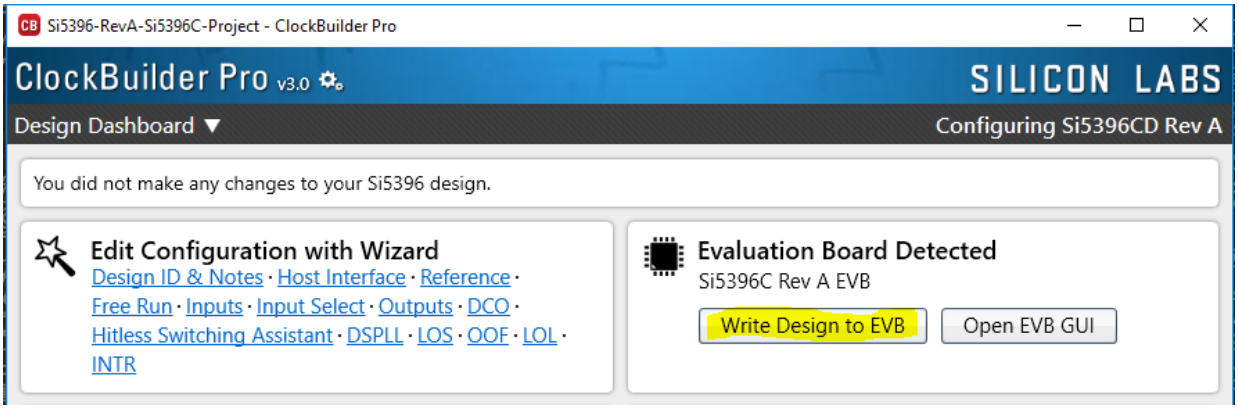


Figure 10.11. Write Design to EVB

Failure to perform this step will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify that the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

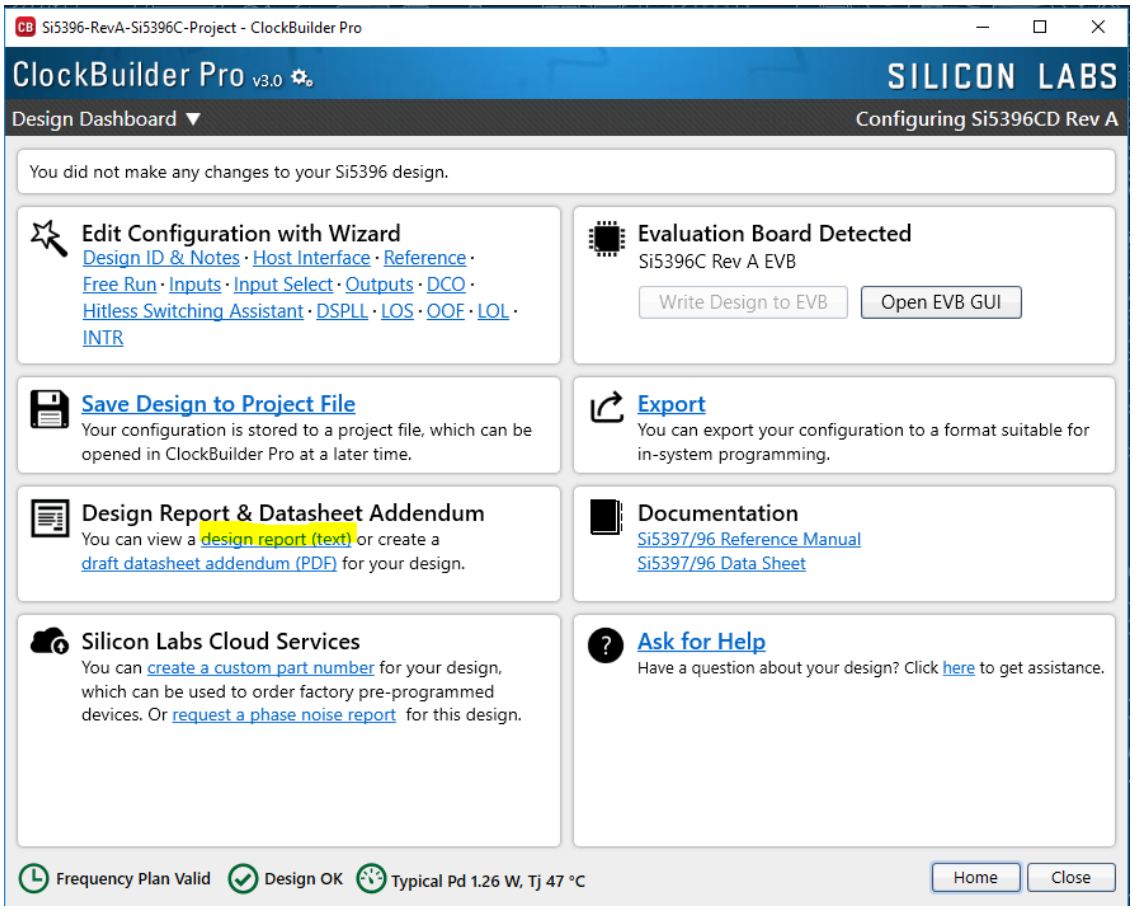


Figure 10.12. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

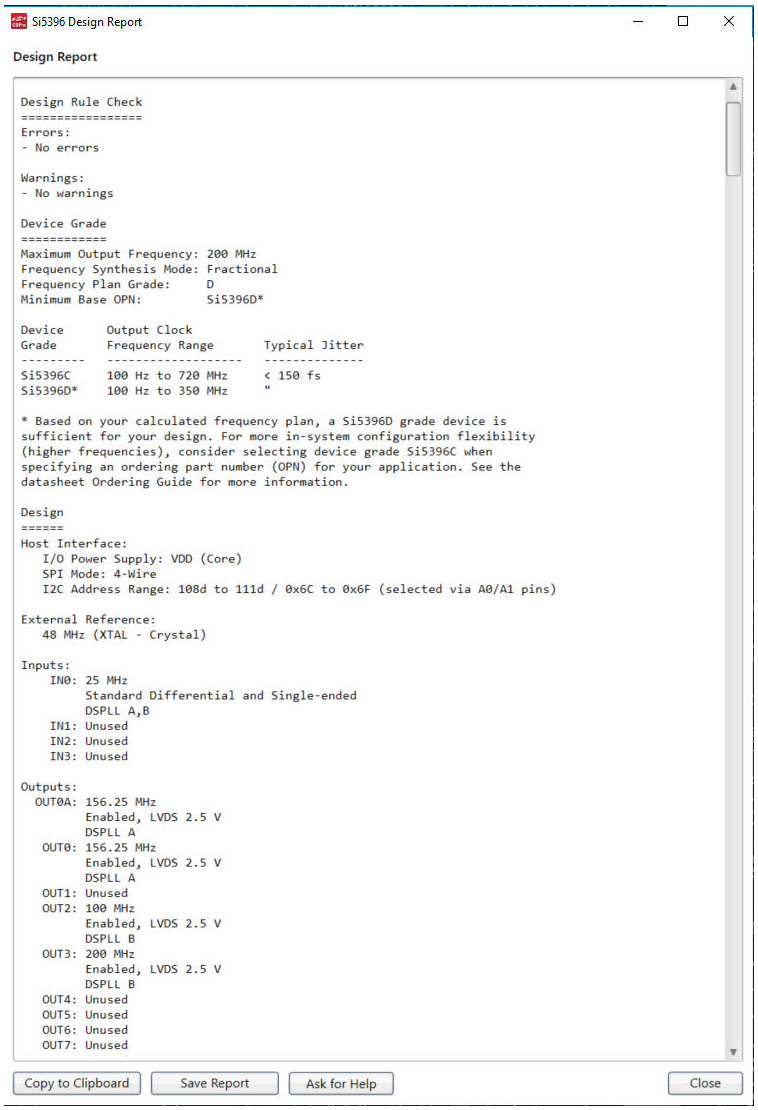


Figure 10.13. Design Report Window

10.5.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will run in “locked” mode.

10.6 Workflow Scenario 2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the “default” configuration using the CBPro Wizard, click on the links below under “Edit Configuration with Wizard”.

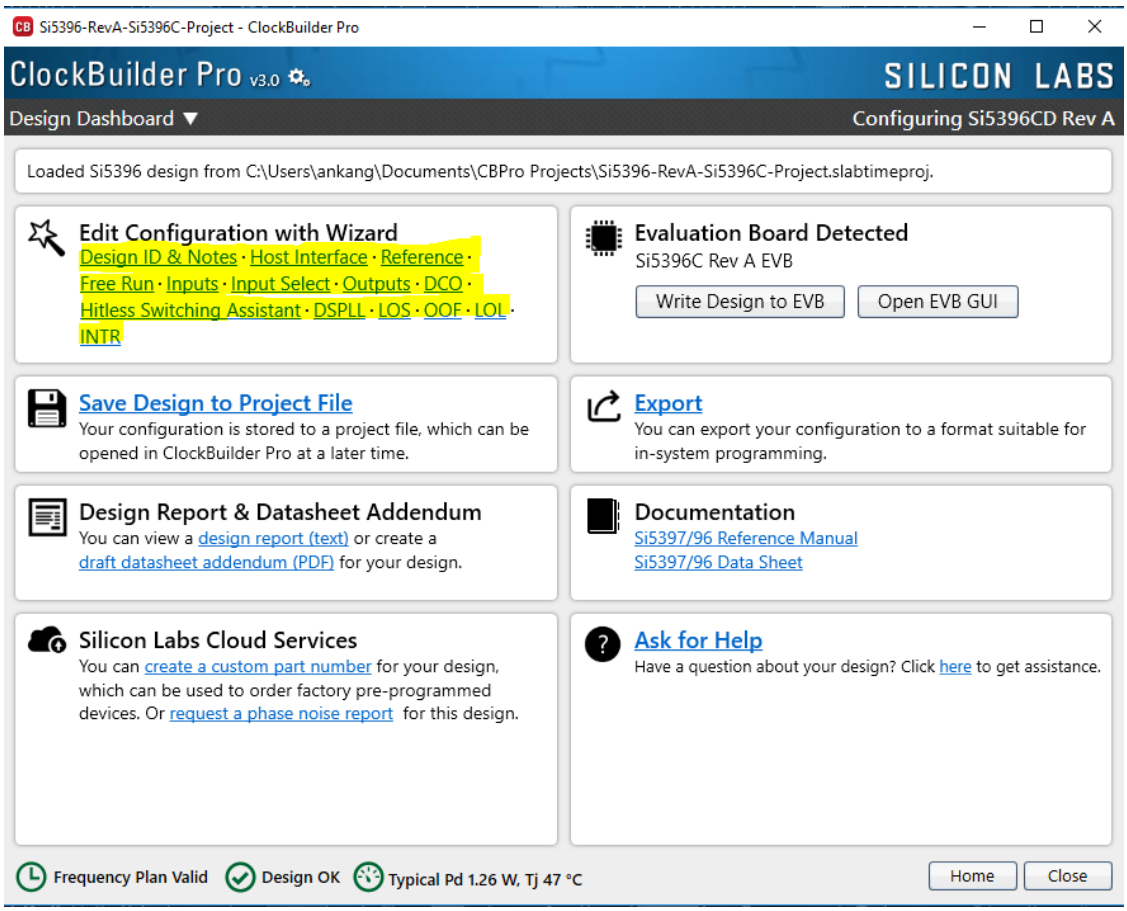


Figure 10.14. Edit Configuration with Wizard

You will now be taken to the Wizard’s step-by-step menus to allow you to change any of the default plan’s operating configurations.

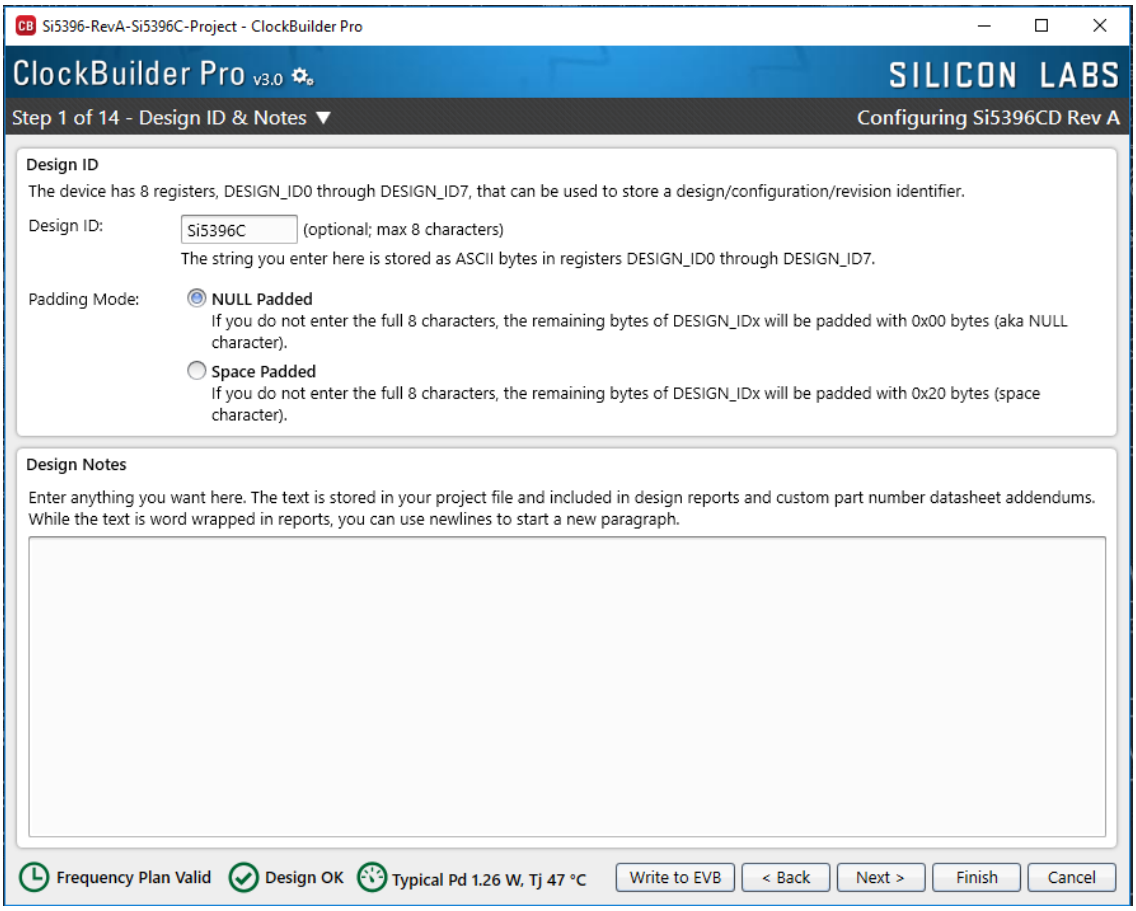


Figure 10.15. Design Wizard

Note that you can click on the icon in the lower left corner of the menu to confirm that your frequency plan is valid. After making your desired changes, click on Write to EVB to update the DUT and reconfigure your device real-time. The Design Write status window will appear each time you make a change.

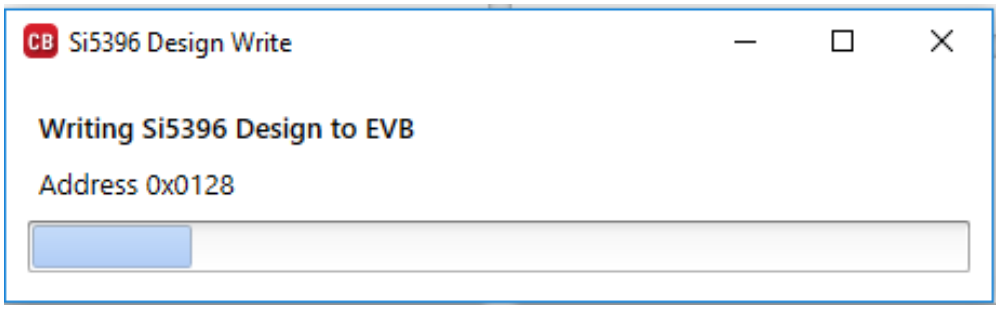


Figure 10.16. Writing Design Status

10.7 Workflow Scenario 3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking the icon on your desktop and selecting "Open Project".

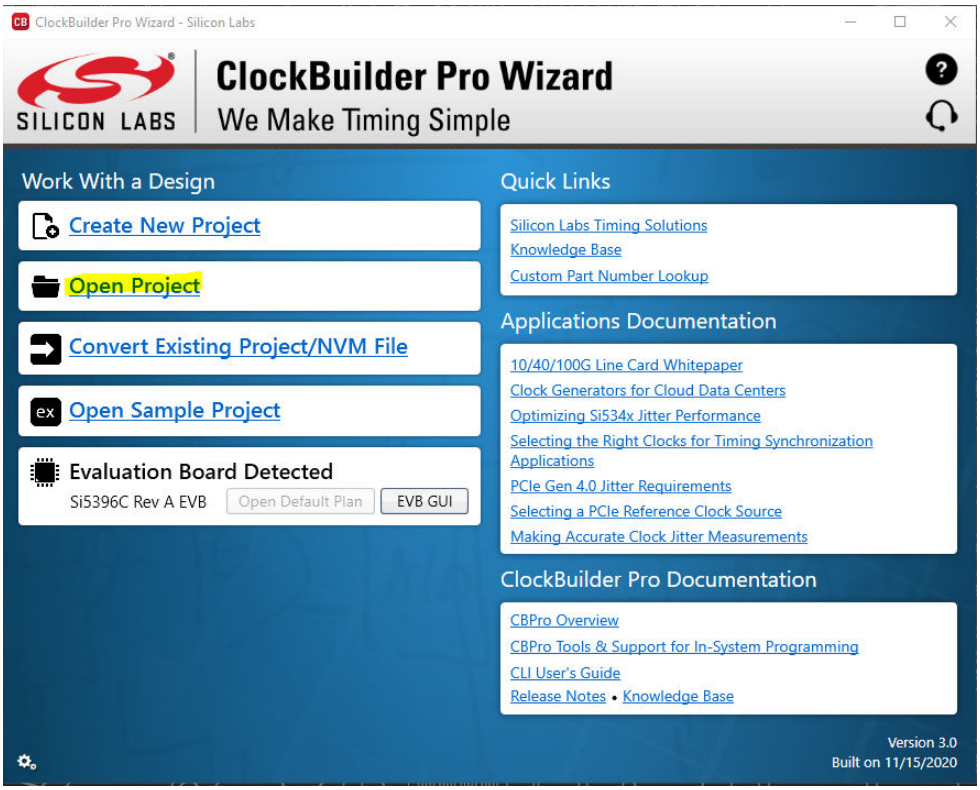


Figure 10.17. Open Design Project File

Locate your CBPro design file (*.slabtimeproj or *.sitproj file) in the Windows file browser.

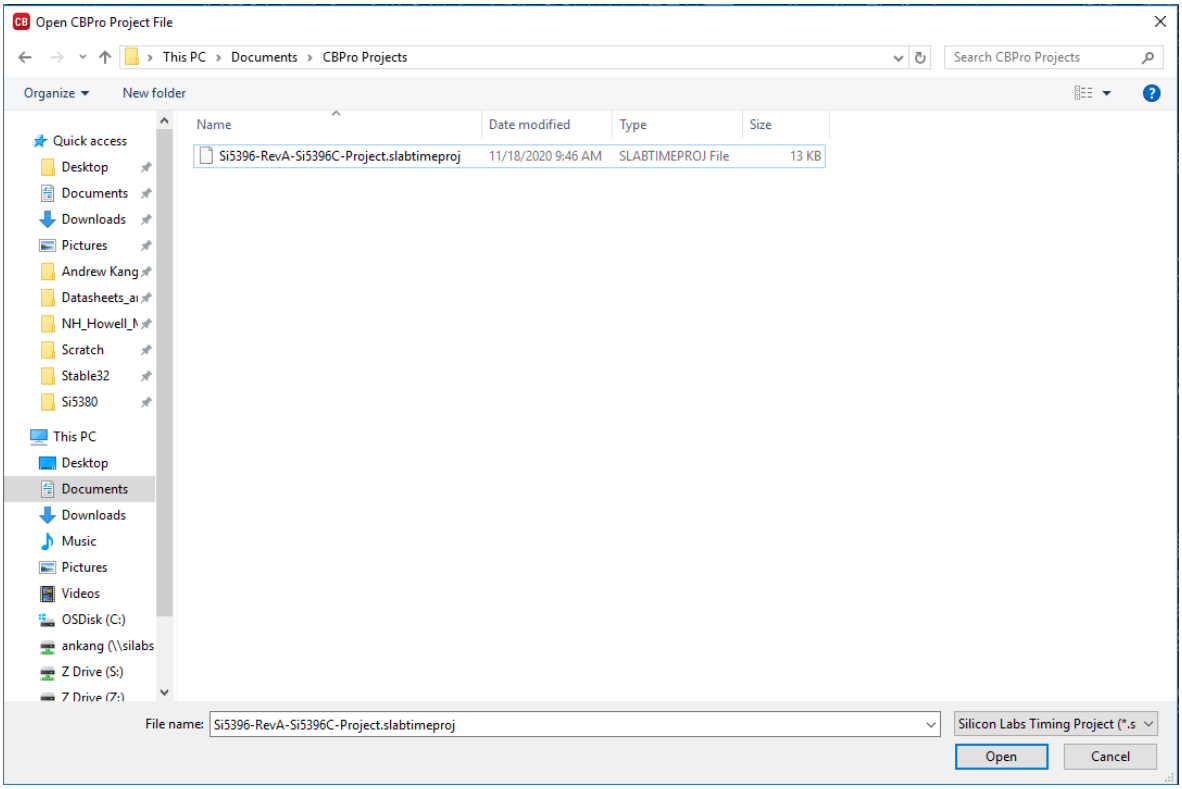


Figure 10.18. Browse to Project File

Select "Yes" when the "Write Design to EVB" popup appears:

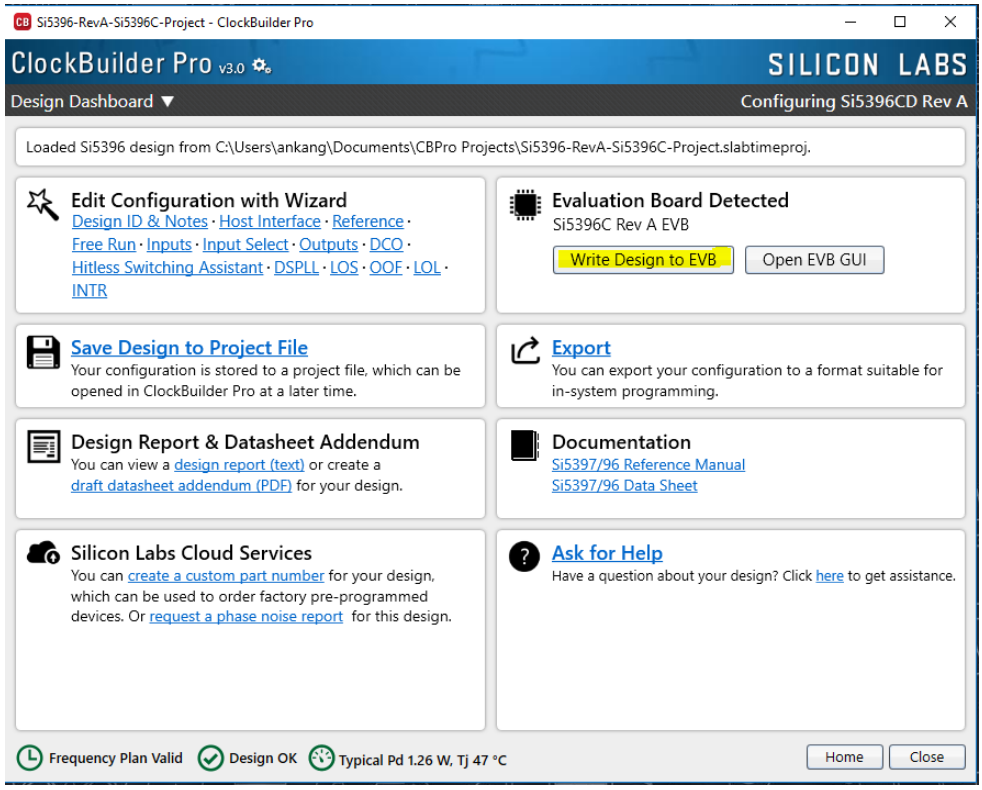


Figure 10.19. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

10.8 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:

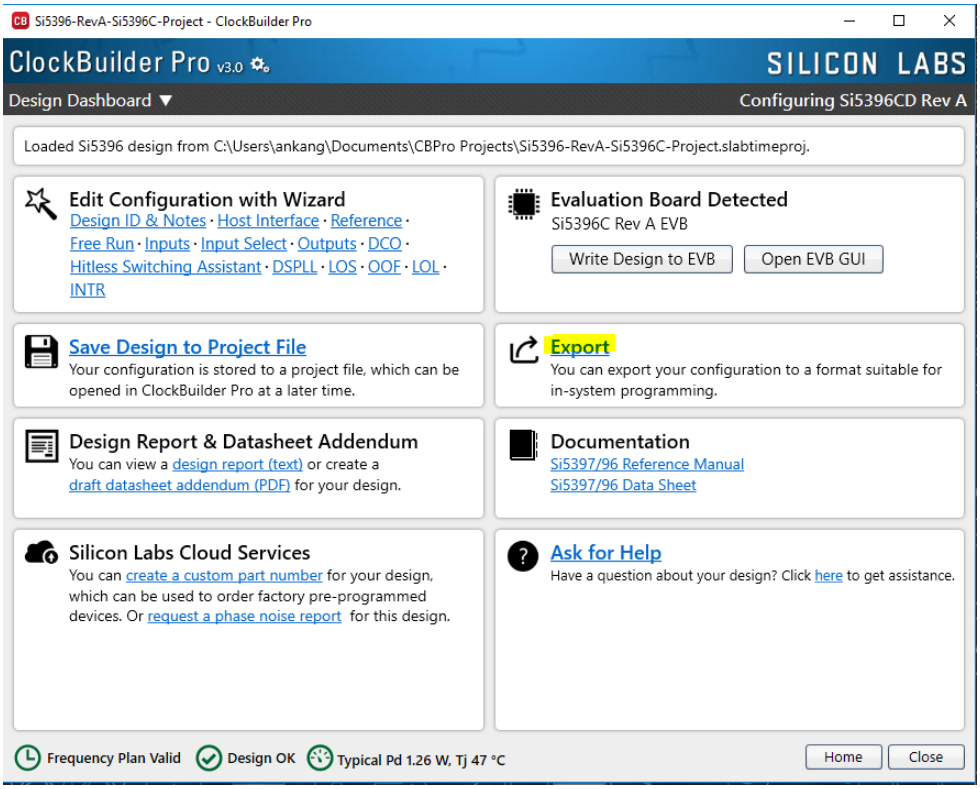


Figure 10.20. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming:

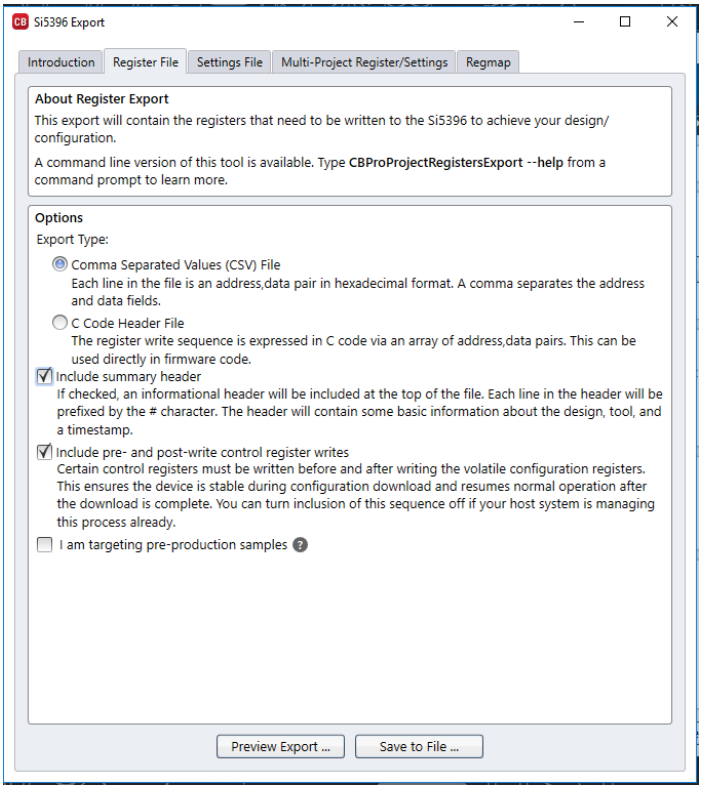


Figure 10.21. Export Settings

11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is **NOT** the same as writing a configuration into the Si5396C/L using ClockBuilder Pro on the Si5396C/L EVB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5396C/L RAM space and can be done virtually an unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si5397/96 Family Reference Manual and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the desired configuration is valid when choosing to write to OTP.

12. Serial Device Communications

12.1 Onboard SPI Support

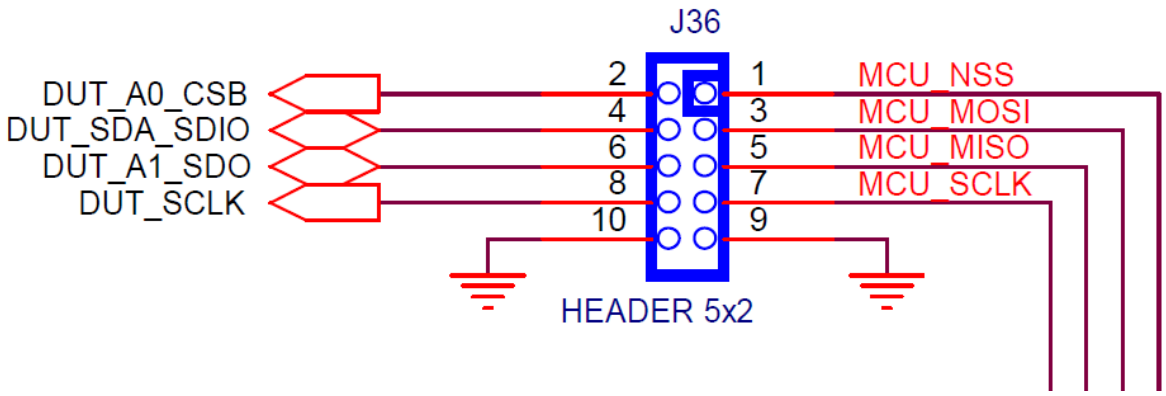
The MCU onboard the Si5396C/L EVB communicates with the Si5396C/L device through a 4-wire Serial Peripheral Interface (SPI) link. The MCU is the SPI master and the Si5396C/L device is the SPI slave. The Si5396C/L device can also support a 2-wire I^2C serial interface, although the Si5396C/L EVB does NOT support the I^2C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I^2C.

12.2 External I^2C Support

I^2C can be supported if driven from an external I^2C controller. The serial interface signals between the MCU and Si5396C/L pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I^2C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the onboard MCU from the Si5396C/L device. The shunt at J4 (I2C_SEL) must also be removed to select I^2C as Si5396C/L interface type. An external I^2C controller connected to the Si5396 side of J36 can then communicate to the Si5396C/L device. For more information on I^2C signal protocol, refer to the Si5396 data sheet.

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5396C/L device, and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. When the jumper shunts have been removed from J36 and J4, I^2C operation should use J36 pin 4 (DUT_SDA_SDIO) as the I2CSDA and J36 pin 8 (DUT_SCLK) as the I2CSCLK. Note that the external I^2C controller will need to supply its own I^2C signal pull-up resistors.

Figure 12.1. Serial Communications Header J36



13. Si5396C/L EVB Schematic, Layout, and Bill of Materials (BOM)

The Si5396C/L EVB Schematic, Layout, and Bill of Materials (BOM) can be found online at:

www.silabs.com/documents/public/schematic-files/si539x-design-files.zip

Note: Please be aware that the Si5396C/L EVB schematic is in **OrCad Capture** *hierarchical format* and not in a typical “flat” schematic format.

This document supports the evaluation board silkscreened Si5396C/L EVB for the following configurations as described in the table below. The data sheet documents the different Si5396C/L grades.

Table 13.1. Evaluation Board Configurations[1]

Config #	Eval Board Label	Si5396		Notes
		Grade	Revision	
1	Si5396C-A-EB	C	A	Crystal and related components installed.
2	Si5396L-A-EB	L	A	Crystal and related components not installed. Only the DUT and label differ versus Si5396C-A-EB.

Note:

1. Note that it is not possible to load an Si5396C project onto an Si5396L-A-EB or vice-versa. Use Si5396C/D plans for Si5396C-A-EB and Si5396L/M plans for Si5396L-A-EB.