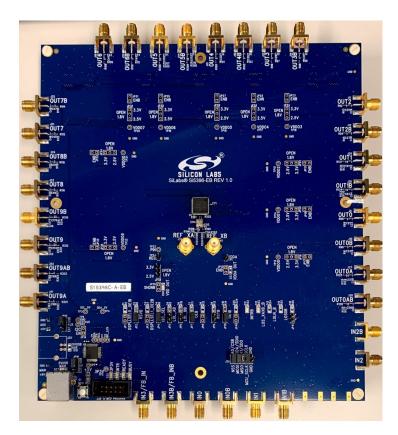


# UG467: Si5396C/L Evaluation Board User's Guide

The Si5396C/L -EVB is used for evaluating the Si5396C/L Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier. The Grade C board requires an external reference. The Grade L board does not require a reference because it is internal to the chip. This user guide is intended for both the Si5396C and Si5396L EVBs. The device grade and revision is distinguished by a white 1 x 0.187 inch label installed in the lower left corner of the board. In the example below, the label, "SI5396C-A-EB", indicates the evaluation board has been assembled with an Si5396 device, Grade C, Revision A, installed. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.). Note that the Si5396A/B/J/K are all 4-output, 2 PLL devices in a 44-pin package, while the Si5396C/D/L/M grade 12-output devices.



#### KEY FEATURES

- Si5396C-A-EVB for evaluating external reference versions Si5396C/D
- Si5396L-A-EVB for evaluating internal reference versions Si5396L/M
- Powered from USB port or external power supply
- Onboard 48 MHz XTAL or Reference SMA Inputs allow holdover mode of operation on the Si5396C
- ClockBuilder Pro<sup>®</sup> (CBPro) GUI programmable VDD supply allows device to operate from 3.3 V, 2.5 V, or 1.8 V
- CBPro GUI programmable VDDO supplies allow each of the outputs to have its own power supply voltage selectable from 3.3 V, 2.5 V, or 1.8 V
- CBPro GUI-controlled voltage, current, and power measurements of VDD and all VDDO supplies
- Status LEDs for power supplies and control/ status signals of Si5396C/L
- SMA connectors for input clocks, output clocks, and optional external timing reference clock to be used on external reference grades only

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# 1. Functional Block Diagram

Below is a functional block diagram of the Si5396C EVB. Keep in mind that the Grade L board does not use an external XTAL or reference and does not use the XA/XB pins. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See 3. Quick Start or 10.3 Overview of ClockBuilder Pro Applications for more information.

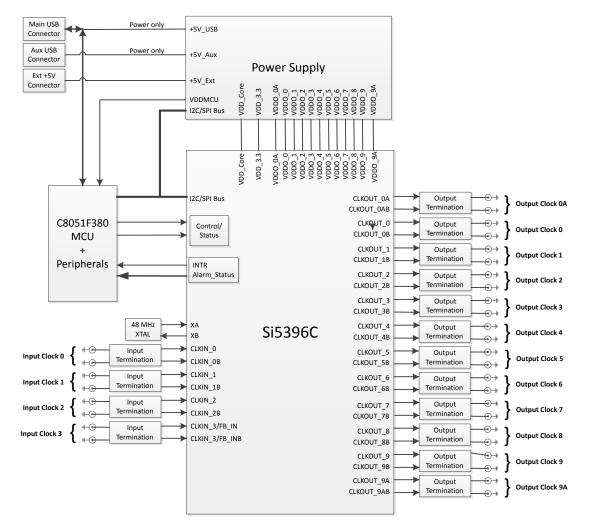


Figure 1.1. Si5396C EB Functional Block Diagram

UG467: Si5396C/L Evaluation Board User's Guide • Si5396C/L EVB Support Documentation and ClockBuilder Pro Software

# 2. Si5396C/L EVB Support Documentation and ClockBuilder Pro Software

Si5396C/L EVB schematics, BOMs, user's guides, and software can be found online www.silabs.com/documents/public/schematic-files/ si539x-design-files.zip

UG467: Si5396C/L Evaluation Board User's Guide • Quick Start

### 3. Quick Start

1. Install the ClockBuilder Pro desktop software from http://www.silabs.com/CBPro.

- 2. Connect a USB cable from Si5396C/L EVB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in Table 4.1 Si5396C/L EVB Jumper Defaults<sup>1</sup> on page 6.

4. Launch the ClockBuilder Pro Software.

- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5396C/L EVB.
- 6. Find Si5396 data sheet: https://www.silabs.com/documents/public/data-sheets/si5397-96-a-datasheet.pdf

# 4. Jumper Defaults

Location	Туре	l= Installed 0 = Open	Location	Туре	I = Installed 0 = Open
JP1	2-pin	0	JP23	2-pin	0
JP2	2-pin	I	JP24	3-pin	All Open
JP3	2-pin	0	JP25	2-pin	0
JP4	2-pin	I	JP26	3-pin	All Open
JP5	2-pin	I	JP27	2-pin	0
JP6	2-pin	I	JP28	3-pin	All Open
JP7	2-pin	I	JP29	2-pin	0
JP8	2-pin	0	JP30	3-pin	All Open
JP9	2-pin	0	JP31	2-pin	0
JP10	2-pin	I	JP32	3-pin	All Open
JP13	2-pin	0	JP33	2-pin	0
JP14	2-pin	I	JP34	3-pin	All Open
JP15	3-pin	1 to 2	JP35	2-pin	0
JP16	3-pin	1 to 2	JP36	3-pin	All Open
JP17	2-pin	0	JP38	3-pin	All Open
JP18	3-pin	All Open	JP39	2-pin	0
JP19	2-pin	2-pin O JP40	2-pin	0	
JP20	3-pin	All Open	JP41	2-pin	0
JP21	2-pin	0	J36	5 x 2 Hdr	All 5 installed
JP22	3-pin	All Open			

# Table 4.1. Si5396C/L EVB Jumper Defaults<sup>1</sup>

1. Refer to the Si5396C/L EVB schematics for the functionality associated with each jumper.

# 5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy

D27, D22, and D26 are illuminated when USB +5 V, Si5396 +3.3 V, and Si5396 VDD supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity.

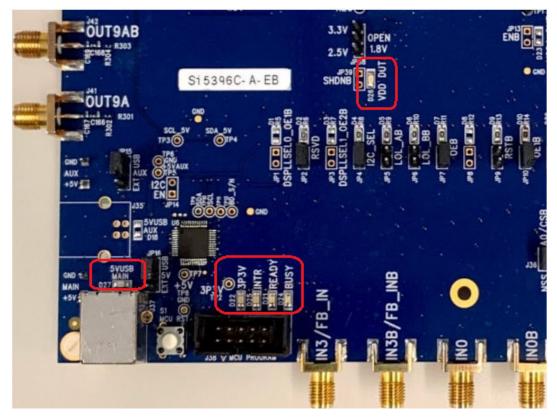


Figure 5.1. Status LEDs

UG467: Si5396C/L Evaluation Board User's Guide • External Reference Input (XA/XB)

# 6. External Reference Input (XA/XB)

An external reference (XTAL) is required in grade C in combination with the internal oscillator to produce an ultra-low-jitter reference clock for the DSPLL and to provide a stable reference for the free-run and holdover modes. To evaluate the device with a REFCLK, C111 and C113 must be populated and the XTAL removed (see the figure below). Also, R197 and R202 must be populated. The REFCLK can then be supplied to J39 and J40.

**Note:** For the Si5396L-A, which is the grade with the XTAL internal to the device, there will be no external XTAL supplied on the board and no input from Ref\_XA and Ref\_XB. In this case, it is advised that R197 and R202 are removed.

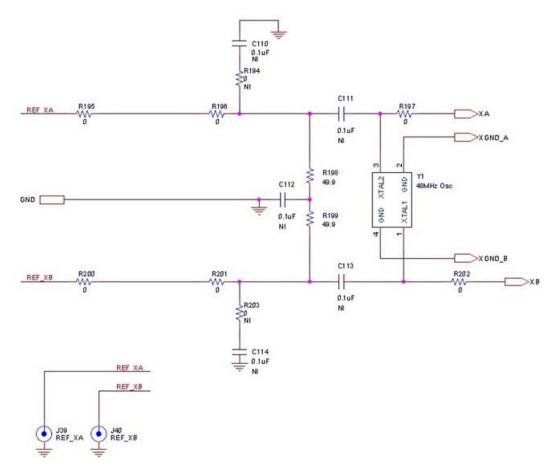


Figure 6.1. External Reference Input Circuit

UG467: Si5396C/L Evaluation Board User's Guide • Clock Input Circuits (INx/INxB)

# 7. Clock Input Circuits (INx/INxB)

The Si5396C/L EVB has eight SMA connectors (IN0, IN0B – IN3, IN3B) for receiving external clock signals. All input clocks are terminated as shown below. Note that input clocks are ac-coupled and 50  $\Omega$  terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, refer to the Si5396 reference manual.

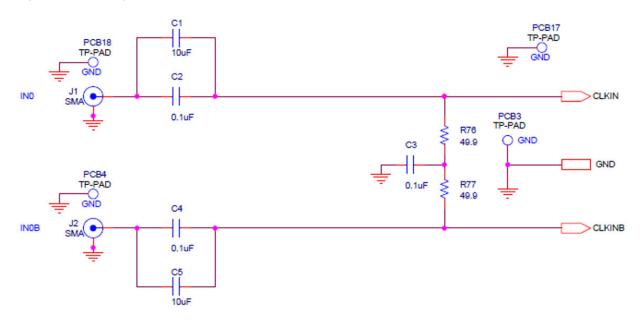


Figure 7.1. Input Clock Termination Circuit

UG467: Si5396C/L Evaluation Board User's Guide • Clock Output Circuits (OUTx/OUTxB)

# 8. Clock Output Circuits (OUTx/OUTxB)

Each of the 24 output drivers (12 differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5396C/L EVB provides pads for optional output termination resistors and/or low-frequency capacitors. Note that components with the schematic "NI" designation are not normally populated on the Si5396C/L EVB and provide locations on the PCB for optional dc/ac terminations by the end user.

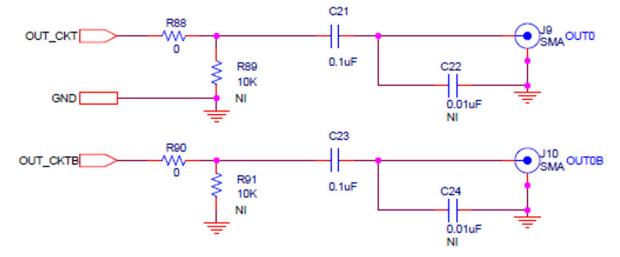


Figure 8.1. Output Clock Termination Circuit

UG467: Si5396C/L Evaluation Board User's Guide • Installing ClockBuilder Pro Desktop Software

# 9. Installing ClockBuilder Pro Desktop Software

To install the CBPro software on any **Windows 7** (or above) PC, go to http://www.silabs.com/CBPro and download the ClockBuilder Pro software. Installation instructions and a user's guide for ClockBuilder Pro are available at the download link shown above.

UG467: Si5396C/L Evaluation Board User's Guide • Using the Si5396C/L EVB

## 10. Using the Si5396C/L EVB

#### 10.1 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the EVB with a USB cable as shown in the figure below:

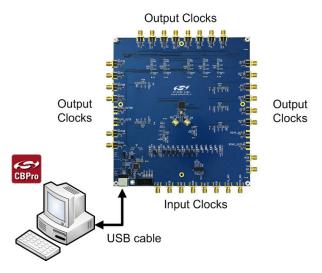


Figure 10.1. EVB Connection Diagram

#### **10.2 Additional Power Supplies**

Although additional power (besides the power supplied by the host PC's USB port) is not needed for most configurations, two additional +5 VDC power supplies (MAIN and AUX) can be connected to J33 and J34 (located on the bottom of the board, near the USB connector). Refer to the Si5396C/L EVB schematic for details.

The Si5396C/L EVB comes pre-configured with jumpers installed at JP15 and JP16 (pins 1–2 in both cases) to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

The following figure shows the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.

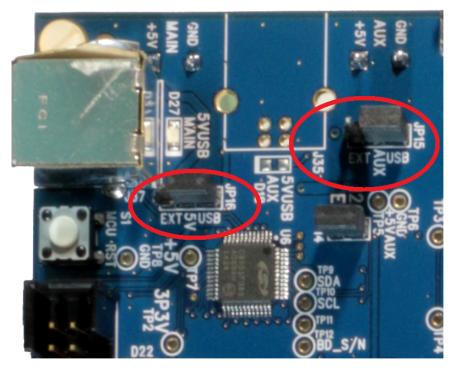


Figure 10.2. JP15–JP16 Standard Jumper Shunt Installation

The general guidelines for single USB power supply operation are as follows:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA, respectively, at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current-limited and need all output clock drivers enabled, reconfigure the EVB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
  - Connect an external +5 V power supply to terminal block J33 on the back side of the PCB.
  - Move the jumper at JP15 from pins 1-2 USB to pins 2-3 EXT.

#### **10.3 Overview of ClockBuilder Pro Applications**

**Note:** The following instructions and screen captures may vary slightly depending on the grade of your device and your version of ClockBuilder Pro. (The screen captures below were taken for a board labeled "SI5396C-A-EB".) The ClockBuilder Pro installer will install **two** main applications:

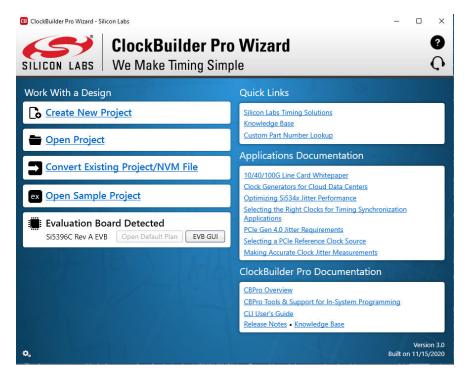


Figure 10.3. Application #1: ClockBuilder Pro Wizard

#### Use the CBPro wizard to:

- · Create a new design
- · Review or edit an existing design
- · Export: create in-system programming

cog Filtered Auto Scroll: On Timestamp Source Messag 09:35:19.113 EV8 Starting 09:35:19.128 EV8 Pausing	or DUT Register Editor Voltage	Regulators All	Voltages GPIC	_		
VDD         1.80V           VDDA         3.30V           VDDA         3.30V           VDDO         1.80V           VDDOS         1.80V           Supplies         Pereeron           Cog         1.80V           Supplies         Suplicitore           Supplies         Suplicitore <td< th=""><th></th><th>Regulators All</th><th>Valtages CDIC</th><th></th><th></th><th></th></td<>		Regulators All	Valtages CDIC			
VDDA         3.30V           VDD00         1.80V           VDD01         1.80V           VDD02         1.80V           VDD03         1.80V           VDD03         1.80V           VDD04         1.80V           VDD05         1.80V           VDD06         1.80V           VDD07         1.80V           VDD08         1.80V           VDD09         1.80V           VD009         1.80V           VD009         1.80V           Power On         1.80V           Supplies         Power On           Power Supplies         Power Supplies           Supplies         Ever Supplies           Supplies         Ever Supplies	Voltage		voltages GPIC	O Status Registers	~	Control Registers
VDDA         3.30V           VDDO0         1.80V           VDD01         1.80V           VDD02         1.80V           VDD03         1.80V           VDD03         1.80V           VDD03         1.80V           VDD04         1.80V           VDD05         1.80V           VDD06         1.80V           VDD07         1.80V           VDD08         1.80V           VDD09         1.80V           VD009         1.80V           VD009 <td></td> <td>Current</td> <td>Power</td> <td></td> <td></td> <td>Soft Reset and Calibra</td>		Current	Power			Soft Reset and Calibra
VDDA         3.30V           VDDA         3.30V           VDDO0         1.80V           VDD01         1.80V           VDD02         1.80V           VDD03         1.80V           VDD04         1.80V           VDD05         1.80V           VDD06         1.80V           VDD07         1.80V           VDD08         1.80V           VDD09         1.80V           VD009         1.80V           9         1.80V           9         1.81V           9         1.81V           9         1.81V           9         1.81V </td <td>On 1.794 V</td> <td>2.833 mA</td> <td>5.082 mW</td> <td>Read</td> <td></td> <td>SOFT_RST_ALL</td>	On 1.794 V	2.833 mA	5.082 mW	Read		SOFT_RST_ALL
VDD00         1.80V           VDD01         1.80V           VDD02         1.80V           VDD03         1.80V           VDD03         1.80V           VDD03         1.80V           VDD04         1.80V           VDD05         1.80V           VDD06         1.80V           VDD07         1.80V           VDD09         1.80V           VDD09         1.80V           VDD09         1.80V           VDD09         1.80V           VDD09         1.80V           VD009         1.80V           VD009         1.80V           VD009         1.80V           VD009         1.80V           Supplies         Select Voltage           Power On         9           9         1.810 IS         1.810 Starting           9.351:19.113         EV8         Matrings						SOFT_RST_PLLA
VDD01         1.80V         I           VDD02         1.80V         I           VDD03         1.80V         I           VDD04         1.80V         I           VDD05         1.80V         I           VDD05         1.80V         I           VDD06         1.80V         I           VDD07         1.80V         I           VDD08         1.80V         I           VDD09         1.80V         I           VDD09         1.80V         I           VD009         1.80V         I           Itered         Auto Scrolt On         I           Itered         Auto Scrolt Scr	On 3.296 V	-1,722 mA	-5,676 mW	Read		SOFT_RST_PLLB
VDD02         1.80V         I           VDD03         1.80V         I           VDD04         1.80V         I           VDD05         1.80V         I           VDD06         1.80V         I           VDD07         1.80V         I           VDD08         1.80V         I           VDD09         1.80V         I           VDD09         1.80V         I           VDD09         1.80V         I           VDD09         1.80V         I           Itered         Auto Scrolt On         I           Sourco         Messinsini 1.8         IVB           Sastistini 1.8         IVB         Starting	Off 0.009 V	0 mA	0 mW	Read		
VDD03 1.80V  VDD04 1.80V  VDD05 1.80V  VDD05 1.80V  VDD05 1.80V  VDD06 1.80V  VDD07 1.80V  VDD09 1.80V  VDD09 1.80V  VDD09 1.80V  VDD09 1.80V  VD09 1.	Off 0 V	0 mA	0 mW	Read		Hard Reset, Sync, & F Down
VDD04 1.80V VDD05 1.80V VDD06 1.80V VDD07 1.80V VDD09 1.80V VDD09 1.80V VDD09 1.80V VDD09 1.80V VD09 1.80V 1.	Off 0 V	0 mA	0 mW	Read		HARD RST
VDD04 1.80V VDD05 1.80V VDD06 1.80V VDD07 1.80V VD007 1.80V VD009 1.80V 1.	Off 0 V	0 mA	0 mW	Read		-
VDDOS 1.80V  All Output  Supplies  VDDOS 1.80V  All Output  Supplies  VDDOS 1.80V  Sutch VDDOS 1.80V  VDDOS 1	Off 0 V	0 mA	0 mW	Read		SYNC
VDD06 1.80V 1 VDD07 1.80V 1 VDD08 1.80V 1 VDD09 1.80V 1 All Output Supplies Power On 1 tered Auto Scroll: On 1 mestamp Source Messag 353:10.113 KVB Starting 353:10.128 EVB Pausing		0 mA	0 mW			PDN: 0
VDD07 1.80V VDD08 1.80V VDD09 1.80V VDD09 1.80V VD09 All Output Supplies Power On C VD09 Auto Scroll: On C Messag SS19.113 EVB Pausing SS19.128 EVB Pausing Pausing SS19.128 EVB Pausing Pausi				Read		Frequency Adjus
VDO08 1.80V  VDO09 1.80V  All Output  VD09 1.80V  VD09	Off 0 V	0 mA	0 mW	Read		FINC
VDD09 1.80V All Output Select Voltage Power On tered Auto Scroll: On satisfield V8 Starting 33519.113 V8 Pausing 33519.128 U8 Pausing	Off 0 V	0 mA	0 mW	Read		FDEC
All Output Supplies Power On Auto Scroll: On Auto Scroll: On Auto Scroll: On Survey Message (35:19.113 V/B Message) (35:19.113 V/B Pousing)	Off 0 V	0 mA	0 mW	Read		FDEC
Supplies Power On tered Auto Scroli: On staramp Source Message s35:19.113 EV8 Starting s25:19.128 EV8 Pausing	Off 0 V	0 mA	0 mW	Read		
Supplies Power On Control Cont	🔽 Total	1,111 mA	-0.594 W	Read All		
ttered Auto Scroll: On mestamp Source Messag 1:35:19.113 EVB Starting 1:35:19.128 EVB Pausing		ompare Design Es	timator to Mon	uroments		
Itered         Auto Scroll: On           mestamp         Source         Messag           k35:19.113         EVB         Starting           k35:19.128         EVB         Pausing	Power Off Co	ompare Design Es	umates to meas	surements		
mestamp Source Messag 3:35:19.113 EVB Starting 3:35:19.128 EVB Pausing						
0:35:19.113 EVB Starting 0:35:19.128 EVB Pausing	Insert Marker	Clear Cop	y to Clipboard	Pause		
235:19.113 EVB Starting 235:19.128 EVB Pausing						
:35:19.128 EVB Pausing	Set_Voltage_Mux(settir	a=VDD 9 PIN)				
25-10 100 EVR Starting	70 msec for voltage M					
Starting	Read_ADC(num_sampl	es=10)				
:35:19.204 EVB Finished	d Read_ADC(num_samp	les=10) => 0.1				
35:19.204 EVB Finished	d Measure_Voltage(char	nnel=VDD_9_PIN)	=> 0			
:35:19.204 EVB Finished Power: 0		gulator_id=VDD_9	) => Voltage_R	eg: 0.000V, Voltage_Pin: 0.000V, Current: 0.000A	A,	

Figure 10.4. Application #2: EVBGUI

## Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5396C)
- Control the EVB's regulators
- Monitor voltage, current, and power on the EVB

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# 10.4 Common ClockBuilder Pro Workflow Scenarios

Three common workflow scenarios when using CBPro and the Si5396C/L EVB are:

- Workflow Scenario 1: Testing a Silicon Labs-Created Default Configuration
- Workflow Scenario 2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario 3: Testing a User-Created Device Configuration

Each workflow scenario is described in more detail in the following sections.

# 10.5 Workflow Scenario 1: Testing a Silicon Labs Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows:

Once the PC and EVB are connected, launch ClockBuilder Pro by clicking this icon on your PC's desktop:



Figure 10.5. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.

© ClockBuilder Pro Wizard       •<					
Work With a Design	Quick Links				
Create New Project	Silicon Labs Timing Solutions Knowledge Base Custom Part Number Lookup				
Convert Existing Project/NVM File	Applications Documentation 10/40/100G Line Card Whitepaper				
ex Open Sample Project	Clock Generators for Cloud Data Centers Optimizing Si534x Jitter Performance Selecting the Right Clocks for Timing Synchronization				
Evaluation Board Detected Si5396C Rev A EVB	Applications PCIe Gen 4.0 Jitter Requirements Selecting a PCIe Reference Clock Source Making Accurate Clock Jitter Measurements				
	ClockBuilder Pro Documentation				
	CBPro Tools & Support for In-System Programming CLI User's Guide Release Notes - Knowledge Base				
o.	Version 3.0 Built on 11/15/2020				

Figure 10.6. Open Default Plan

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When you open the default plan (based on your EVB model number), a pop-up will appear:

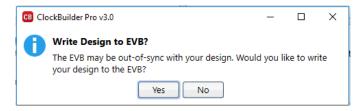


Figure 10.7. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5396C/L device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

🛯 Si5396 Design Write	_	×
Writing Si5396 Design to EVB		
Address 0x0128		

Figure 10.8. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below:

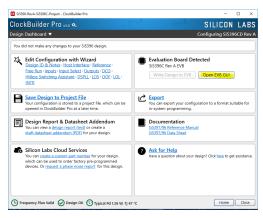


Figure 10.9. Open EVB GUI

The EVB GUI will appear. Note that all power supplies will be set to the values defined in the device's default CBPro project file created by Silicon Labs, as shown in the following figure:

CB Si5396C Re	v A EVB - Cloc	kBuilder Pro								– 🗆 🗙
File Help										
Info DUT S	PI DUT Sett	ings Editor	DUT Register Editor	Regulators	All Voltages	GPIO	Status Registers		~	Control Registers
			Voltage	Currer	nt Power				Î	Soft Reset and Calibration
	VDD 1.80V	Or	1.788 V	2,383	mA 4,261 i	nW [	Read			
v	DDA 3.30V	Or	3.296 V	-2,337	mA -7,703 i	mW [	Read			SOFT_RST_PLLA
VD	DO0 2.50V		2.490 V	31	mA 77 i	mW [	Read			SOFT_RST_PLLB
VD	DO1 2.50V		2.508 V	16	mA 40 i	nW [	Read			Hard Reset, Sync, & Power
VD	DO2 2.50V		2.497 V	16	mA 40 i	nW [	Read			Down
VD	DO3 2.50V	Or	2.498 V	16	mA 40 i	nW [	Read			HARD_RST
VD	DO4 2.50V	Or	2.504 V	16	mA 40 i	mW [	Read			SYNC
VD	DO5 2.50V		2.497 V	16	mA 40 i	nW [	Read			PDN: 0
VD	DO6 2.50V		2.501 V	15	mA 38 i	nw [	Read			Frequency Adjust
VD	DO7 2.50V			16	mA 40 i	nw [	Read			FINC
	DO8 2.50V			16			Read			FDEC
		_								
VD	DO9 2.50V	🔽 🔽	2.509 V	31 (	mA 78 i	nW [	Read			
All Output	Select	t Voltage	Total	235	mA -2.969	w	Read All		U	
Supplies	D Powe	r On Pow	rer Off Co	ompare Desig	in Estimates to	Measu	rements		-	
Log										
Filtered 🗧	Auto Scro	ll: On 📱 🛛	Insert Marker	Clear	Copy to Clipb	bard	Pause			
Timestamp	Source	Message								
09:43:25.245	EVB	Starting Set	_Voltage_Mux(settin	g=VDD_9_PI	N)					
09:43:25.259	EVB		msec for voltage Ml							
09:43:25.331	EVB	Starting Rea	id_ADC(num_sample	es=10)						
09:43:25.335	EVB	Finished Rea	ad_ADC(num_sampl	es=10) => 72	27.1					
09:43:25.335	EVB	Finished Me	asure_Voltage(chan	nel=VDD_9_I	PIN) => 3.44					
09:43:25.335	EVB	Finished Me 0.078W	asure_Regulator(reg	gulator_id=VI	DD_9) => Volta	ige_Reg	g: 2.509V, Voltage_	Pin: 3.440V, Current: 0.031A, Power:	:	
EVB Firmware 1	.6   Device: Si5	396CD   DUT I	Mode: SPI 4-Wire; FW	Low-Level Co	mmands				C	ClockBuilder Pro v3.0 [2020-11-15

Figure 10.10. EVB GUI Window

#### 10.5.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the highlighted "Read All" button and then reviewing the voltage, current, and power readings for each VDDx supply.

**Note:** Switching the VDD and VDDA supplies "Off" and then "On" will power-down and reset the DUT. Each time this is done, you must go back to the Wizard's main menu and select "Write Design to EVB" to reload the Silicon Labs default plan into the DUT's register space, as shown below.

(	B Si5396-RevA-Si5396C-Project - ClockBuilder Pro	- 🗆 X
(	ClockBuilder Pro v3.0 🎭	SILICON LABS
C	Design Dashboard 🔻	Configuring Si5396CD Rev A
	You did not make any changes to your Si5396 design.	
	Edit Configuration with Wizard         Design ID & Notes · Host Interface · Reference ·         Free Run · Inputs · Input Select · Outputs · DCO ·         Hitless Switching Assistant · DSPLL · LOS · OOF · LOL ·         INTR	Evaluation Board Detected Si5396C Rev A EVB Write Design to EVB Open EVB GUI

Figure 10.11. Write Design to EVB

Failure to perform this step will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify that the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

Si5396-RevA-Si5396C-Project - ClockBuilder Pro	– 🗆 X
ClockBuilder Pro v3.0 🎭	SILICON LABS
Design Dashboard 🔻	Configuring Si5396CD Rev A
You did not make any changes to your Si5396 design.	
Edit Configuration with Wizard Design ID & Notes · Host Interface · Reference · Free Run · Inputs · Input Select · Outputs · DCO · Hitless Switching Assistant · DSPLL · LOS · OOF · LOL · INTR	Evaluation Board Detected Si5396C Rev A EVB Write Design to EVB Open EVB GUI
Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a design report (text) or create a draft datasheet addendum (PDF) for your design.	Documentation Si5397/96 Reference Manual Si5397/96 Data Sheet
Silicon Labs Cloud Services You can <u>create a custom part number</u> for your design, which can be used to order factory pre-programmed devices. Or <u>request a phase noise report</u> for this design.	Ask for Help Have a question about your design? Click here to get assistance.
Frequency Plan Valid 🕢 Design OK 🕚 Typical Pd 1.26 W, Tj 47 °C	Home Close

Figure 10.12. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

esign Repo			
	rt		10.0
Design Ru			A
Errors: - No erro			
- No errol	PS		
Warnings:			
- No warn	ings		
NO Warn.	1153		
Device Gr			
	utput Frequency: 200 MHz		
	Synthesis Mode: Fractional		
	Plan Grade: D		
Minimum B			
Device	Output Clock		
Grade	Frequency Range Typical Jitter		
Si5396C	100 Hz to 720 MHz < 150 fs		
5i5396D*	100 Hz to 350 MHz "		
Record ou	n your calculated frequency plan, a Si5396D grade device is		
	t for your design. For more in-system configuration flexibility		
	requencies), consider selecting device grade Si5396C when		
	g an ordering part number (OPN) for your application. See the		
	Ordering Guide for more information.		
adedsheee	oracing datac for more informacion		
Design			
======			
Host Inter	rface:		
T (0 D			
1/0 PO	wer Supply: VDD (Core)		
SPI Mo	de: 4-Wire		
SPI Mo			
SPI Mo I2C Ad	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins)		
SPI Mo I2C Ad External I	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference:		
SPI Mo I2C Ad	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins)		
SPI Mon I2C Adr External I 48 MHz	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference:		
SPI Mov I2C Add External I 48 MHz Inputs:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal)		
SPI Mo I2C Ad External I 48 MHz Inputs: IN0: 5	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz		
SPI Mo I2C Ad External 48 MHz Inputs: IN0:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal)		
SPI Mon I2C Add External 1 48 MHz Inputs: IN0:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended		
SPI Mon I2C Add 48 MHz Inputs: IN0: IN1: IN1: IN1:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended DSPLL A,B JMused JMused		
SPI Mon I2C Add 48 MHz Inputs: IN0: IN1: IN1: IN1:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended DSPLL A,B Junsed		
SPI Mod I2C Add 48 MHz Inputs: IN0: IN1: IN1: IN1: IN2: IN3:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended DSPLL A,B JMused JMused		
SPI Mod I2C Add External 48 MHz Inputs: IN0: IN1: IN1: IN1: IN2: IN3: Outputs:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended SSPLL A,B Jnused Jnused Jnused		
SPI Mod I2C Add External 1 48 MHz Inputs: IN0: IN0: IN1: IN2: IN3: Outputs: OUT0A:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz 25 MHz Standard Differential and Single-ended JSPLL A,B Jnused Jnused Jnused 156.25 MHz		
SPI Mon I2C Add External 1 48 MHz Inputs: IN0: IN1: IN2: IN1: IN2: IN3: Outputs: OUTØA:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended DSPLL A,B JMUSEd JMUSEd JMUSEd 156.25 MHz Enabled, LVDS 2.5 V		
SPI Mod I2C Ad External 1 48 MHz Inputs: IN0: IN1: IN2: IN3: OUT0A:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended JSPLL A,B Jnused Jnused 156.25 MHz Enabled, LVDS 2.5 V SPLL A		
SPI Mod I2C Ad External 48 MHz Inputs: IN0: IN1: IN1: IN1: IN2: OUT9A: OUT9A:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz 25 MHz SSPLL A,B JMUSEd JMUSEd JMUSEd 156.25 MHz Enabled, LVDS 2.5 V SSPLL A 156.25 MHz		
SPI Mod I2C Ad External 48 MHz Inputs: IN0: IN1: IN1: IN3: UN1: IN3: Outputs: OUTØA:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 225 MHz Standard Differential and Single-ended JSPLL A,B Juused Juused Juused Juused Juused 156.25 MHz Enabled, LVDS 2.5 V JSPLL A JS6.25 MHz Enabled, LVDS 2.5 V		
SPI Mo I2C Ad External 1 48 MHz Inputs: IN0: IN1: IN1: IN2: IN3: IN3: IN3: IN3: IN3: IN3: IN3: IN3	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended DSPLL A,B Jmused Jmused 156.25 MHz Enabled, LVDS 2.5 V DSPLL A 156.25 MHz Enabled, LVDS 2.5 V DSPL		
SPI Mo I2C Ad External 1 48 MHz Inputs: INU: IN1: IN2: IN3: OUT04: OUT04: OUT04:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended DSPLL A,B Jmused Jmused 156.25 MHz Enabled, LVDS 2.5 V DSPLL A 156.25 MHz Enabled, LVDS 2.5 V DSPL		
SPI Mo. I2C Ad External 1 48 MHz Inputs: IN1: IN1: IN2: IN3: OUT04: OUT04: OUT04: OUT01: OUT1:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended 35PLL A,B Juused Juused 156.25 MHz Enabled, LVDS 2.5 V 35PLL A 156.25 MHz Enabled, LVDS 2.5 V 35PLL A Junsed 100 MHz Enabled, LVDS 2.5 V		
SPI Mo. I2C Ad External 1 48 MHz Inputs: IN0: IN1: IN2: IN3: OUTputs: OUTputs: OUTputs: OUTPuts: OUTO:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended JSPLL A,B Jnused Jnused Jnused Jnused Jnused 156.25 MHz Enabled, LVDS 2.5 V JSPLL A Jnused LOS 2.5 V JSPLL A Jnused LOS 2.5 V JSPLL A Jnused LOS 2.5 V JSPLL A		
SPI Mo. I2C Ad External 48 MHz Inputs: IN0: IN1: IN2: IN3: Uutputs: OUT0A: OUT0A: OUT04: OUT04: OUT1: OUT2: OUT3:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz 25 MHz Standard Differential and Single-ended DSPLL A,B JMused JMused JMused 156.25 MHz Enabled, LVDS 2.5 V DSPLL A 156.25 MHz Enabled, LVDS 2.5 V DSPLL A Inabled, LVDS 2.5 V DSPLL A Inabled, LVDS 2.5 V DSPLL A JMUSEd		
SPI Mo. I2C Ad. 48 MHz 48 MHz Inputs: IN1: IN2: IN3: OUT04: OUT04: OUT04: OUT05: OUT04:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 225 MHz Standard Differential and Single-ended JSPLL A,B Junused Junused 156.25 MHz Enabled, LVDS 2.5 V JSPLL A L56.25 MHz Enabled, LVDS 2.5 V JSPLL A L50 JUNS A L50 JU		
SPI Mo. I2C Ad External 48 MHz Inputs: IN0: IN1: IN2: IN3: Outputs: OUT04: OUT04: OUT04: OUT04: OUT1: OUT2: OUT3:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended DSPLL A,B Jmused Jmused Jmused 156.25 MHz Enabled, LVDS 2.5 V DSPLL A 156.25 MHz Enabled, LVDS 2.5 V DSPLL A 100 MHz Enabled, LVDS 2.5 V DSPLL B 200 MHz Enabled, LVDS 2.5 V DSPLL B 200 MHz Enabled, LVDS 2.5 V		
SPI Mo. I2C Add External 48 MHz Inputs: IN0: IN1: IN2: IN2: IN3: OUT04: OUT04: OUT04: OUT04: OUT1: OUT2: OUT3:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz Standard Differential and Single-ended JSPLL A,B Junused Junused Junused Junused Junused JS6.25 MHz Enabled, LVDS 2.5 V JSPLL A Junused J00 MHz Enabled, LVDS 2.5 V JSPLL A Junused J00 MHz Enabled, LVDS 2.5 V JSPLL B J00 HHz Enabled, LVDS 2.5 V		
SPI Mo. I2C Add External 48 MHz Inputs: IN0: IN1: IN2: IN1: IN2: IN3: OUT04: OUT04: OUT05: OUT04: OUT2: OUT3:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 25 MHz 25 MHz 25 MHz 55 MHz Grabled, LVDS 2.5 V 35 PLL A 156.25 MHz Grabled, LVDS 2.5 V 35 PLL A Jmused 100 MHz Grabled, LVDS 2.5 V 35 PLL A 100 MHz Brabled, LVDS 2.5 V 35 PLL A 100 MHz Brabled, LVDS 2.5 V 35 PLL A 100 SPLL A		
SPI Mo. I2C Ad External 48 MHz Inputs: IN0: IN1: IN2: IN2: IN2: IN2: OUT04: OUT04: OUT04: OUT05: OUT3:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 225 MHz Standard Differential and Single-ended DSPLL A,B Juused Juused Juused 156.25 MHz Enabled, LVDS 2.5 V DSPLL A Jused 100 MHz Enabled, LVDS 2.5 V DSPLL A Jused 100 MHz Enabled, LVDS 2.5 V DSPLL B Z00 MHz Enabled, LVDS 2.5 V DSPLL B Jused Jused Jused Jused		
SPI Mo. I2C Add External 48 MHz Inputs: IN0: IN1: IN2: IN1: IN2: IN3: OUT04: OUT04: OUT05: OUT04: OUT2: OUT3:	de: 4-Wire dress Range: 108d to 111d / 0x6C to 0x6F (selected via A0/A1 pins) Reference: (XTAL - Crystal) 225 MHz Standard Differential and Single-ended DSPLL A,B Juused Juused Juused 156.25 MHz Enabled, LVDS 2.5 V DSPLL A Jused 100 MHz Enabled, LVDS 2.5 V DSPLL A Jused 100 MHz Enabled, LVDS 2.5 V DSPLL B Z00 MHz Enabled, LVDS 2.5 V DSPLL B Jused Jused Jused Jused		*

Figure 10.13. Design Report Window

#### 10.5.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will run in "locked" mode.

#### 10.6 Workflow Scenario 2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on the links below under "Edit Configuration with Wizard".

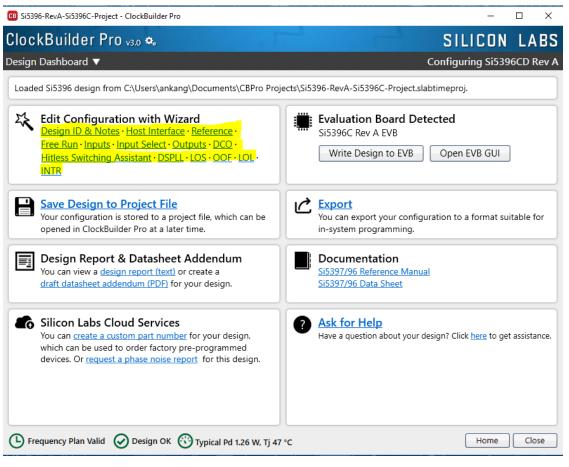


Figure 10.14. Edit Configuration with Wizard

You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

Si5396-RevA-Si53	96C-Project - ClockBuilder Pro	-		2
lockBuild	er Pro v3.0 🐝	SILICON	LA	A B
ep 1 of 14 - De	esign ID & Notes 🔻	Configuring Si53	96CD I	Re۱
<b>Design ID</b> The device has 8 r	egisters, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuratic	on/revision identifier.		
Design ID:	Si5396C (optional; max 8 characters)			
	The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESI	GN_ID7.		
adding Mode:	NULL Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character).	padded with 0x00 bytes (ak	a NULL	
5	Space Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character).			
nter anything yo	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be			m
nter anything yo	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character). u want here. The text is stored in your project file and included in design reports and custo			ım
nter anything yo	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character). u want here. The text is stored in your project file and included in design reports and custo			Im
nter anything yo	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character). u want here. The text is stored in your project file and included in design reports and custo			Im
nter anything yo	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character). u want here. The text is stored in your project file and included in design reports and custo			ım
nter anything yo	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character). u want here. The text is stored in your project file and included in design reports and custo			Im
nter anything yo	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character). u want here. The text is stored in your project file and included in design reports and custo			Im
	If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be character). u want here. The text is stored in your project file and included in design reports and custo			ım

Figure 10.15. Design Wizard

Note that you can click on the icon in the lower left corner of the menu to confirm that your frequency plan is valid. After making your desired changes, click on Write to EVB to update the DUT and reconfigure your device real-time. The Design Write status window will appear each time you make a change.

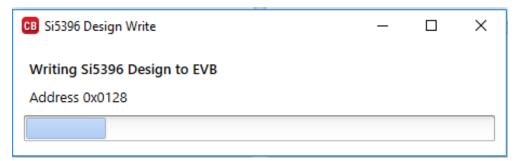


Figure 10.16. Writing Design Status

#### 10.7 Workflow Scenario 3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking the icon on your desktop and selecting "Open Project".



Figure 10.17. Open Design Project File

Locate your CBPro design file (\*.slabtimeproj or \*.sitproj file) in the Windows file browser.

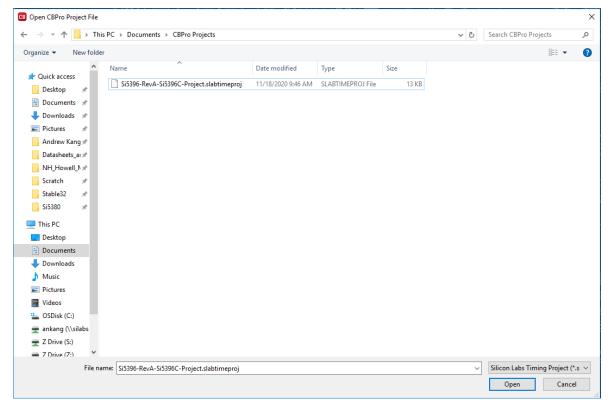


Figure 10.18. Browse to Project File

Select "Yes" when the "Write Design to EVB" popup appears:

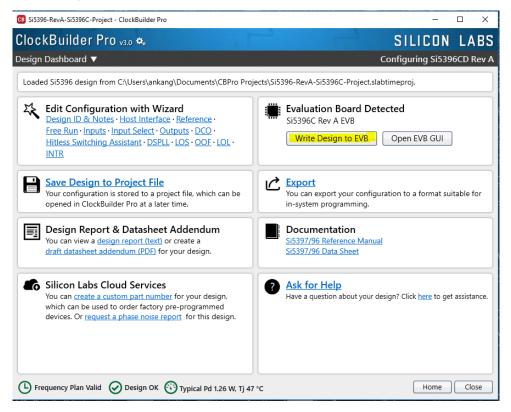


Figure 10.19. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

#### 10.8 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:

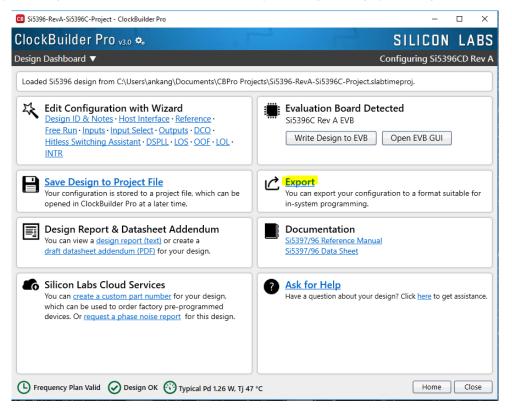


Figure 10.20. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming:

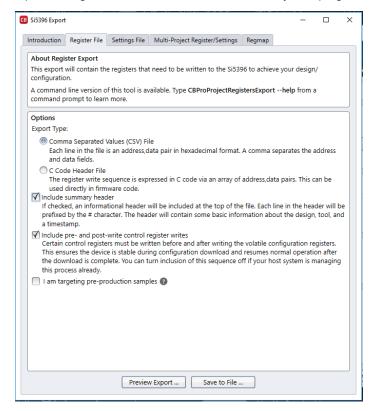


Figure 10.21. Export Settings

UG467: Si5396C/L Evaluation Board User's Guide • Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

# 11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

**Note:** Writing to the device non-volatile memory (OTP) is **NOT** the same as writing a configuration into the Si5396C/L using ClockBuilder Pro on the Si5396C/L EVB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5396C/L RAM space and can be done virtually an unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si5397/96 Family Reference Manual and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the desired configuration is valid when choosing to write to OTP.

UG467: Si5396C/L Evaluation Board User's Guide • Serial Device Communications

# 12. Serial Device Communications

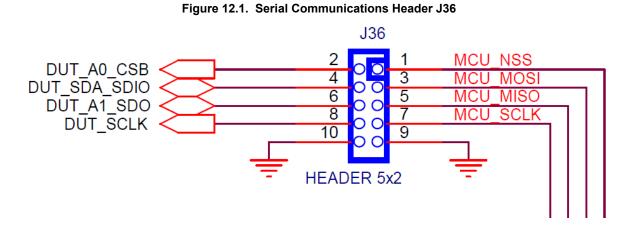
#### 12.1 Onboard SPI Support

The MCU onboard the Si5396C/L EVB communicates with the Si5396C/L device through a 4-wire Serial Peripheral Interface (SPI) link. The MCU is the SPI master and the Si5396C/L device is the SPI slave. The Si5396C/L device can also support a 2-wire I<sup>2</sup>C serial interface, although the Si5396C/L EVB does NOT support the I<sup>2</sup>C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I<sup>2</sup>C.

#### 12.2 External I<sup>2</sup>C Support

I<sup>2</sup>C can be supported if driven from an external I<sup>2</sup>C controller. The serial interface signals between the MCU and Si5396C/L pass through shunts loaded on header J36. These jumper shunts must be installed in J36 for normal EVB operation using SPI with CBPro. If testing of I<sup>2</sup>C operation via external controller is desired, the shunts in J36 can be removed thereby isolating the onboard MCU from the Si5396C/L device. The shunt at J4 (I2C\_SEL) must also be removed to select I<sup>2</sup>C as Si5396C/L interface type. An external I<sup>2</sup>C controller connected to the Si5396 side of J36 can then communicate to the Si5396C/L device. For more information on I<sup>2</sup>C signal protocol, refer to the Si5396 data sheet.

The figure below illustrates the J36 header schematic. J36 even numbered pins (2, 4, 6, etc.) connect to the Si5396C/L device, and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. When the jumper shunts have been removed from J36 and J4,  $I^2C$  operation should use J36 pin 4 (DUT\_SDA\_SDIO) as the I2CSDA and J36 pin 8 (DUT\_SCLK) as the I2CSCLK. Note that the external  $I^2C$  controller will need to supply its own  $I^2C$  signal pull-up resistors.



UG467: Si5396C/L Evaluation Board User's Guide • Si5396C/L EVB Schematic, Layout, and Bill of Materials (BOM)

# 13. Si5396C/L EVB Schematic, Layout, and Bill of Materials (BOM)

The Si5396C/L EVB Schematic, Layout, and Bill of Materials (BOM) can be found online at:

www.silabs.com/documents/public/schematic-files/si539x-design-files.zip

Note: Please be aware that the Si5396C/L EVB schematic is in OrCad Capture *hierarchical format* and not in a typical "flat" schematic format.

This document supports the evaluation board silkscreened Si5396C/L EVB for the following configurations as described in the table below. The data sheet documents the different Si5396C/L grades.

### Table 13.1. Evaluation Board Configurations<sup>1</sup>

Config #	Eval Board Label	Si5396 Grade Revision		Notes
1	Si5396C-A-EB	С	А	Crystal and related components installed.
2	Si5396L-A-EB	L	А	Crystal and related components not installed. Only the DUT and label differ versus Si5396C-A-EB.

#### Note:

1. Note that it is not possible to load an Si5396C project onto an Si5396L-A-EB or vice-versa. Use Si5396C/D plans for Si5396C-A-EB and Si5396L/M plans for Si5396L-A-EB.