Si838x Data Sheet

Bipolar Digital Field Inputs for PLCs and Industrial I/O Modules

The Si838x provides eight input channels ideal for 24 V digital logic commonly used for industrial applications. These channels can either sink or source current and feature integrated safety rated isolation. In combination with a few external components, this provides compliance to IEC 61131-2 switch types 1, 2, or 3. The input interface is based on Skyworks' ground-breaking CMOS based LED emulator technology which enables the bipolar capability (sinking or sourcing inputs) with no VDD required on the field side. The output interface from the Si838x device allows for low power operation with 2.25 V compliance. These products utilize Skyworks' proprietary CMOS-based isolation technology, supporting up to 2.5 kV_{RMS} withstand voltage. This technology enables high CMTI (up to 300 kV/µs), lower propagation delays and channel skew, reduced variation with temperature and age, and tighter part-to-part matching. The Si838x offers longer service life and dramatically higher reliability compared to opto-coupled input solutions.

Product options include parallel or serialized outputs. Parallel outputs can be purchased with built-in, low-pass filters for improved noise immunity, reduced design complexity and cost. Cascading a total of 128 channels (16x Si838x) with a single MCU interface is possible with the Si8380S serial output option. The Si8380S also unlocks the ability to configure each channel with unique filtering behavior.

Applications:

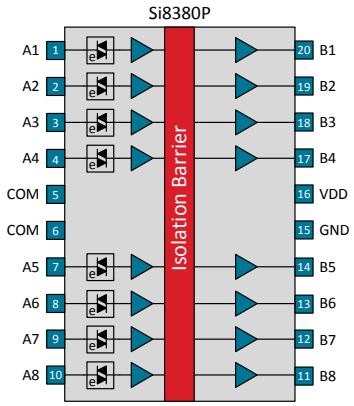
- Programmable logic controllers
- Industrial data acquisition
- Distributed control systems
- CNC machines
- I/O modules
- Motion control systems

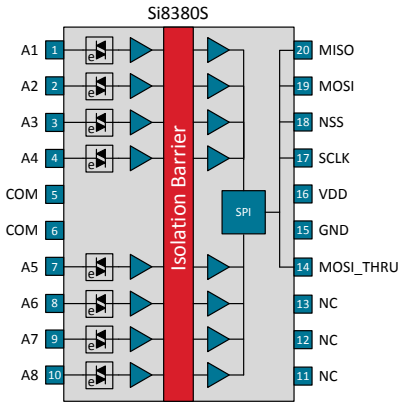
Safety Regulatory Approvals:

- UL 1577 recognized
  - Up to 2500 V_{RMS} for one minute
- CSA component notice 5A approval
  - IEC 60950-1
  - IEC 62368-1
- VDE certification conformity
  - VDE 0884-10
- CQC certification approval
  - GB4943.1

KEY FEATURES

- Bipolar digital interface with 24 V sinking or sourcing inputs
- Eight total inputs in one package
- High data rates of up to 2 Mbps
- Safety rated integrated isolation of 2.5 kV_{RMS}
- Low input current of 1 mA typ
- No VDD required on field side
- High electromagnetic immunity
- Selectable debounce filter times of up to 100 ms
- Configurable debounce filter modes available with SPI interface option
- Transient immunity up to 300 kV/µs
- Flow-through output configuration with eight outputs
- Option for SPI interface with daisy-chain capability
- Wide 2.25 to 5.5 V VDD operation
- Wide operating temperature range
  - –40 to +125 °C
- Compliant to IEC 61131-2
  - Type 1, 2, 3
- RoHS-compliant packages
  - QSOP-20





1. Ordering Guide

Table 1.1. Si838x Ordering Guide

Ordering Part Number	Output Interface	Number of High-Speed Channels	Low-Pass Debounce Filter Delay[1, 2]	Package Type[3]	Isolation Rating
Si8380S-IU	Serial	0	0 ms	20-QSOP	2.5 kV_{RMS}
Si8380P-IU	Parallel	0	0 ms	20-QSOP	2.5 kV_{RMS}
Si8382P-IU	Parallel	2	0 ms	20-QSOP	2.5 kV_{RMS}
Si8384P-IU	Parallel	4	0 ms	20-QSOP	2.5 kV_{RMS}
Si8388P-IU	Parallel	8	0 ms	20-QSOP	2.5 kV_{RMS}
Si8380PF-IU	Parallel	0	10 ms	20-QSOP	2.5 kV_{RMS}
Si8382PF-IU	Parallel	2	10 ms	20-QSOP	2.5 kV_{RMS}
Si8384PF-IU	Parallel	4	10 ms	20-QSOP	2.5 kV_{RMS}
Si8380PM-IU	Parallel	0	30 ms	20-QSOP	2.5 kV_{RMS}
Si8382PM-IU	Parallel	2	30 ms	20-QSOP	2.5 kV_{RMS}
Si8384PM-IU	Parallel	4	30 ms	20-QSOP	2.5 kV_{RMS}
Si8380PS-IU	Parallel	0	100 ms	20-QSOP	2.5 kV_{RMS}
Si8382PS-IU	Parallel	2	100 ms	20-QSOP	2.5 kV_{RMS}
Si8384PS-IU	Parallel	4	100 ms	20-QSOP	2.5 kV_{RMS}

Note:

1. Low-pass debounce filter delay applies to low-speed channels only.
2. All low-speed channels have a built-in 4 µs low-pass debounce filter delay, in addition to the low-pass filter delay listed in this table. See 3.6 Debounce Filter for details of the low-pass debounce filter operation.
3. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
4. Additional filter and channel configurations available upon request. Contact Skyworks for more information.
5. “Si” and “SI” are used interchangeably.
6. An "R" at the end of the Ordering Part Number indicates tape and reel option.

Table of Contents

2. System Overview

2.1 Theory of Operation

The operation of an Si838x channel is analogous to that of a bipolar opto-coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si838x channel is shown in the figure below.

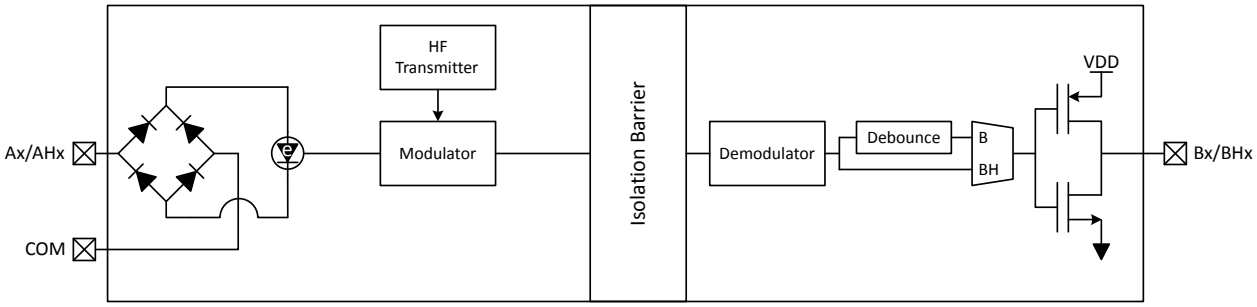


Figure 2.1. Simplified Channel Diagram

This product enables 24 V bipolar digital inputs to be connected to its input through a resistor network which acts as a voltage divider. Other digital voltage levels and characteristics can be implemented with simple modifications to the resistor network. See 4.2 IEC 61131-2 Compliance Options for resistor network recommendations. The inputs can be sourcing or sinking type. To enable this functionality, there is a diode bridge and an LED emulator at the front end of each input channel that drives an OOK (On-Off Key) modulator/demodulator across the capacitive isolation barrier. See 3.3 Bipolar LED Emulator Input for details on the input channel.

On the output side, the signal is either passed directly to the output stage in the case of a high-speed channel (BHx), or the signal is routed through a debounce filter block in the case of a low-speed channel (Bx). Thus, the high-speed channel offers the highest performance with the least propagation delay, but also the worst noise immunity. With the addition of the debounce filter block on the low-speed channel, precise noise control can be achieved.

The debounce block is configured by selecting the debounce filter mode applied and the amount of debounce filter delay time desired. There are three debounce filter modes available: deglitch filter mode, low-pass filter mode, and blanking filter mode. There are four debounce filter delay time options available: no delay, or delays of 10, 30, or 100 milliseconds. Additionally, a built-in low-pass filter delay of 4 µs is always present in low-speed channels, regardless of user configuration options. The desired filter delay time for parallel output devices can be selected by part number in 1. Ordering Guide. This filter delay time selection applies to all low-speed channels present on the device. The only filter mode available for parallel output interface devices is the low-pass filter mode.

In addition to the parallel output interface options available on the Si838x, there is also a serial output interface option. The Si8380S offers a four wire SPI interface with an additional MOSI_THRU output to facilitate the cascading of up to 16 Si8380S devices. Using the SPI interface detailed in section 3.5 Serial Peripheral Interface, the debounce filter type and filter delay time can each be controlled on a per channel basis. The debounce filter modes are explained in detail in 3.6 Debounce Filter.

3. Device Operation

Table 3.1. Truth Table Summary

VDD	Input, Ax/AHx	Output, Bx/BHx
P[1]	ON	HIGH
P	OFF	LOW
UP[2]	X	Undetermined[3]

1. P = powered (> UVLO).
2. UP = Unpowered (< UVLO).
3. An undetermined state can be any value within the absolute maximum rating of the output channel. See Table 5.10 Absolute Maximum Ratings[1] on page 23 for details.

3.1 Device Behavior

During any period in which VDD is below the UVLO threshold, such as device start-up, the output Bx/BHx is in an undetermined state until VDD is brought above the UVLO threshold for a time period of approximately t_{START}, after which Bx/BHx is immediately pulled low. Following this, the output is high when the current flowing from anode to cathode in the LED emulator is > $I_{F(ON)}$. Note that there is a propagation delay time (t_P) between a valid change on the input and a valid change on the output. Also note that there is a similar rise (t_R) and fall (t_F) time that should be accounted for in any valid change of the output. Finally, for low-speed channels, there is an additional filter delay time added to the propagation delay time. See Table 5.2 Electrical Characteristics on page 16 for detailed propagation delay specifications for all channel configurations, as well as specifications for all other timing parameters defined here.

Device startup, normal operation, and shutdown behavior are shown in the figure below.

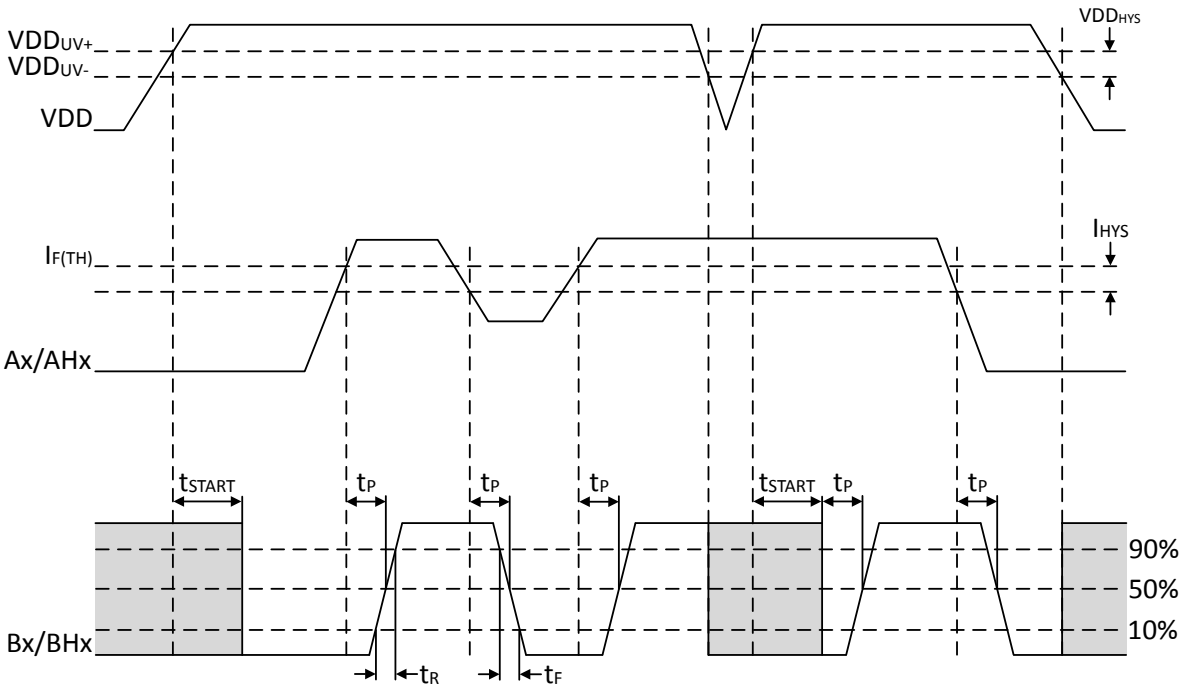


Figure 3.1. Si838x Timing Diagram

3.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating range. During UVLO, the outputs from the device do not track the inputs to the device. For example, the device unconditionally enters UVLO when VDD falls below VDD_{UV-} and exits UVLO when VDD rises above VDD_{UV+}. During UVLO, the outputs are in an undetermined state and should be controlled using external components like a pull-up or pull-down resistor. See section 3.4.2 Output Pin Termination and State Control for circuit recommendations

3.3 Bipolar LED Emulator Input

Each input channel on the Si838x can be modeled as a full bridge rectifier attached to an LED. A simplified equivalent circuit is depicted in Figure 3.2. Note that the model changes based on the whether the channel is sourcing or sinking current.

The input current to the LED emulator is used to power the isolation channel transmitter and send the input signal across the isolation barrier. This eliminates the need for a power supply on the input side of the device. See section 2.1 Theory of Operation for a complete overview of the signal path through the device.

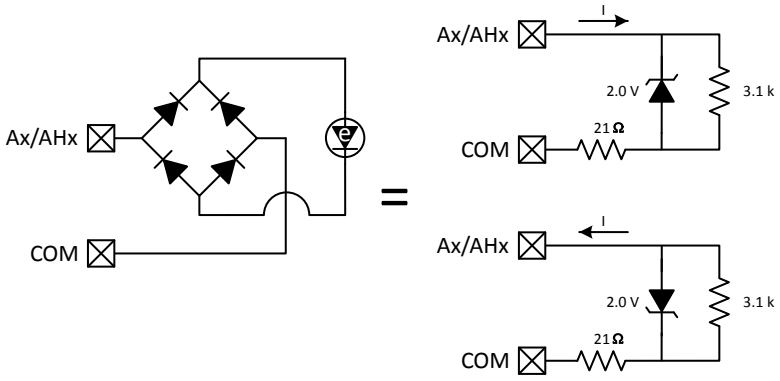


Figure 3.2. Bipolar LED Emulator Model

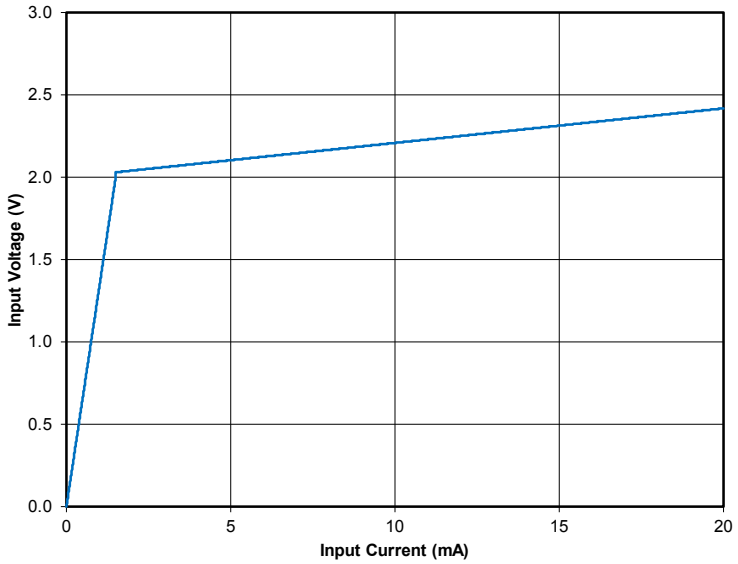


Figure 3.3. Bipolar LED Emulator Model I-V Curve

3.4 Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as the Si838x, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 5.5 Insulation and Safety-Related Specifications[1] on page 20 and Table 5.7 VDE 0884-10 Insulation Characteristics[1] on page 21 detail the creepage/clearance and working voltage capabilities of the Si838x. These tables also detail the component standards (UL1577, VDE 0884, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specification requirements. Refer to the end-system specification (60950-1, etc.) requirements before starting any design that uses the Si838x.

3.4.1 Supply Bypass

The Si838x device requires a 0.1 µF bypass capacitor between VDD and GND. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the outputs if the system is excessively noisy.

3.4.2 Output Pin Termination and State Control

The nominal output impedance of an Si838x output channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

To control for undetermined states on the output channel during UVLO, it is recommended to use a weak 100 kΩ pull-up or pull-down resistor to enforce either a high or low output state. For more information on output states and their conditions refer to Table 3.1 Truth Table Summary on page 5 and 3. Device Operation.

3.5 Serial Peripheral Interface

The Si8380S includes a Serial Peripheral Interface (SPI) that provides control and monitoring capability of the isolated channels using a commonly available microcontroller protocol. The direct-mapped registers allow an external master SPI controller to monitor the status of the eight input channels, as well as to control the filtering mode and delay of each channel. Additionally, support is provided to easily daisy-chain up to sixteen Si8380S devices. Each of these daisy-chained devices may be uniquely addressed by one master SPI controller.

3.5.1 SPI Register Map

The addressable SPI registers include one eight-bit register to reflect the status of each of the eight channels, which is read-only. Also, four additional registers provide two bits to specify the debounce filter delay, and two bits to specify the debounce filter mode for each of the eight channels. These user accessible SPI registers are illustrated in the following table.

Table 3.2. Si8380S SPI Register Map

Name	Address	Access	Description
CHAN_STATUS	0x0	Read	Current value of each of the eight input channels {STATUS[7:0]}
DBNC_MODE0	0x1	Read/Write	Mode control bits for the first four channel debounce filters organized as: {md_ch3[1:0],md_ch2[1:0],md_ch1[1:0],md_ch0[1:0]}
DBNC_MODE1	0x2	Read/Write	Mode control bits for the second four channel debounce filters organized as: {md_ch7[1:0],md_ch6[1:0],md_ch5[1:0],md_ch4[1:0]}
DBNC_DLY0	0x3	Read/Write	Delay control bits for the first four channel debounce filters organized as: {dly_ch3[1:0],dly_ch2[1:0],dly_ch1[1:0],dly_ch0[1:0]}
DBNC_DLY1	0x4	Read/Write	Delay control bits for the second four channel debounce filters organized as: {dly_ch7[1:0],dly_ch6[1:0],dly_ch5[1:0],dly_ch4[1:0]}

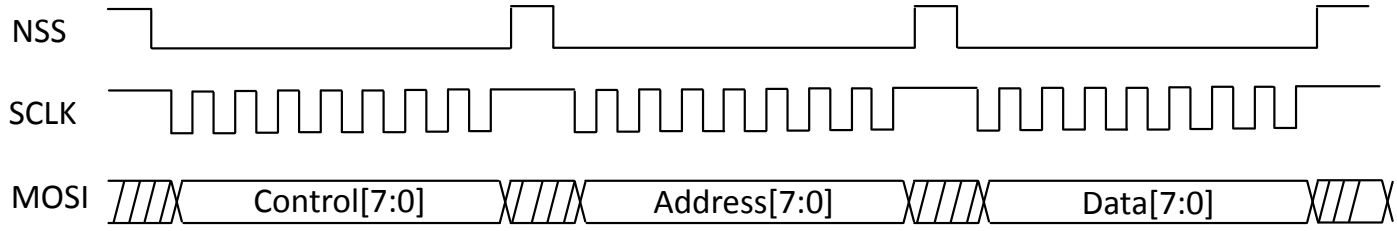
3.5.2 SPI Communication Transactions

SPI communication is performed using a four wire control interface. The four Si8380S device pins utilized for SPI include:

- SCLK (input) the SPI clock
- NSS (input) active low device select
- MOSI (input) master-out-slave-in
- MISO (output) master-in-slave-out

Additionally, a fifth wire MOSI_THRU (output) is provided as an Si8380S device pin to facilitate daisy chaining.

An Si8380S SPI communication packet is composed of three serial bytes. In this sequence, byte 0 is the control byte, and specifies the operation to be performed as well as the device to be selected in a daisy-chain organization. The CID[3:0] field should be set to all zeros by the SPI master in non daisy-chained operation. Next, byte 1 specifies the address of the internal Si8380S SPI register to be accessed. The final byte in the packet consists of either the data to be written to the addressed Si8380S SPI register (using MOSI), or the data read from the addressed Si8380S SPI register (using MISO). Details of the SPI communication packet are presented in the following figure for an Si8380S SPI write transaction.



Control Byte							
7	6	5	4	3	2	1	0
BRCT	R/Wb	0	0	CID[0]	CID[1]	CID[2]	CID[3]
Address Byte							
7	6	5	4	3	2	1	0
A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Data Byte							
7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

BRCT 1 - broadcast (write)
0 - only addressed part (write)
Ignored on reads

R/Wb 1 - read
0 - write

CTL[5:4] Reserved (set to 0,0)

CID[3:0] Daisy-chained part ID (0) is closest to the master MOSI. Accomplished by decrementing the CID as it passes through to the next Si8380S device in the daisy chain on MOSI_THRU

Figure 3.4. SPI Communication Packet Structure, Write Operation and Control Byte Structure

The SPI master will provide the timing of the signals and framing of the communication packets for all Si8380S SPI inputs: NSS, SCLK, and MOSI. Data is communicated from the SPI master to the Si8380S using the MOSI signal. The NSS and SCLK signals provide the necessary control and timing reference allowing the Si8380S to discern valid data on the MOSI signal. Data is returned to the SPI master by the Si8380S utilizing the MISO signal only during the final byte of a three byte SPI read communication packet. At all other times, the MISO signal is tri-stated by the Si8380S. Each of the eight bits for these three packets is captured by the Si8380S on eight adjacent rising edges of SCLK. Each frame of eight bits is composed within bounding periods where the device select, NSS, is deasserted. Upon the reception of the eight bits within a byte transaction, the deassertion of NSS advances the byte counter within the internal Si8380S SPI state machine. Should the transmission of an eight bit packet be corrupted, either with the deassertion of NSS before the eighth rising edge of SCLK, or with the absence of the deassertion of NSS after the eighth rising edge of SCLK, the internal SPI state machine may become unsynchronized with the master SPI controller.

To re-establish SPI synchronization with the Si8380S, the SPI master may, at any time, deassert the SPI device select signal NSS, and force a clock cycle on SCLK. When unsynchronized, the rising edge of SCLK when NSS is deasserted (high) re-initializes the internal SPI state machine. The Si8380S will then treat the immediately following eight bit SPI transaction after NSS is once again asserted as the first byte in a three byte SPI communication packet.

Any preceding communication packet will be abandoned by the Si8380S at the point synchronization is lost, and the NSS signal is deasserted. This could occur at any point in the three byte sequence of a SPI communication packet. One should note that abandoning a SPI write operation early, even during the last byte of the three byte SPI communication packet, will leave the destination register unchanged. However, if the number of SCLK cycles exceeds eight during the last byte of the three byte SPI write packet,

the destination Si8380S register may be corrupted. To remedy both of these situations, it is recommended that such a corrupted write operation be repeated immediately following resynchronization of the SPI interface.

3.5.3 SPI Read Operation

Referring to Figure 3.4 SPI Communication Packet Structure, Write Operation and Control Byte Structure on page 8, in an SPI read operation the control byte will only have bit 6 set to a 1 in a single Si8380S device organization (no daisy chaining). Bit 7 (the broadcast bit) is ignored during a read operation since only one device may be read at a time in either a single or daisy-chained organization.

The second byte in the three byte read packet is provided by the SPI master to designate the address of the Si8380S internal register to be queried. If the read address provided does not correspond to a physically available Si8380S internal register, all zeroes will be returned as the read value by the Si8380S.

The read data is provided during the final byte of the three byte read communication packet to the querying master SPI device utilizing the Si8380S's MISO output, which remains tri-stated at all other times.

The SPI read operation timing diagram is illustrated in the figure below.

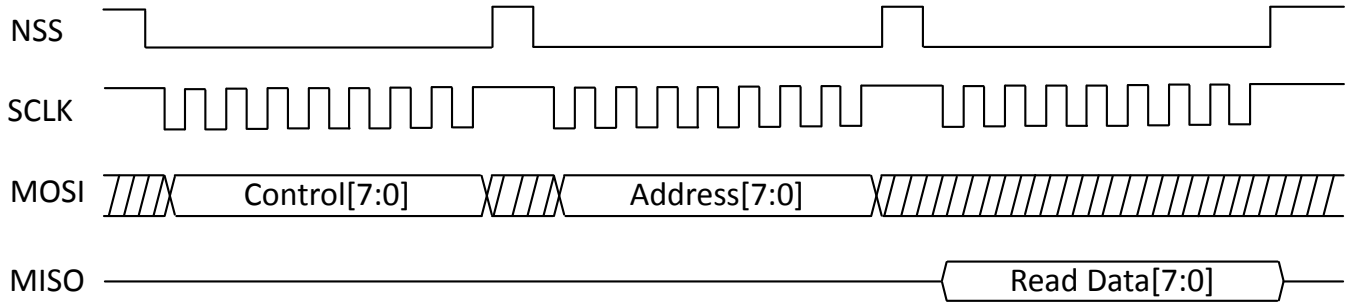


Figure 3.5. SPI Read Operation

3.5.4 SPI Write Operation

Again referring to Figure 3.4 SPI Communication Packet Structure, Write Operation and Control Byte Structure on page 8, in an SPI write operation the control byte may optionally have bit 7 (the broadcast bit) set to 1. During an SPI write operation, the broadcast bit forces all daisy-chained Si8380S devices to update the designated internal SPI register with the supplied write data, regardless of the Si8380S device being addressed using the CID[3:0] field of the control word.

The second byte in the three byte write packet is provided by the SPI master to designate the address of the Si8380S internal register to be updated. If the write address provided does not correspond to a physically available Si8380S internal register, no internal Si8380S SPI register update will occur.

The write data is provided by the SPI master during the final byte of the three byte write communication packet. The Si8380S MISO output remains tri-stated during the entire SPI write operation.

The SPI write operation timing diagram is illustrated in the figure below.

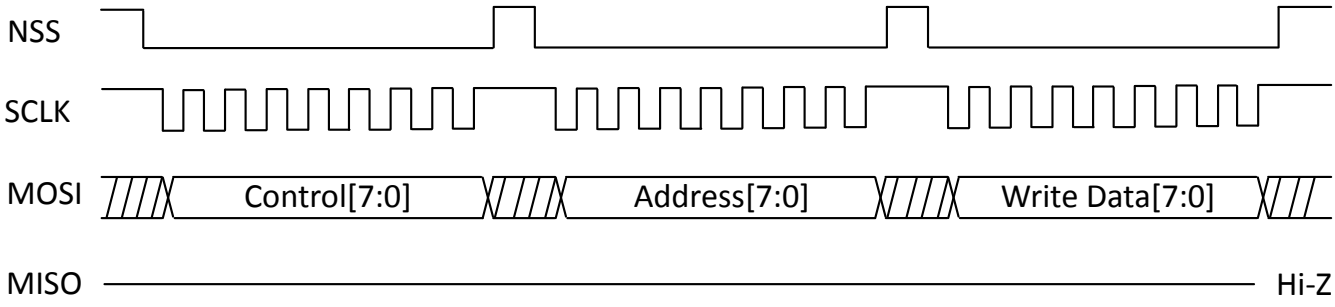


Figure 3.6. SPI Write Operation

3.5.5 SPI Daisy-Chain Organization

The Si8380S provides the capability to easily interconnect multiple Si8380S devices on a common SPI interface administered by a single SPI master requiring no additional control signals. To accomplish this, the Si8380S includes the additional SPI device output pin MOSI_THRU. Connecting together multiple Si8380S devices in this manner utilizes the MOSI_THRU pin of one Si8380S device to feed the MOSI pin of the next Si8380S device in the daisy chain. All bits composing an SPI communication packet from the SPI master are passed directly through by the Si8380S from the MOSI input to the MOSI_THRU output unchanged, except for the CID[3:0] field of the control byte.

The least significant four bits of the control byte in an SPI communication packet, CID[3:0], are dedicated to addressing one of up to sixteen Si8380S devices connected in a daisy chain, with 0000 indicating the device whose MOSI pin is fed directly by the SPI master, 0001 the following Si8380S device, etc. As this bit field is passed through the Si8380S, it is decremented by one. This four bit field is placed in the control word by the SPI master in reverse order, allowing the carry of the decrement to ripple into the next bit in the CID field as the bits of the control word proceed: CID[0] is placed at bit 3 and CID[3] placed at bit 0 of the control word. When a given Si8380S device in the daisy chain is presented with the CID[3:0] code of 0000, it is activated as the one to be addressed. All remaining operations between the SPI master and the Si8380S activated in this manner proceed as previously discussed in 3.5 Serial Peripheral Interface for the case of a single Si8380S slave. The organization of a system with Si8380S devices daisy-chained in this manner is depicted in the figure below.

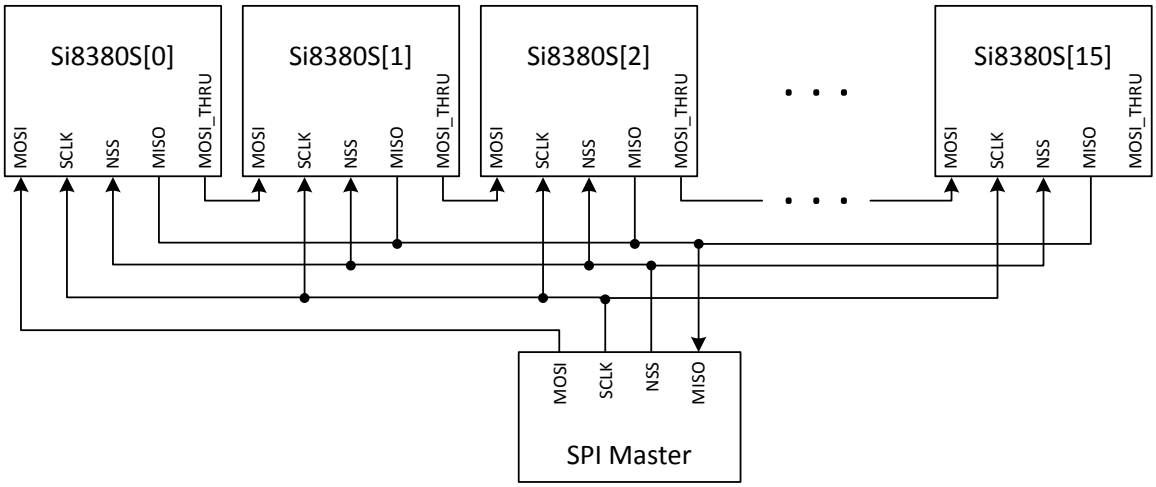


Figure 3.7. SPI Daisy-Chain Organization

From the preceding figure, and referring to Figure 3.4 SPI Communication Packet Structure, Write Operation and Control Byte Structure on page 8, in order to read from Si8380S[1], the control word would be:

Control[7:0] = 0100_1000.

Similarly, in order to write to Si8380S[12], the control word would be:

Control[7:0] = 0000_0011.

Finally, if it were desired to update an internal SPI register of all daisy-chained Si8380S devices, the control word would be:

Control[7:0] = 1000_0000.

If the broadcast bit is zero during a write operation, only the Si8380S device being addressed using the CID[3:0] field of the control word in a daisy-chain organization will be updated. If the broadcast bit is one during a write operation, the CID[3:0] field is ignored, and all Si8380S devices connected in a daisy chain will be updated. For non-daisy-chain operation, the CID[3:0] field should always be all zeros.

Note that there is a finite combinational delay associated with passing the MOSI input pin of a given Si8380S to the MOSI_THRU output pin. As a result, the maximum possible SCLK frequency will be reduced based on the number of Si8380S devices connected in a daisy-chain organization.

3.5.6 SPI Interface Timing Specification

The timing diagram for the Si8380S SPI interface is presented in the figure below.

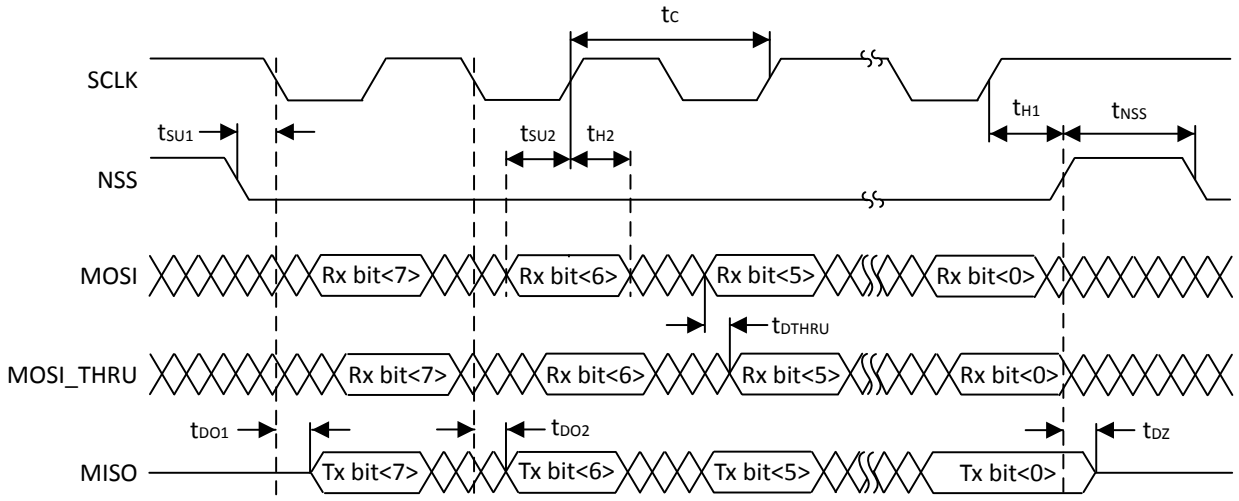


Figure 3.8. SPI Timing Diagram

The timing specifications depicted in this figure apply to each byte of the three byte Si8380S SPI communications packet. Refer to the SPI timing specifications in Table 5.3 SPI Timing Characteristics[1] on page 18.

Although this discussion of the Si8380S SPI interface has focused on a preferred organization (separate MISO/MOSI wires), other options are available with regard to the Si8380S control interface. Possible Si8380S organizations include:

- MISO/MOSI wired operation
  - MISO/MOSI may be two separate wires, or may be connected together if the SPI master is capable of tri-stating its MOSI pin during the data byte packet transfer of a read operation.
- Multiple Si8380S devices interfaced in a non-daisy-chain format
  - The SPI master provides multiple NSS signals, one for each of a multiple of Si8380S slaves.
  - Every Si8380S shares a single trace from its MOSI input back to the SPI master (the Si8380S MOSI_THRU signal is not utilized).

3.6 Debounce Filter

The Si838x has a debounce filter on low-speed channels. The high-speed channels have no debounce filtering. The debounce filter can be configured either through part number selection for parallel output devices, or through the SPI interface on the Si8380S device. When using the Si8380S device, the user has control over the debounce filter mode and filter delay on a per channel basis. Parallel output devices with low-speed channels use the low-pass filtering mode as defined in 3.6.2 Debounce Filtering Modes. Parallel output devices also feature part number selectable debounce filter delay times of 0, 10, 30 and 100 ms. The debounce filter is incorporated directly into the path of the input data stream on low-speed channels allowing signal conditioning of the digital inputs to reduce noise and improve common mode transient immunity (CMTI.) See 1. Ordering Guide for more details on part numbers.

3.6.1 Debounce Control Registers

When using the Si8380S, debounce filter operation is controlled using read/write control registers mapped into the Si8380S SPI address space. The details of these registers are covered in section 3.5.1 SPI Register Map. The options available using these registers are outlined in tables below. For each of the eight input channels, two data bits are allocated to control the debounce delay, and two data bits are used to select the debounce filtering mode. This consumes a total of 32 bits, which are allocated across four individual Si8380S SPI control registers of one byte each.

Table 3.3. Debounce Filter Delay Control

dbnc_dly[1:0]	Delay (ms)	Comment
00	0	No additional debounce filter delay
01	10	Fast debounce filter delay
10	30	Medium debounce filter delay
11	100	Slow debounce filter delay
Note: All low-speed channels include a built-in 4 µs low-pass debounce filter delay. Additional delay may be added based on the debounce filter delay control setting.		

Table 3.4. Debounce Filter Mode Control

dbnc_mode[1:0]	Filter Mode	Comment
00	Deglitch filter	Simple trailing edge delay filter
01	Low-pass filter	Replicates a traditional low-pass filter
1X	Blanking filter	Leading edge delay filter

3.6.2 Debounce Filtering Modes

In addition to configuring filter delay time, the user can also select between three filtering modes provided by the debounce function which result in different filter behavior. Like the debounce filter delay setting, these debounce filter modes may be unique for each of the eight Si8380S input channels. All low-speed channels present on parallel output devices are configured with the low-pass filter mode only.

The first of these three modes, corresponding to dbnc_mode[1:0] == 00, employs only a simple trailing edge delay commonly used in digital deglitch filters. In this mode, once the channel's input has been stable for the amount of time specified in the corresponding channel's debounce delay setting t_D, the channel's output assumes the value of the channel's input. Consequently, any glitches on the channel's input having a duration less than the channel's debounce delay setting t_D, will be suppressed.

The second mode, corresponding to dbnc_mode[1:0] == 01, performs a low-pass filtering function on the input channel and is the mode of the built-in 4 µs filter found in all low-speed channels. When the channel's input has assumed a new value, a counter begins counting toward the debounce delay setting t_D. If before the count t_D is reached the channel's input returns to its previous value, this counter is decremented. Assuming that the channel's input again assumes the new value before the counter is decremented back to 0 (i.e., noise pulse width is less than the time the channel's input had previously assumed a new value), the counter incrementing resumes from a non-zero value. Once this count has reached the designated delay t_D, the channel's output assumes the new value. Using this mechanism, any noise pulse on the channel's input having a duration less than the channel's debounce filter delay setting t_D, will be suppressed. However, unlike dbnc_mode[1:0] == 00, when the channel's input returns to the new value after this noise pulse, credit is given for the time this new value was active before the pulse.

The final mode, corresponding to dbnc_mode[1:0] == 1X, realizes a leading edge filtering function on the input channel, similar to a blanking filter. Internally, a counter is initialized to zero. When the channel's input changes, the channel's output immediately assumes the new value, and the counter is reset to the current delay setting t_D. Independent of what occurs on the channel's input, the counter begins decrementing after this change, leaving the channel blind to changes on the input. When the counter again reaches zero, the channel's current input is compared to the channel's current output. If they are different the channel's output immediately assumes the new value. If they are the same, the channel's output will immediately change on the next new value seen by the channel's input. In either case, a change on the channel's input resets the counter to the current delay setting t_D.

A graphical depiction of the operation and behavior for each debounce filter mode is provided in the following figure, which has been constrained to the signal path within the filter function only.

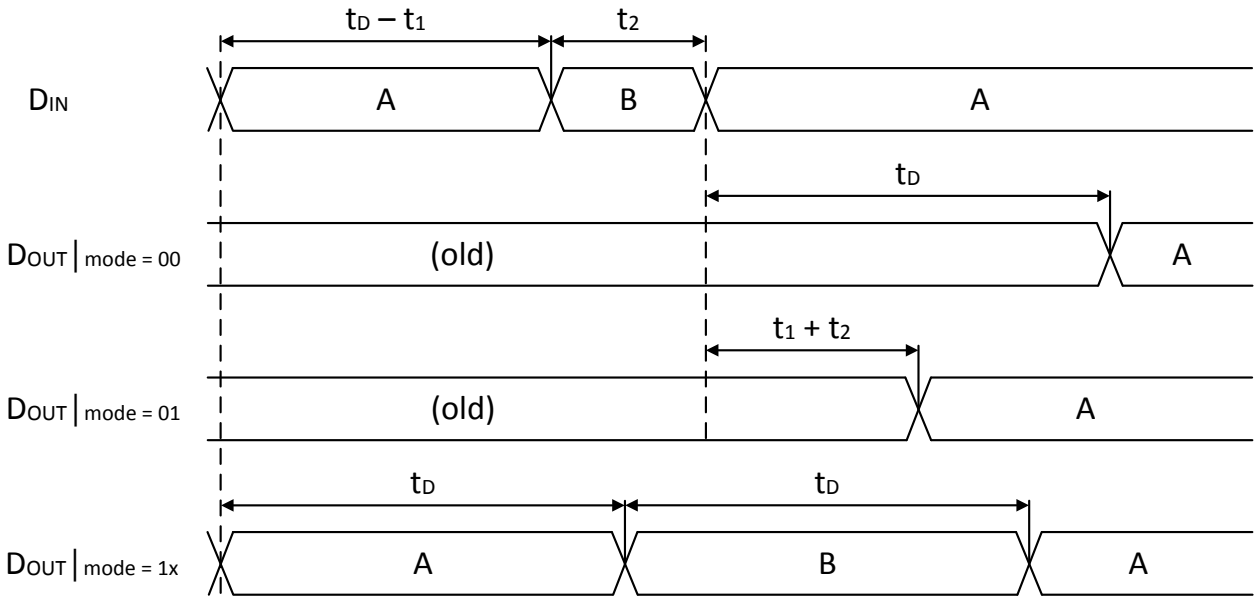


Figure 3.9. Debounce Filter Modes Timing Diagram

4. Applications

4.1 System Level Transitions

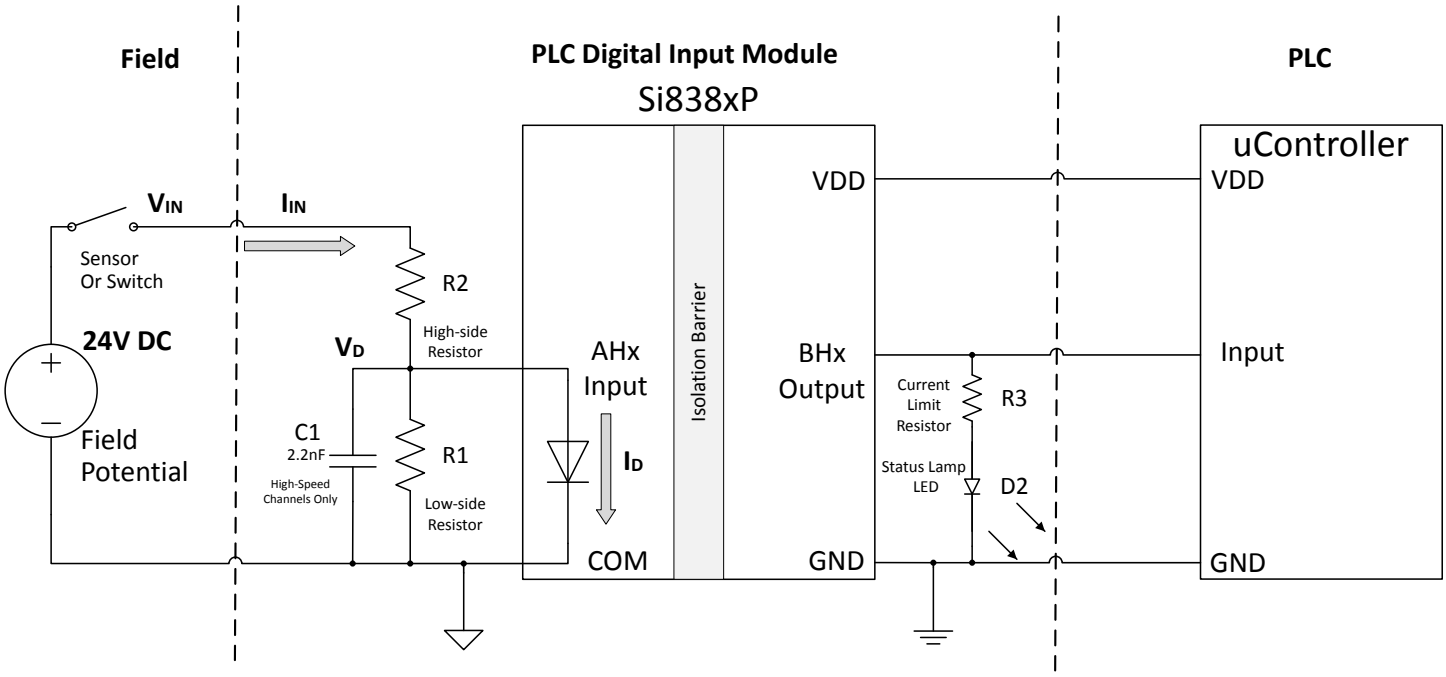


Figure 4.1. System Level Drawing of a High-speed Channel on the Si838x with the Supporting Bill of Materials

The Si838x combined with an appropriate input resistor network and indication LED will produce a 24 V digital input module which adheres to the IEC 61131-2 specification.

Resistors R1 and R2 set the transition voltages and currents for the system, as visualized in the figure below, while capacitor C1, is required only for high-speed channels and serves to improve CMTI performance. Further, resistor R3 is selected based on desired LED, D2, brightness during a system ON condition.

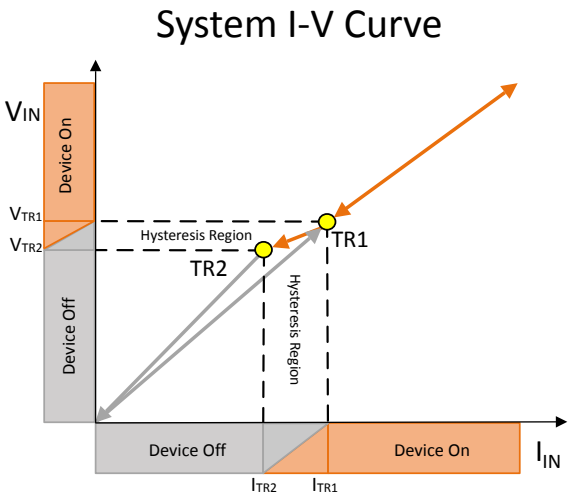


Figure 4.2. Visualization of System Level Transitions when Using an Si838x According to the Recommended Design Process

4.2 IEC 61131-2 Compliance Options

The IEC 61131-2 standard articulates three types of digital inputs for 24V logic sensing. Each type category dictates boundary conditions on the system level input space, (V_{IN}, I_{IN}), defining the range of values for which the module must output a logic LOW, a logic HIGH, or transition between the two.

The table below provides a per-input type bill of materials recommendation for plug-n-play designs adhering to the specification or as a starting point for custom designs. These recommendations assume a resistor tolerance of 5%. A custom input design does not need to follow the recommendations listed in the table below. However, it is important that a custom design adhere to the electrical specifications defined in Table 5.2 Electrical Characteristics on page 16.

Table 4.1. Si838x Recommended Input Bill of Materials and System Level Transition Values

	Input Resistor Values		Nominal TR1 Values		Nominal TR2 Values	
PLC Digital Input Type	R1 (Ω)	R2 (Ω)	I_{IN} (mA)	V_{IN} (V)	I_{IN} (mA)	V_{IN} (V)
Type-1	2400	6200	1.18	8.70	1.07	7.97
Type-2	390	1500	4.14	7.60	3.88	7.13
Type-3	750	2700	2.45	7.98	2.27	7.44
Note: Based on 24 V DC PLC digital input types as defined by IEC 61131-2.						

4.3 Custom Bill of Materials

A PLC digital input module based on the Si838x can have its transition values customized on a per-channel basis in accordance with the system level equations and tolerances. An extended discussion of this process and an example design are available in AN970: Design Guide for PLC Digital Input Modules Using the Si838x.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
VDD Supply Voltage	VDD	2.25	—	5.5	V
Maximum data rate, high-speed channels		—	2	—	Mbps
Maximum data rate, low-speed channels, (+0 ms t_D)		—	250	—	kbps
Maximum data rate, low-speed channels, (+10 ms t_D)		—	100	—	bps
Maximum data rate, low-speed channels, (+30 ms t_D)		—	33	—	bps
Maximum data rate, low-speed channels, (+100 ms t_D)		—	10	—	bps
Input Current (sinking or sourcing)	$\lvert I_{F(ON)} \rvert$	1.0	—	20	mA
Operating Temperature (Ambient)	T_A	–40	—	+125	°C
Note: The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.					

Table 5.2. Electrical Characteristics

VDD = 2.25 V – 5.5 V; GND = 0 V; T_A = –40 to +125 °C; typical specs at 25 °C; VDD = 5 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Current Threshold	$I_{F(TH)}$		460	606	950	µA
Input Current Hysteresis[1]	I_{HYS}		30	76	200	µA
Input Voltage Threshold	$V_{F(TH)}$		1.21	1.38	1.5	V
Input Voltage Hysteresis[2]	V_{HYS}		30	73	130	mV
Input Capacitance	C_I	f = 100 kHz	—	105	—	pF
VDD Undervoltage Threshold	VDD_{UV+}	VDD rising	1.93	2.06	2.19	V
VDD Undervoltage Threshold	VDD_{UV-}	VDD falling	1.79	1.91	2.01	V
VDD Undervoltage Hysterisis	VDD_{HYS}		—	150	—	mV
Low-Level Input Voltage	V_{IL}	SCLK, NSS, MOSI	—	—	0.8	V
High-Level Input Voltage	V_{IH}	SCLK, NSS, MOSI	2.0	—	—	V
Low-Level Output Voltage	V_{OL}	IOL = 4 mA	—	—	0.4	V
High-Level Output Voltage	V_{OH}	IOH = –4 mA	VDD – 0.4	—	—	V
Output Impedance	Z_O		—	50	—	Ω

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Current (All Inputs 0 or 1)						
IDD		All inputs 0	2.8	4.8	6.7	mA
		All inputs 1	3.6	5.4	7.6	mA
125 kHz Supply Current						
IDD		All inputs switching	3.7	5.5	7.7	mA
1 MHz (2 Mbps) Supply Current						
IDD		All inputs switching	3.9	5.6	8.0	mA
Timing Characteristics (VDD = 5 V, C_L = 15 pF)						
Propagation Delay[3]	t_P	AHx channels	47	82	124	ns
		Ax channels (+0 ms t_D)	3.8	4.1	4.6	µs
		Ax channels (+10 ms t_D)	—	10	—	ms
		Ax channels (+30 ms t_D)	—	30	—	ms
		Ax channels (+100 ms t_D)	—	100	—	ms
Pulse Width Distortion[3]	PWD	AHx channels	—	6	50	ns
		Ax channels	—	80	—	ns
Propagation Delay Skew[4]	$t_{PSK(P-P)}$	AHx channels	—	—	±30	ns
		Ax channels	—	—	±80	ns
Channel–Channel Skew[5]	t_{PSK}	AHx channels	—	—	±30	ns
		Ax channels	—	—	±80	ns
Output Rise Time	t_R	50 Ω load +100 pF	—	3.9	—	ns
Output Fall Time	t_F	50 Ω load +100 pF	—	3.7	—	ns
Device Startup Time	t_{START}		—	150	—	µs
Common Mode Transient Immunity[6]	CMTI	AHx channels	25	50	—	kV/µs
		Ax channels	200	300	—	kV/µs

Notes:

1. The current value at which device turns off is determined by $I_{F(OFF)} = I_{F(TH)} - I_{HYS}$.
2. The voltage value at which the device turns off is determined by $V_{F(OFF)} = V_{F(TH)} - V_{HYS}$.
3. See Figure 3.1 Si838x Timing Diagram on page 5 for propagation delay test conditions and pulse width distortion test conditions.
4. Propagation delay skew is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
5. Channel-channel skew is the magnitude of the difference in propagation delay times measured between different channels operating at the same supply voltages, load, and ambient temperature.
6. See Figure 5.1 Common Mode Transient Immunity (CMTI) Measurement Circuit on page 19 for CMTI test conditions.

Table 5.3. SPI Timing Characteristics[1]

VDD = 2.25 V – 5.5 V; GND = 0 V; T_A = –40 to +125 °C; typical specs at 25 °C; VDD = 5 V

Parameter	Symbol	Min	Typ	Max	Unit
Cycle time (SCLK)[2]	t_C	100	—	—	ns
Delay time, SCLK fall to MISO active	t_{DO1}	—	—	20	ns
Delay time, SCLK fall to MISO transition	t_{DO2}	—	—	20	ns
Delay Time, NSS rise to MISO hi-Z	t_{DZ}	—	—	20	ns
Setup time, NSS fall to SCLK fall	t_{SU1}	25	—	—	ns
Hold time, SCLK rise to NSS rise	t_{H1}	20	—	—	ns
Setup time, MOSI to SCLK rise	t_{SU2}	25	—	—	ns
Hold time, SCLK rise to MOSI transition	t_{H2}	20	—	—	ns
Delay time between NSS active	t_{NSS}	200	—	—	ns
Propagation delay, MOSI to MOSI_THRU[2]	t_{DTHRU}	—	—	15	ns

Notes:

1. See Figure 3.8 SPI Timing Diagram on page 11 for SPI timing characteristics test conditions.
2. When implementing a daisy chain, see 3.5.5 SPI Daisy-Chain Organization for cycle time considerations. Cycle time will increase according to $t_C(N) = t_{C(MIN)} + t_{DTHRU}(N-1)$ where N is the number of Si8380S devices present in the daisy chain.

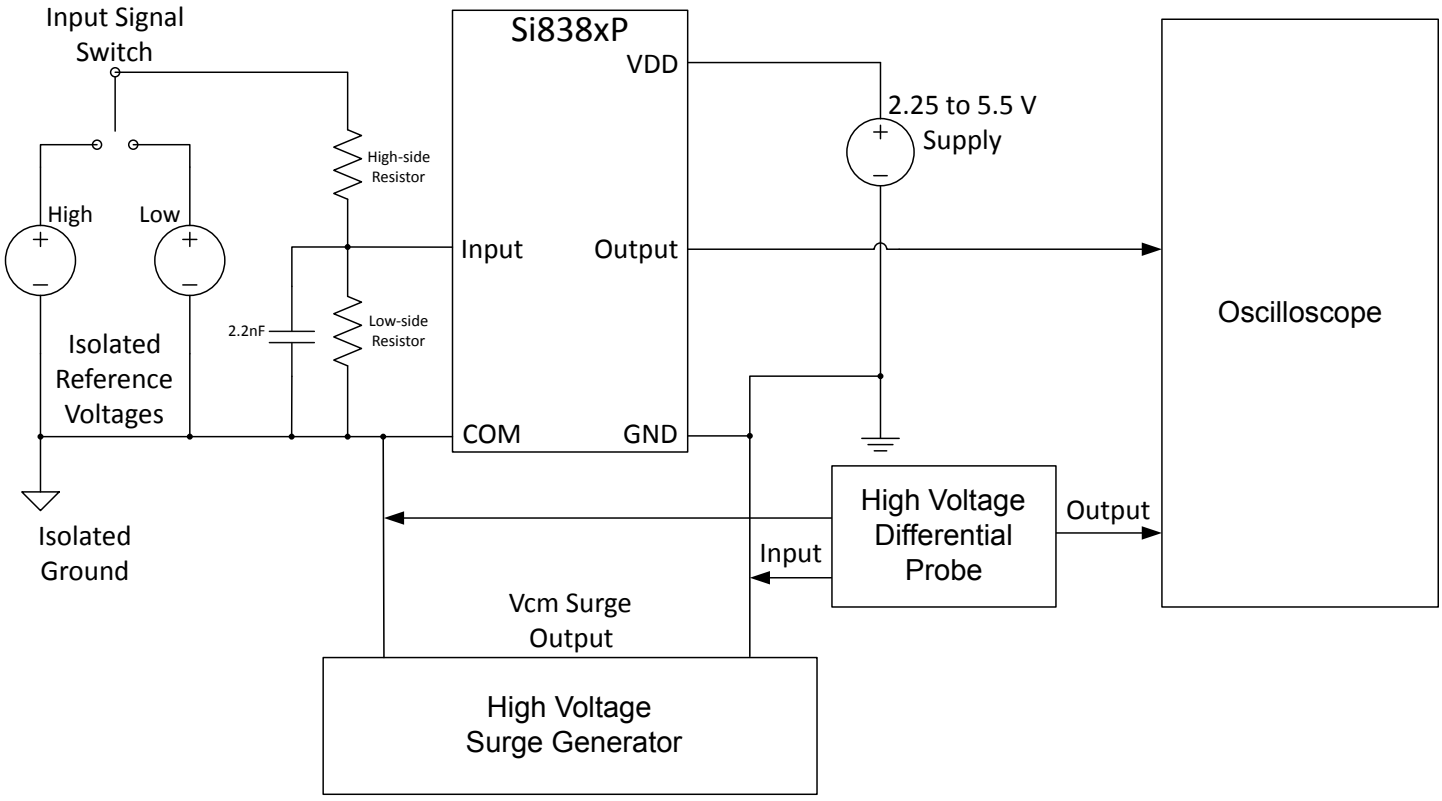


Figure 5.1. Common Mode Transient Immunity (CMTI) Measurement Circuit

Table 5.4. Regulatory Information[1]

CSA
The Si838x is certified under CSA Component Acceptance Notice 5A. For more details, see Master Contract Number 232873.
60950-1: Up to 148 V_{RMS} reinforced insulation working voltage. Up to 460 V_{RMS} basic insulation working voltage.
62368-1: Up to 300 V_{RMS} basic insulation working voltage.
VDE
The Si838x is certified according to VDE0884. For more details, see Certificate 40018443.
VDE 0884-10: 560 V_{PEAK} for basic insulation working voltage
UL
The Si838x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V_{RMS} isolation voltage for single protection.
CQC
The Si838x is certified under GB4943.1-2011. For more details, see Certificate CQC16001160381.
Rated up to 250 V_{RMS} basic insulation working voltage.
Note: 1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices that are production tested to 3.0 kV_{RMS} for 1 s. For more information, see 1. Ordering Guide.

Table 5.5. Insulation and Safety-Related Specifications[1]

Parameter	Symbol	Test Condition	QSOP-20	Unit
Nominal External Air Gap (Clearance)	CLR		3.6 min	mm
Nominal External Tracking (Creepage)	CPG		3.6 min	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.008	mm
Tracking Resistance	CTI	IEC60112	600	V
Erosion Depth	ED		0.057	mm
Resistance (Input-Output)[1]	RIO		10^{12}	Ω
Capacitance (Input-Output)[1]	CIO	f = 1 MHz	1	pF

Note:
1. To determine resistance and capacitance, the Si838x is converted into a 2-terminal device. Pins 1–10 are shorted together to form the first terminal, and pins 11–20 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 5.6. IEC 60664-1 Ratings

Parameter	Test Condition	QSOP-20
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I–IV
	Rated Mains Voltages < 300 V_{RMS}	I-III
	Rated Mains Voltages < 400 V_{RMS}	I-II
	Rated Mains Voltages < 600 V_{RMS}	I-II

Table 5.7. VDE 0884-10 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
			QSOP-20	
Maximum Working Insulation Voltage	V_{IORM}		560	V_{PEAK}
Input to Output Test Voltage	V_{PR}	Method b1 (VIORM x 1.875 = VPR,100%) Production Test, tm = 1 sec, (Partial Discharge < 5 pC)	1050	V_{PEAK}
Transient Overvoltage	V_{IOTM}	t = 60 s	4000	V_{PEAK}
Surge Voltage	V_{IOSM}	Tested per IEC 60065 with surge voltage of 1.2 µs/50 µs (Si838x tested with 4000 V)	3077	V_{PEAK}
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at TS, V_{IO} = 500 V	R_S		$>10^9$	Ω

Note:
1. This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si838x provides a climate classification of 40/125/21.

Table 5.8. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max	Unit
			QSOP-20	
Safety Temperature	T_S		150	°C
Safety Current	I_S	θ_{JA} = 105 °C/W V_F = 2.8 V, VDD = 5 V, T_J = 150 °C, T_A = 25 °C	240	mA
Power Dissipation	P_S		1.2	W

Note:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 5.2 (QSOP-20) Thermal Derating Curve, Dependence of Safety Limiting Values per VDE on page 22.

Table 5.9. Thermal Characteristics

Parameter	Symbol	QSOP-20	Unit
IC Junction-to-Ambient Thermal Resistance	θ_{JA}	105	°C/W

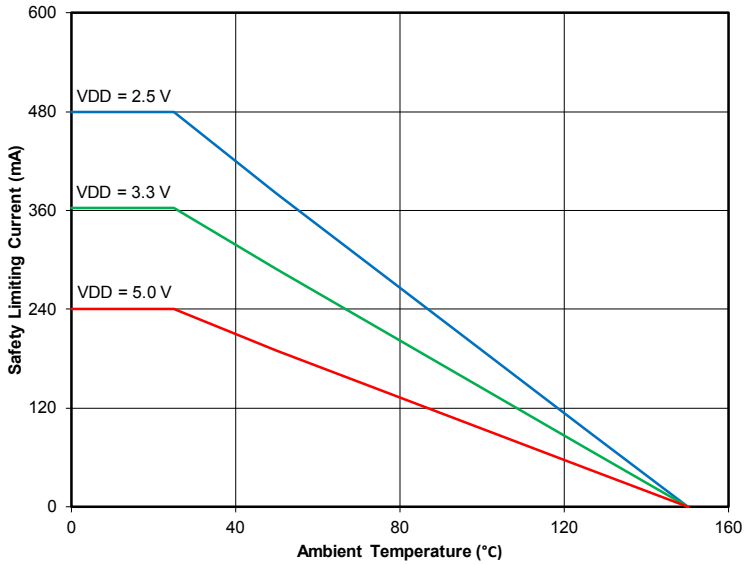


Figure 5.2. (QSOP-20) Thermal Derating Curve, Dependence of Safety Limiting Values per VDE

Table 5.10. Absolute Maximum Ratings[1]

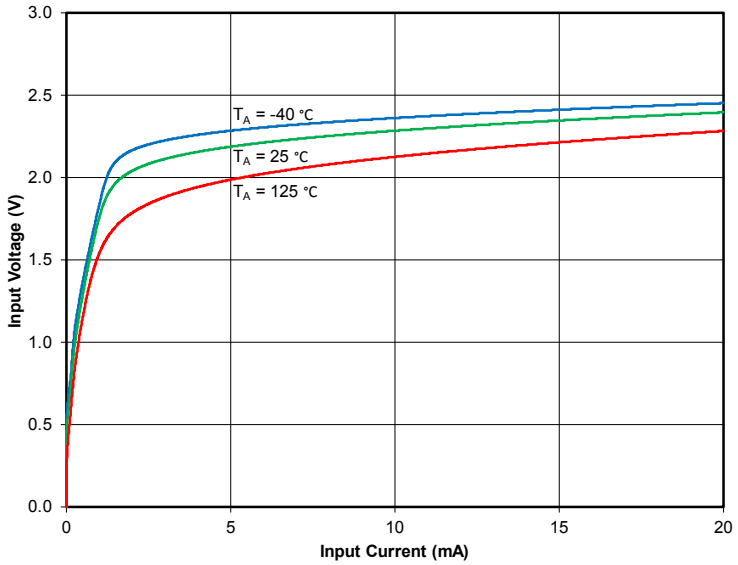
Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	+150	°C
Ambient Temperature	T_A	–40	+125	°C
Junction Temperature	T_J	—	+150	°C
Average Forward Input Current	$I_{F(AVG)}$	—	30	mA
Peak Transient Input Current (< 1 µs pulse width, 300 ps)	I_{FTR}	—	1	A
Supply Voltage	VDD	–0.5	7	V
Output Voltage	V_{OUT}	–0.5	VDD+0.5	V
Average Output Current	$I_{O(AVG)}$	—	10	mA
Input Power Dissipation	P_I	—	480	mW
Output Power Dissipation (includes 3 mA per channel for status LED)	P_O	—	484	mW
Total Power Dissipation	P_T	—	964	mW
Lead Solder Temperature (10 s)		—	260	°C
HBM Rating ESD		4	—	kV
Machine Model ESD		200	—	V
CDM		500	—	V
Maximum Isolation Voltage (1 s)		—	3000	V_{RMS}

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.

5.1 Typical Operating Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to Table 5.2 Electrical Characteristics on page 16 for actual specification limits.



Note: Input current and input voltages depicted in the figure above are absolute values and apply to both sourcing and sinking channel designs.

Figure 5.3. Input Voltage vs. Input Current Over Temperature

6. Pin and Package Definitions

The Si838x consists of multiple dies in one package. Each package and bond-out serves a customer need and may reflect multiple bond options. The following packages are defined: QSOP-20. 1. Ordering Guide describes the part number and configuration for these products. Subsequent sections define the pins for each package type and the product block diagrams.

6.1 Pin Descriptions and Block Diagrams

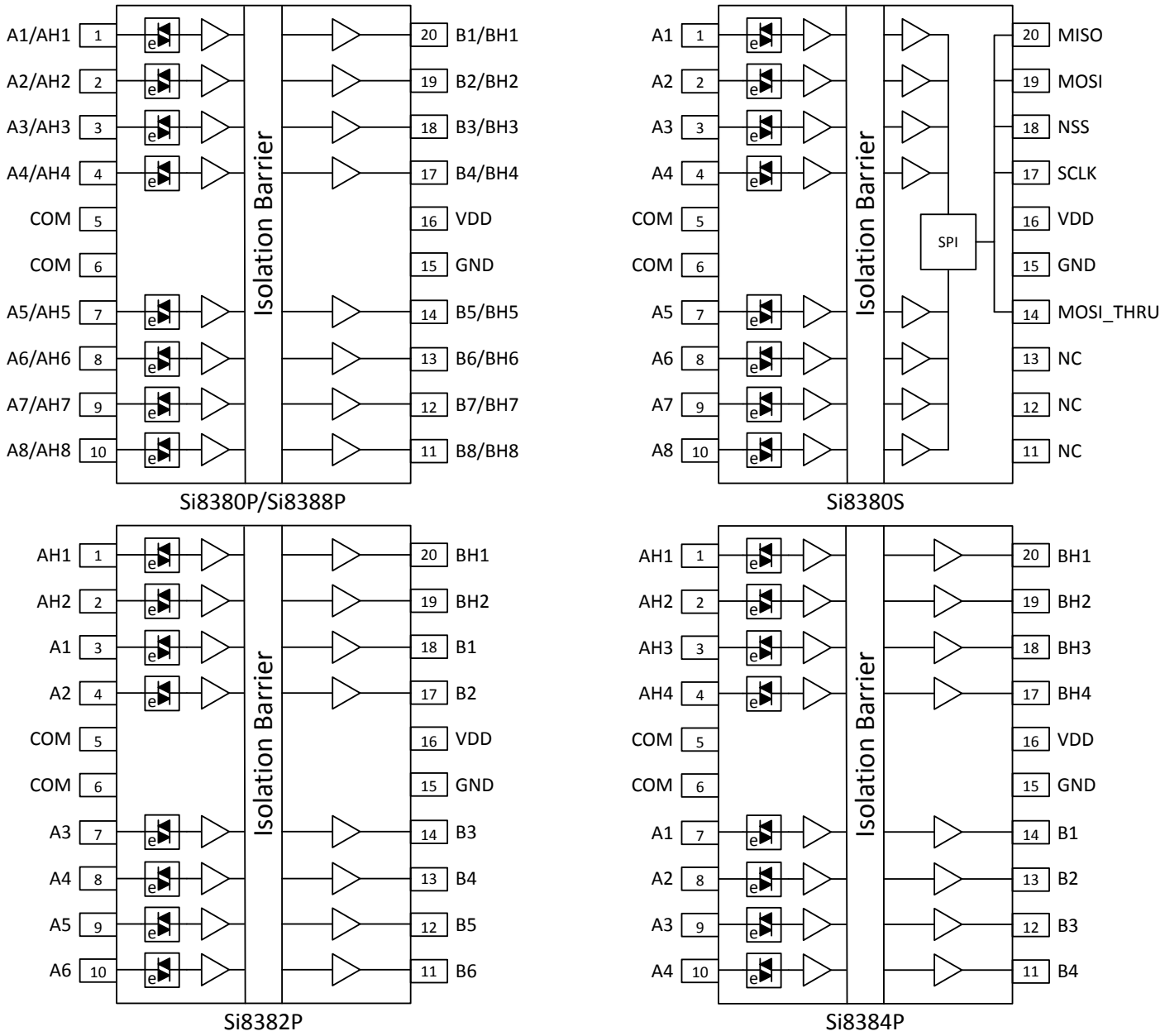


Figure 6.1. Si838x Pin Assignments and Block Diagrams

Table 6.1. Si838x Pin Descriptions

Pin Name	Description
A1 – A8	Low-speed input channels
AH1-AH8	High-speed input channels
COM	Common. Can be connected to ground for sinking inputs or the field supply for sourcing inputs
B1-B8	Low-speed output channels
BH1-BH8	High-speed output channels
VDD	Controller side power supply
GND	Controller side ground
MOSI	SPI, input
SCLK	SPI clock
NSS	SPI chip select
MOSI_THRU	SPI serial data out for cascading multiple Si8380S devices (up to 16)
MISO	SPI, output

7. Package Outline

The figure below illustrates the package details for the 20-pin QSOP package. The table below lists the values for the dimensions shown in the illustration.

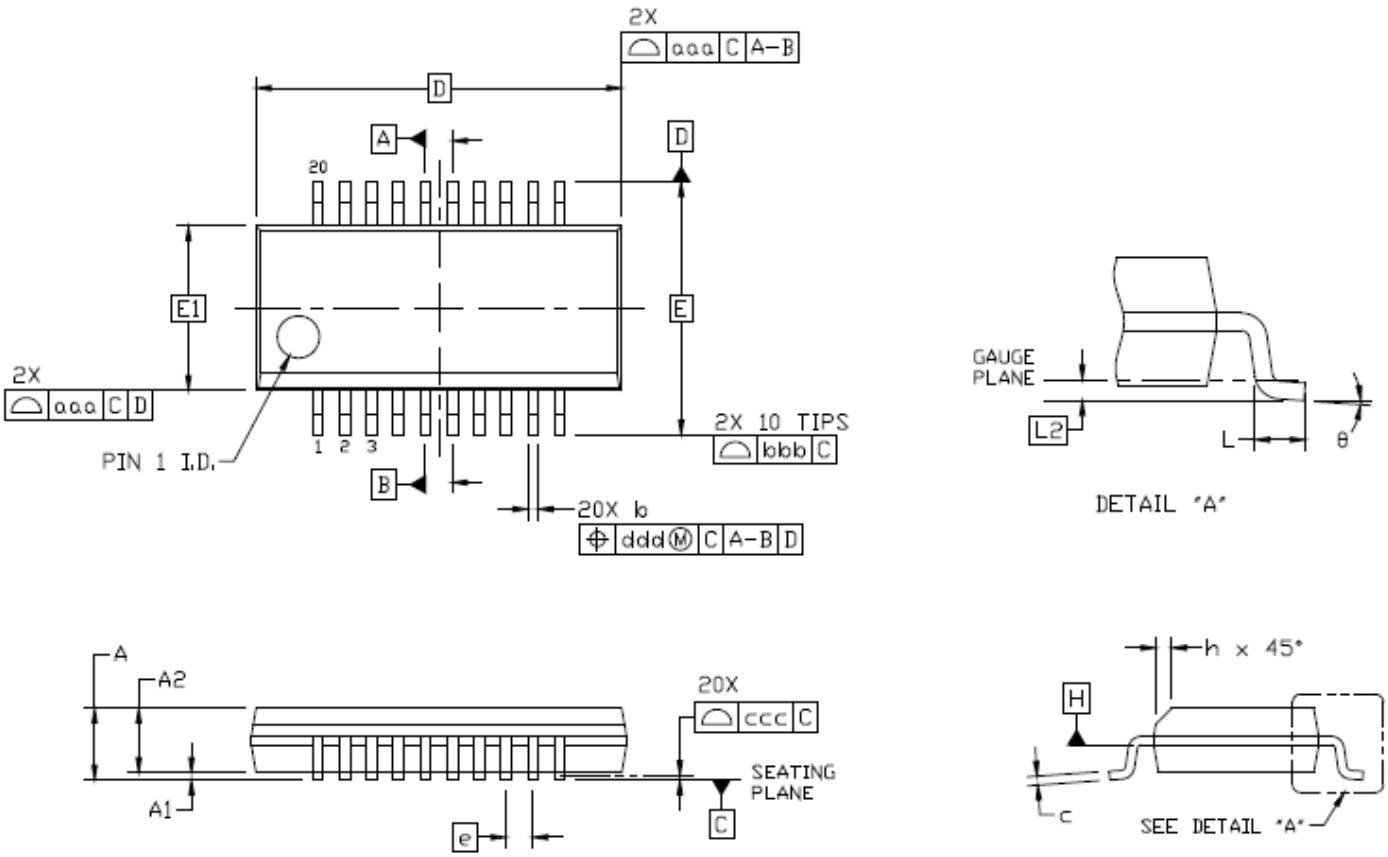


Figure 7.1. 20-Pin QSOP Package Outline

Table 7.1. Package Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	8.66 BSC	
E	6.00 BSC	
E1	3.91 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.20	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline M0-137, Variation AD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Land Pattern

The figure below illustrates the PCB land pattern details for the 20-pin QSOP package. The table below lists the values for the dimensions shown in the illustration.

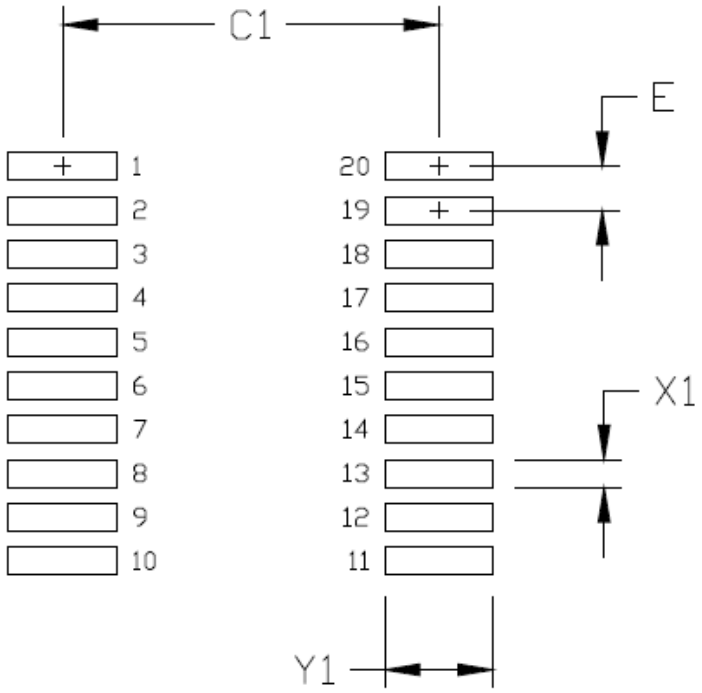


Figure 8.1. 20-Pin QSOP PCB Land Pattern

Table 8.1. 20-Pin QSOP PCB Land Pattern Dimensions

Dimension	Feature	mm
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	0.635
X1	Pad Width	0.40
Y1	Pad Length	1.55

1. This Land Pattern Design is based on IPC-7351 design rules for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

9. Top Marking

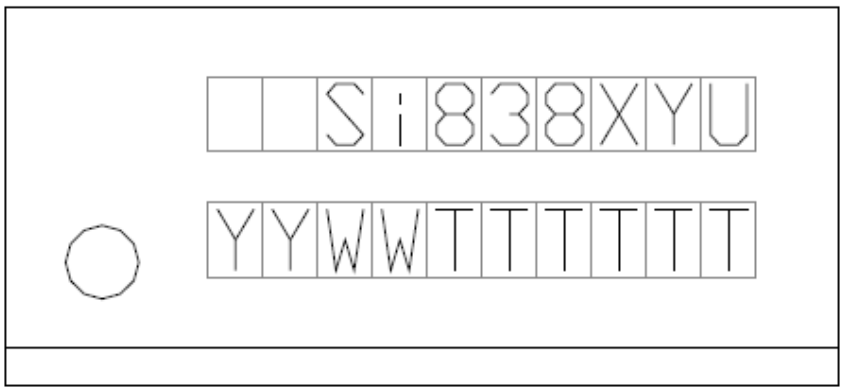


Figure 9.1. Si838x Top Marking (20-Pin QSOP)

Table 9.1. Top Marking Explanation (20-Pin QSOP)

Line 1 Marking:	Base Part Number Ordering Options See 1. Ordering Guide for more information.	Si838 = 8-ch digital input isolator X = # of high-speed channels Y = S, P S = serial outputs P = parallel outputs U = Debounce option None = No additional debounce filter delay time F = fast debounce filter delay time, 10 ms M = medium debounce filter delay time, 30 ms S = slow debounce filter delay time, 100 ms
Line 2 Marking:	YY = Year WW = Workweek TTTTTT = Mfg Code	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date and manufacturing code from Assembly Purchase Order form.

10. Revision History

Revision 1.0

April, 2019

- Reorganized document to improve readability
- Updated content throughout the data sheet to improve readability, matched style guidelines, and corrected minor grammatical errors
- Corrected the output state when device is unpowered in Table 3.1 Truth Table Summary on page 5
- Added 3.3 Bipolar LED Emulator Input to improve input channel design documentation
- Added recommendation to control output states to 3.4.2 Output Pin Termination and State Control
- Removed redundant specifications, added details and notes, and reorganized 5. Electrical Specifications
- Added Input Voltage specifications to Table 5.2 Electrical Characteristics on page 16
- Expanded and clarified Propagation Delay specifications in Table 5.2 Electrical Characteristics on page 16
- Expanded and clarified Propagation Delay specifications in Table 5.2 Electrical Characteristics on page 16
- Defined capacitive load in test conditions for rise and fall time in Table 5.2 Electrical Characteristics on page 16
- Updated Table 5.4 Regulatory Information[1] on page 20 to reflect latest certification status
- Added surge voltage specification to Table 5.7 VDE 0884-10 Insulation Characteristics[1] on page 21
- Corrected Safety Current specification in 4.2 IEC 61131-2 Compliance Options
- Corrected plot in Figure 5.2 (QSOP-20) Thermal Derating Curve, Dependence of Safety Limiting Values per VDE on page 22
- Removed input voltage parameter from Table 5.10 Absolute Maximum Ratings[1] on page 23
- Updated plot in Figure 5.3 Input Voltage vs. Input Current Over Temperature on page 24
- Corrected Line 1 Marking in Table 9.1 Top Marking Explanation (20-Pin QSOP) on page 30

Revision 0.5

April, 2016

- Initial release.