DATA SHEET

Si86S60x: Low Power I²C Isolators

Industrial Applications

- Isolated I²C, System Management Bus (SMBus)
- Isolated digital power supply communications
- Power over Ethernet
- Motor control systems
- Intelligent power systems

Automotive Applications

- Onboard chargers
- Battery management systems
- Charging stations
- Traction inverters
- Hybrid electric vehicles
- Battery electric vehicles

Features

- Independent, bidirectional SDA/SCL isolation channels
- Open drain outputs with 35 mA sink current
- Supports I²C clocks up to 1.7 MHz
- Unidirectional isolation channels support additional system signals (Si86S605, Si86S606)
- Up to 6000 V_{RMS} isolation
- UL, CSA, VDE, CQC recognition
- High electromagnetic immunity
- Wide operating supply voltage
- 3.0 to 5.5 V
- AEC-Q100 qualification
- Wide temperature range
  - –40 to +125 °C
- Transient immunity 100 kV/µs
- RoHS-compliant packages
  - NB SOIC-8
  - SSO-8
  - WB SOIC-16
  - QSOP-16
- Automotive-grade OPNs available
  - AIAG compliant PPAP documentation support
  - IMDS and CAMDS listing support

Safety Regulatory Approvals (Pending)

- UL 1577 recognized
  - Up to 6000 V_{RMS} for 1 minute
- CSA certification conformity
  - 62368-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1

Description

The Si86S60x series of isolators are single-package galvanic isolation solutions for I²C and SMBus serial port applications. These products are based on Skyworks proprietary capacitive isolation technology and offer shorter propagation delays, lower power consumption, smaller installed size, and more stable operation with temperature and age versus optocouplers or other digital isolators. All devices in this family include bidirectional SDA and/or SCL isolation channels with open-drain, 35 mA sink capability that operate to a maximum frequency of 1.7 MHz. The 8-pin versions supports bidirectional SDA and SCL isolation; the Si86S602 supports bidirectional SDA and unidirectional SCL isolation, and the 16-pin versions (Si86S605, Si86S606) feature two unidirectional isolation channels to support additional system signals, such as interrupts or resets. All versions contain protection circuits to guard against data errors when an unpowered device is inserted into a powered system. Small size, low installed cost, low power consumption, and short propagation delays make this family the optimum solution for isolating I²C and SMBus serial ports. Automotive grade products are available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

1. Pin Descriptions

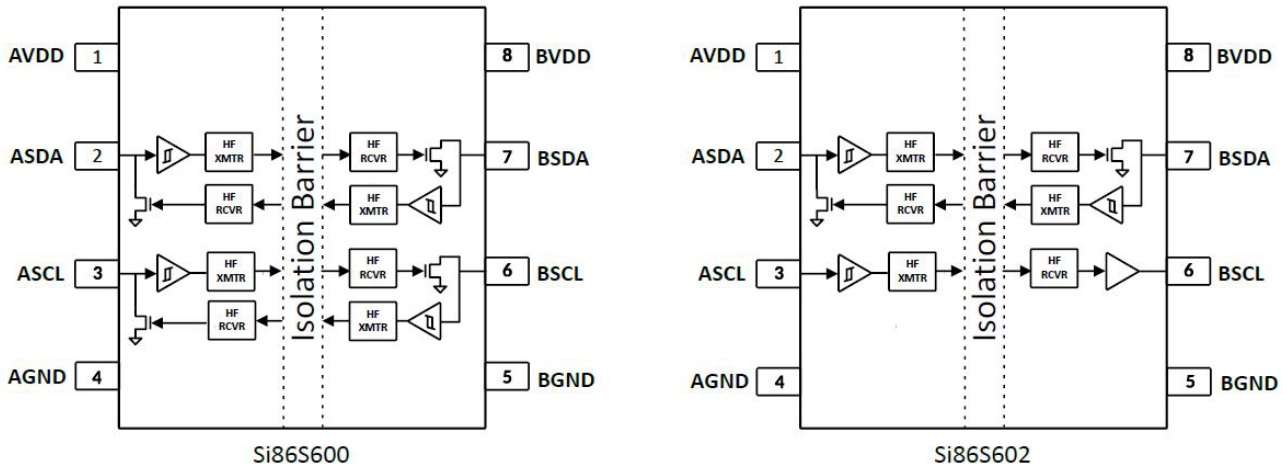

Figure 1. Si86S600/02 Pinout

Table 1. Si86S600/02 in SOIC-8 and SSO-8 Package

Pin	Name	Description
1	AVDD	Side A power supply terminal; connect to a source of 3.0 to 5.5 V.
2	ASDA	Side A data (open drain) input or output.
3	ASCL	Side A clock input or output. Open drain I/O for Si86S600. Standard CMOS input for Si86S602.
4	AGND	Side A ground terminal.
5	BGND	Side B ground terminal.
6	BSCL	Side B clock input or output. Open drain I/O for Si86S600. Push-pull output for Si86S602.
7	BSDA	Side B data (open drain) input or output.
8	BVDD	Side B power supply terminal; connect to a source of 3.0 to 5.5 V.

1.1. Si86S605/06 Pinout

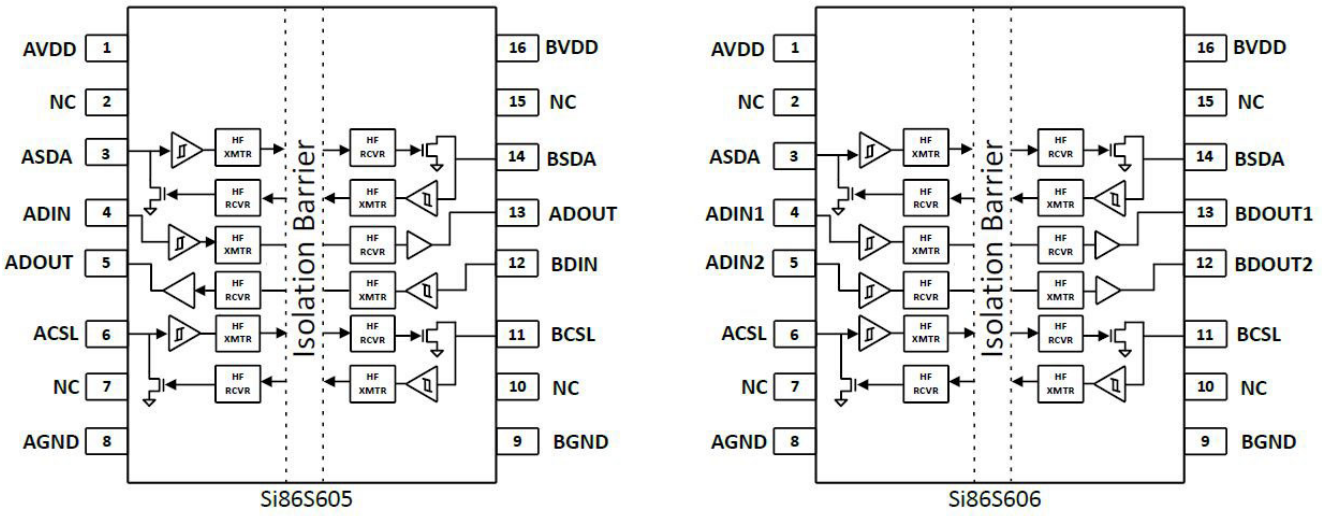

Figure 2. Si86S605/06 Pinout

Table 2. Si86S605/06 in QSOP-16 and WB SOIC-16 Package

Pin	Name	Description
1	AVDD	Side A power supply terminal. Connect to a source of 3.0 to 5.5 V.
2	NC	No connection.
3	ASDA	Side A data (open drain) input or output.
4	ADIN/ADIN1	Side A standard CMOS digital input (non I^2C).
5	ADOUT/ADIN2	Side A digital input/output (non I^2C). Standard CMOS digital input for Si86S606. Push-Pull output for Si86S605.
6	ASCL	Side A clock input or output. Open drain I/O for Si86S605/06.
7	NC	No connection.
8	AGND	Side A ground terminal.
9	BGND	Side B ground terminal.
10	NC	No connection.
11	BSCL	Side B clock input or output. Open drain I/O for Si86S605/06.
12	BDIN/BDOUT2	Side B digital input/output (non I^2C). Standard CMOS digital input for Si86S605. Push-Pull output for Si86S606.
13	BDOUT/BDOUT1	Side B digital push-pull output (non I^2C).
14	BSDA	Side B data open drain input or output.
15	NC	No connection.
16	BVDD	Side B power supply terminal. Connect to a source of 3.0 to 5.5 V.

2. Functional Description

2.1. Theory of Operation

The operation of an Si86S60x channel is analogous to that of an optocoupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si86S60x channel is shown in the figure below.

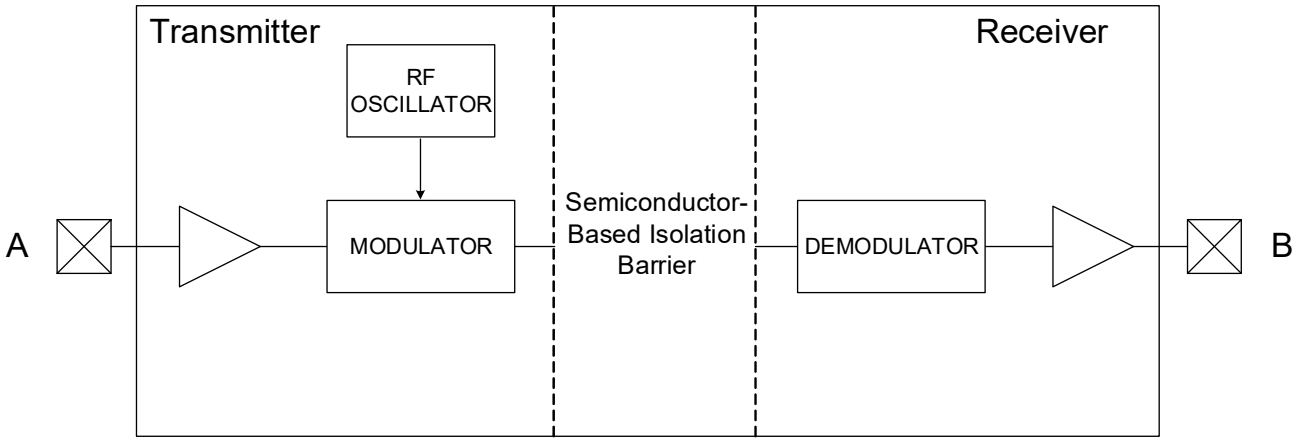

Figure 3. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and improved immunity to magnetic fields. See the following figure for more details.

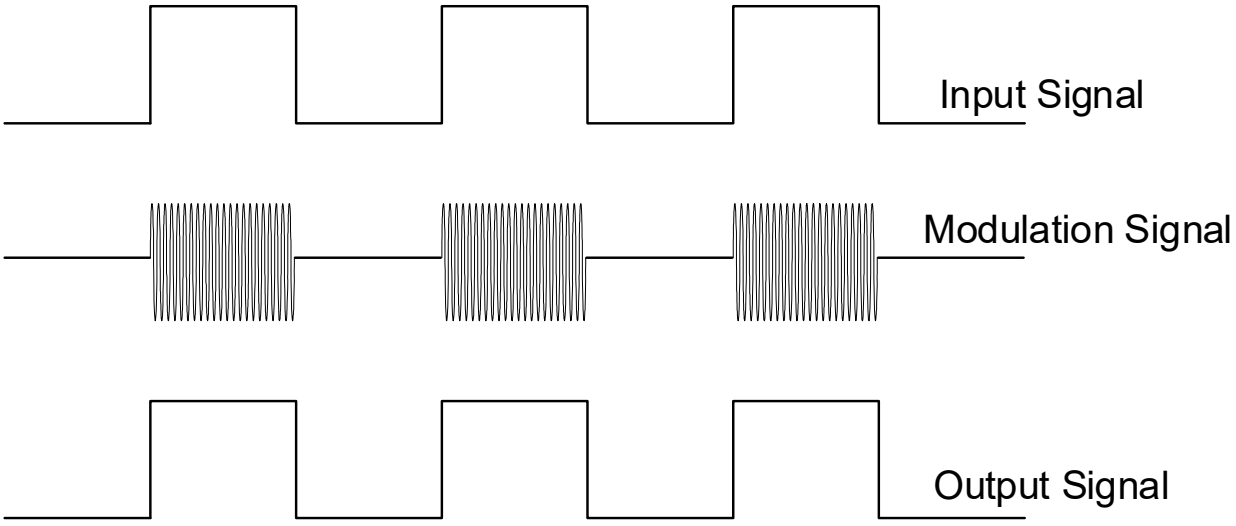

Figure 4. Modulation Scheme

3. Device Operation and System Overview

3.1. Device Startup, UVLO, and Reset Functionality

Outputs are Hi-Z (high impedance) for the I^2C channels and held low for the non-I^2C channels during power up until VDD is above the UVLO threshold for time period t_{START}. Following this, the outputs follow the states of inputs. The start-up time of the device is estimated to be 0.3 ms due to the device initialization time.

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, referring to Figure 5, Side A unconditionally enters UVLO when AVDD falls below UVLO– and exits UVLO when AVDD rises above UVLO+. Side B operates the same as Side A with respect to its BVDD supply.

Along with UVLO, each side has its own self biased circuitry that can detect supply going low enough and issue a complete reset of the part. This is done to avoid loss of device configuration for the particular product option. Referring to the figure below, Side A goes into reset as soon as AVDD goes below RSTB- (~1.7 V) and comes out of reset when AVDD goes above RSTB+. When the supply voltage is above RSTB+ the device configuration is reloaded and all the digital registers are set. Side B operates the same as Side A with respect to its BVDD supply.

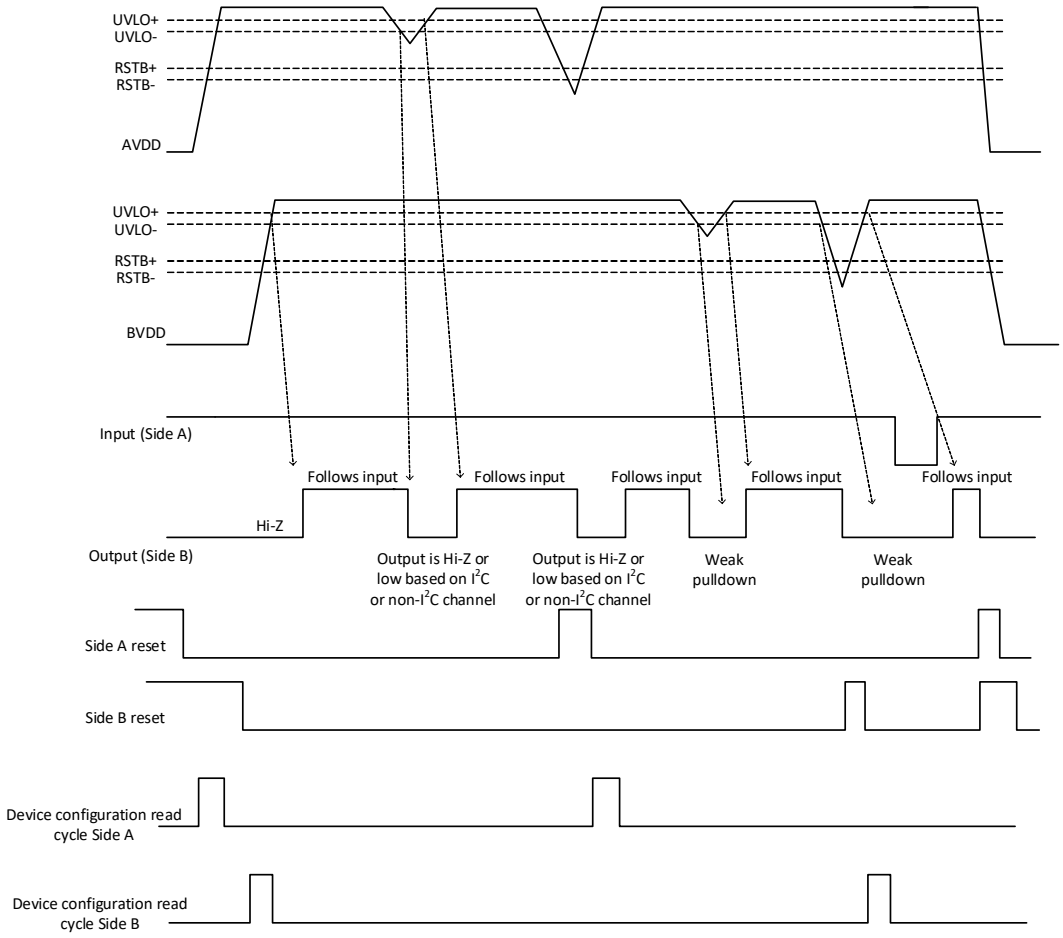

Figure 5. Device Behavior During Startup

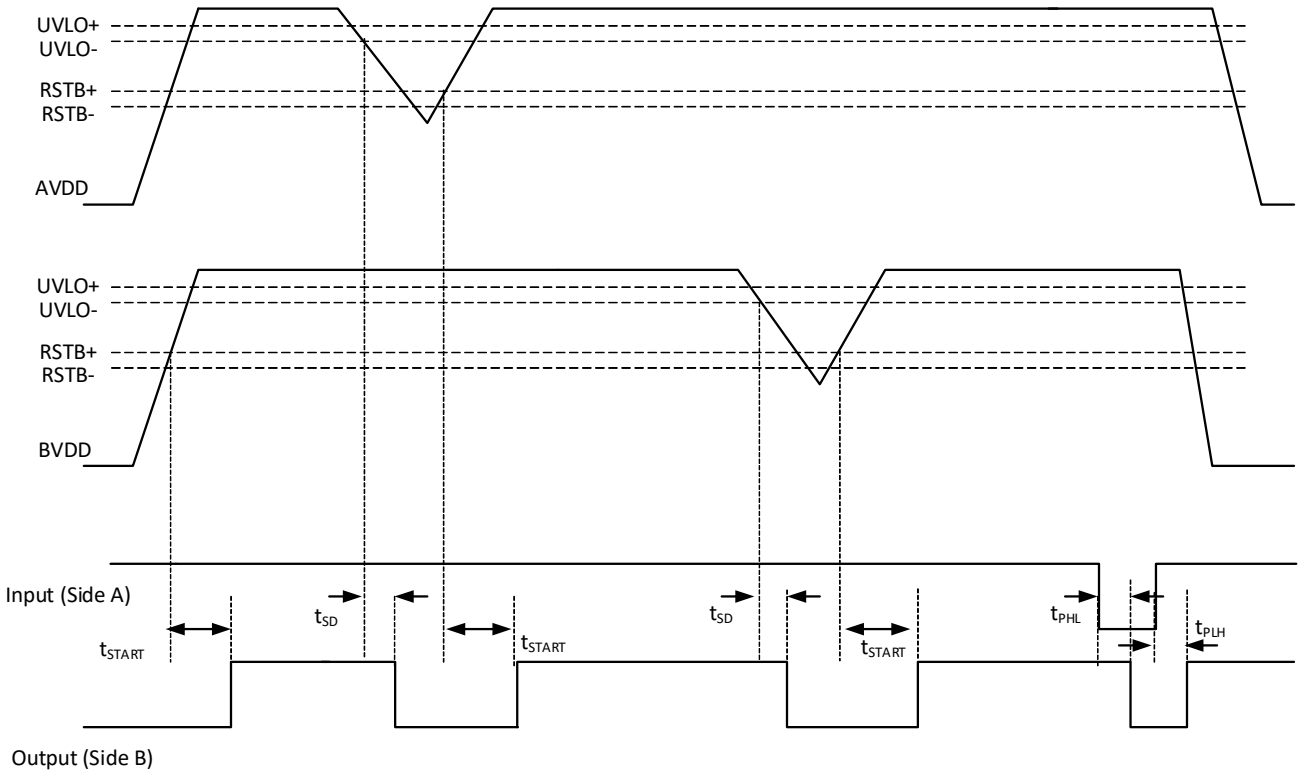

Figure 6. Device Behavior During Normal Operation

3.2. Layout Considerations

To ensure safety in the end-user application, high-voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low-voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 12, “Insulation and Safety-Related Specifications,” on page 19 and Table 14, “IEC 60747-17 Insulation Characteristics for Si86S60x,” on page 20 detail how maintenance of safety data is ensured by protective circuits. This addresses the working voltage and creepage/clearance capabilities of the Si86S60x. These tables also detail the component standards (UL1577, IEC 60747-17), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the following International Electrotechnical Commission (IEC) end-system specifications: 61010-1, 62368-1, 60601-1, etc. requirements before starting any design that uses a digital isolator.

3.2.1. Supply Bypass

The Si86S60x family requires 0.1 and 10 µF bypass capacitors between AVDD, AGND and BVDD, BGND. The capacitors should be placed as close as possible to the respective supply pin to minimize the supply current loop through them. To enhance the robustness of a design, the user may also include resistors (50 to 300Ω) in series with the inputs and outputs if the system is excessively noisy. Note that adding the resistors will change the default pull-up strength of the bus on the device output.

3.2.2. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.

3.3. Typical Application Overview

3.3.1. I^2C Background

In many applications, I^2C, SMBus, and other digital power supply communications, including those for bus power management, the interfaces require galvanic isolation for safety or ground loop elimination. For example, Power over Ethernet (PoE) applications typically use an I^2C interface for communication between the PoE power sourcing device (PSE), and the earth ground referenced system controller. Galvanic isolation is required both by standard and also as a practical matter to prevent ground loops in Ethernet connected equipment.

The physical interface consists of two wires: serial data (SDA) and serial clock (SCL). These wires are connected to open drain drivers that serve as both inputs and outputs. At first glance, it appears that SDA and SCL can be isolated simply by placing two unidirectional isolators in parallel, and in opposite directions. However, this technique creates feedback that latches the bus line low when a logic low is asserted by either side. This problem can be remedied by adding anti-latch circuits, but results in a larger and more expensive solution. The Si86S60x products offer a single-chip, anti-latch solution to the problem of isolating I^2C/SMBus applications and require no external components. In addition, they provide isolation to a maximum of 6.0 kV_{RMS}, support I^2C clock stretching, and operate to a maximum I^2C bus speed of 1.7 Mbps.

3.3.2. I²C Isolator Operation

Without anti-latch protection, bidirectional I²C isolators latch when an isolator output logic low propagates back through an adjacent isolator channel creating a stable latched low condition on both sides. Anti-latch protection is typically added to one side of the isolator to avoid this condition (the "A" side for the Si86S60x).

The following examples illustrate typical circuit configurations using the Si86S60x.

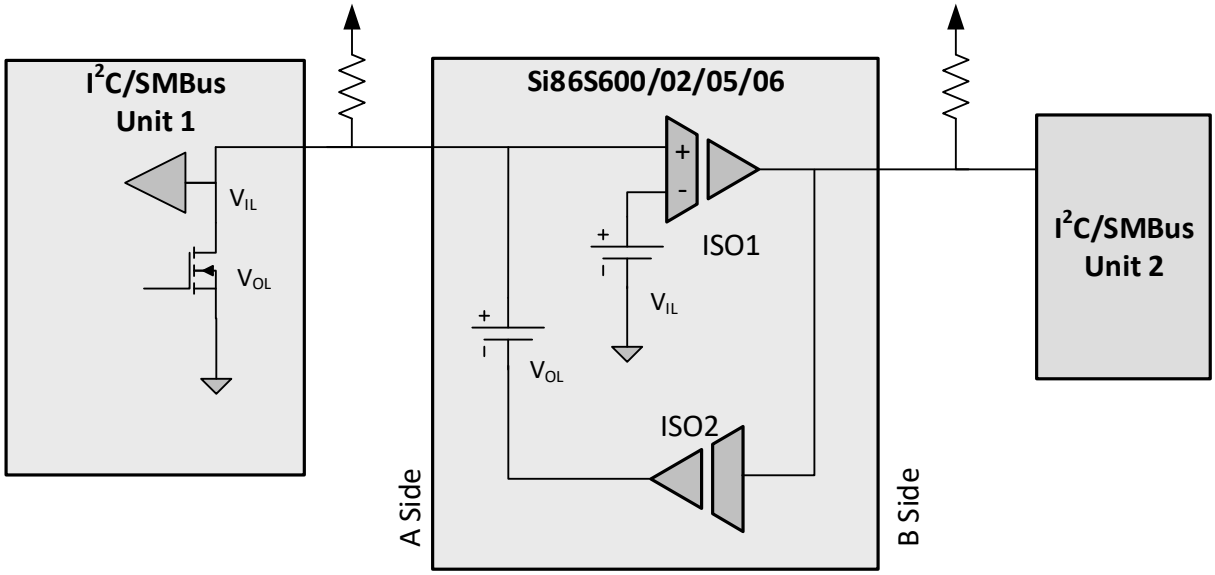

Figure 7. Isolated Bus Overview (I²C Channels Only)

The "A side" output low (V_{OL}) and input low (V_{IL}) levels are designed such that the isolator V_{OL} is greater than the isolator V_{IL} to prevent the latch condition.

3.3.3. I²C Isolator Design Constraints

The table below lists the I²C isolator design constraints for Side A.

Table 3. Design Constraints for Side A

Design Constraint	Data Sheet Values	Effect of Bus Pull-up Strength and Temperature
To prevent the latch condition, the isolator output low level must be greater than the isolator input low level by at least 50 mV.	Isolator V_{OL} 0.7 V typical Isolator V_{IL} 0.5 V typical Input/Output Logic Low Level Difference	This is normally guaranteed by the isolator data sheet. However, if the pull up strength is too weak, the output low voltage will fall and can get too close to the input low logic level. These track over temperature.
The bus output low must be less than the isolator input low logic level.	Bus V_{OL} = 0.4 V maximum Isolator V_{IL} = 0.41 V minimum	If the pull up strength is too large, the devices on the bus might not pull the voltage below the input low range. These have opposite temperature coefficients. Worst case is hot temperature.
The isolator output low must be less than the bus input low.	Bus V_{IL} 0.3 x V_{DD} = 1.0 V minimum for V_{DD}= 3.3 V Isolator V_{OL} = 0.8 V maximum	If the pull up strength is too large, the isolator might not pull below the bus input low voltage. Si86S60x V_{OL}: –1.8 mV/C CMOS buffer: –0.6 mV/C This provides some temperature tracking, but worst case is cold temperature.

3.3.4. I²C Isolator Design Considerations

These considerations will help to determine which side of the bus should be connected to the isolator A side. Ideally, it should be the side which:

- Is compatible with the range of bus pull up specified by the manufacturer. For example, the Si86S60x isolators are normally used with a pull up of 0.5 mA to 3 mA.
- Has the highest input low level for devices on the bus. Some devices may specify an input low of 0.9 V and other devices might require an input low of 0.3 x Vdd. Assuming a 3.3 V minimum power supply, the side with an input low of 0.3 x Vdd is the better side because this side has an input low level of 1.0 V.
- Has devices on the bus that can pull down below the isolator input low level. For example, the Si86S60x input level is 0.41 V. As most CMOS devices can pull to within 0.4 V of GND this is generally not an issue.
- Has the lowest noise. Due to the special logic levels, noise margins can be as low as 50 mV.
- Since Side A has lower noise margin and lower noise immunity, please try to avoid using Side A to connect multiple Si86S60x devices on the same bus.

3.3.5. Typical Application Schematics

The figures below illustrate typical circuit configurations using the Si86S600, Si86S602, Si86S605, and Si86S606.

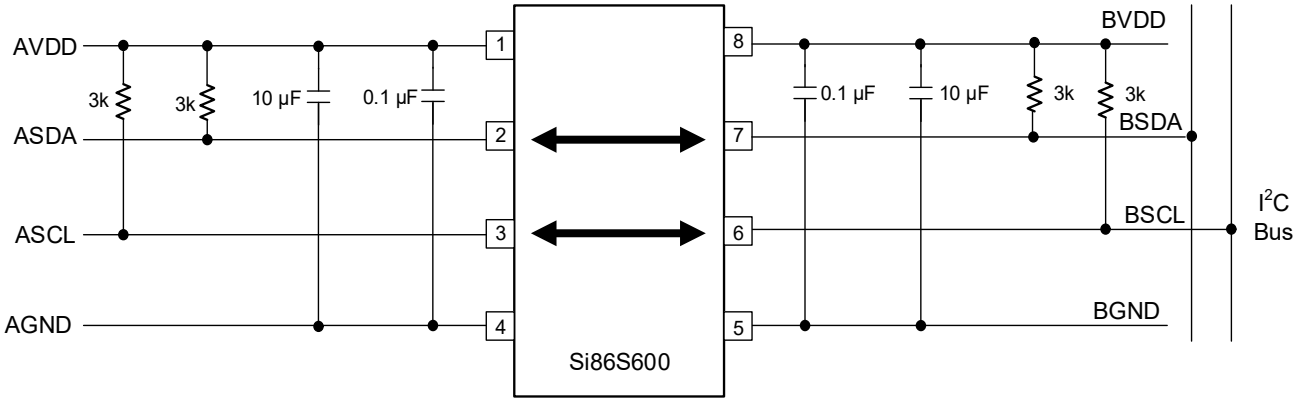

Figure 8. Typical Si86S600 Application Diagram

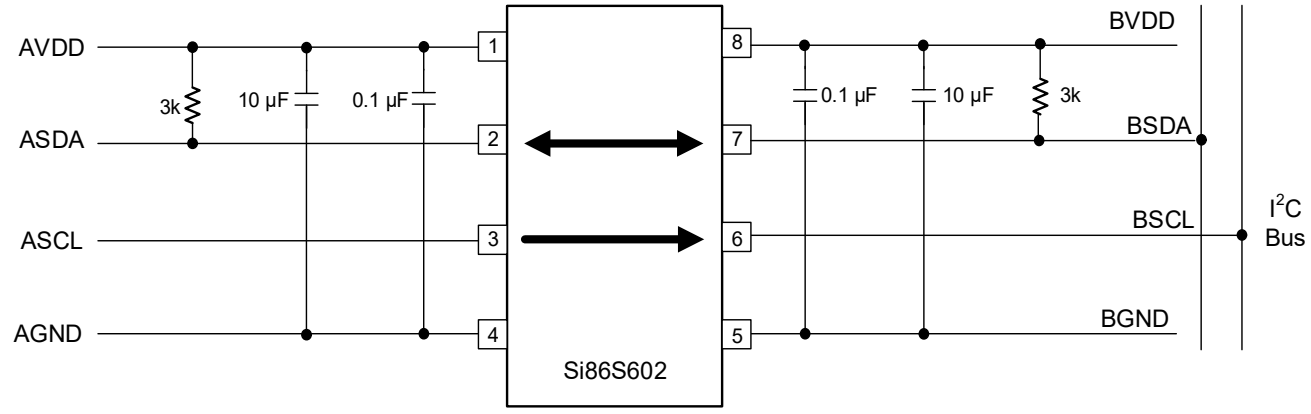

Figure 9. Typical Si86S602 Application Diagram

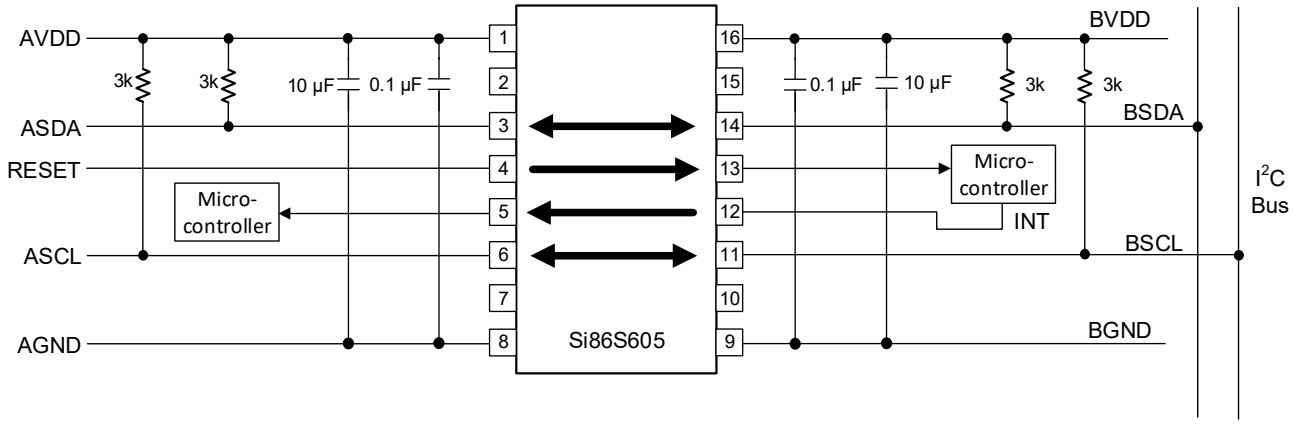

Figure 10. Typical Si86S605 Application Diagram

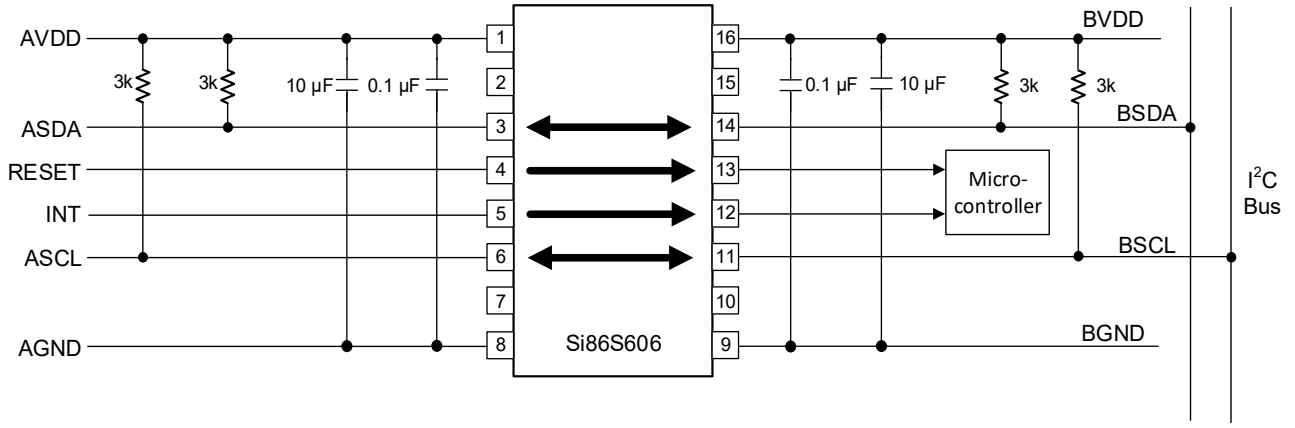

Figure 11. Typical Si86S606 Application Diagram

3.4. Input and Output Characteristics for Non-I²C Digital Channels

The unidirectional Si86S60x inputs and outputs are standard CMOS drivers/receivers, including the ASCL input and BSCL output on the Si86S602 options. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. The following table details powered and unpowered operation of the Si86S60x's non-I²C digital channels.

Table 4. Si86S60x Operation Table

VI Input[1,2,3]	VDDI State[1,4,5]	VDDO State[1,4,5]	VO Output[1,2,3]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X	UP	P	L	Upon transition of VDDI from unpowered to powered, VO returns to the same state as VI in less than 1 µs.
X	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, VO returns to the correct state within 0.3 ms.[6]

1. VDDI and VDDO are the input and output power supplies. VI and VO are the respective input and output terminals.
2. X = not applicable; H = Logic High; L = Logic Low.
3. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
4. Powered (P) state is defined as 3.0 V < VDD < 5.5 V.
5. Unpowered (UP) state is defined as VDD = 0 V.
6. Refer to Figure 5, "Device Behavior During Startup," on page 5. This shows the start-up time from unpowered state, below 1.7 V (RSTB) threshold to powered state, is 0.3 ms. If VDDO only dips below 2.1 V (VDDOK level in diagram below) but stays above RSTB level, the start-up time is 1 us.

4. Electrical Specifications

Table 5. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	–65	150	°C
Operating temperature	T_A	–40	125	°C
Junction temperature	T_J	—	150	°C
Supply voltage	AVDD, BVDD	–0.5	7.0	V
Supply voltage ramp-up	AVDD, BVDD	—	1	V/µs
Input voltage	V_I	–0.5	VDD + 0.5	V
Output voltage	V_O	–0.5	VDD + 0.5	V
Output current drive (non-I^2C channels)	I_O	–10	+10	mA
Side A output current drive (I^2C channels)	I_O	–15	+15	mA
Side B output current drive (I^2C channels)	I_O	–75	+75	mA
ESD	HBM	—	8	kV
	CDM	—	2	kV
	IEC 61000-4-2 contact discharge[2]	—	8000	V
Lead solder temperature (10s)		—	260	°C

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.
2. Test is performed across the isolation barrier with device in a two terminal configuration, with pins on each side shorted together. Tested per IEC 61000-4-2 contact discharge.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 6. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Junction operating temperature	T_J	—	—	150	°C
Ambient operating temperature	T_A	–40	25	125	°C

Table 7. Si86S60x Power Characteristics

3.0 V < VDD < 5.5 V. T_A = –40 to +125 °C. Typical specs at 25 °C and 5.0 V VDD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S600 Supply Current						
AVDD current BVDD current	AIDD BIDD	All channels = 0 dc	— —	4.4 3.3	5.1 4.0	mA
AVDD current BVDD current	AIDD BIDD	All channels = 1 dc	— —	2.8 2.0	3.4 2.5	
AVDD current BVDD current	AIDD BIDD	All channels = 1.7 MHz	— —	3.6 2.7	4.3 3.4	
Si86S602 Supply Current						
AVDD current BVDD current	AIDD BIDD	All channels = 0 dc	— —	3.6 2.6	4.3 3.2	mA
AVDD current BVDD current	AIDD BIDD	All channels = 1 dc	— —	2.1 1.9	2.6 2.5	
AVDD current BVDD current	AIDD BIDD	All channels = 1.7 MHz	— —	2.9 2.3	3.4 2.9	
Si86S605 Supply Current						
AVDD current BVDD current	AIDD BIDD	All non-I^2C channels = 0 All I^2C channels = 1	— —	3.6 2.8	4.5 3.7	mA
AVDD current BVDD current	AIDD BIDD	All non-I^2C channels = 1 All I^2C channels = 0	— —	5.8 4.7	7.4 6.2	
AVDD current BVDD current	AIDD BIDD	All non-I^2C channels = 0.5 MHz All I^2C channels = 1.7 MHz	— —	4.7 3.8	5.9 4.9	
Si86S606 Supply Current						
AVDD current BVDD current	AIDD BIDD	All non-I^2C channels = 0 All I^2C channels = 1	— —	3.0 3.2	3.8 4.2	mA
AVDD current BVDD current	AIDD BIDD	All non-I^2C channels = 1 All I^2C channels = 0	— —	5.8 4.7	7.1 5.8	
AVDD current BVDD current	AIDD BIDD	All non-I^2C channels = 0.5 MHz All I^2C channels = 1.7 MHz	— —	4.5 3.9	5.4 5.1	

Table 8. Si86S60x Electrical Characteristics for Bidirectional I²C Channels
3.0V < VDD < 5.5 V. T_A = –40 to +125 °C. Typical specs at 25 °C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Logic levels side A Logic input threshold[1] Logic low output voltages Input/output logic low level difference[2]	 I2CV$_{IL}$ (Side A) I2CV$_{OL}$ (Side A) I2CΔV (Side A)	 IASDA, IASCL (>0.5 mA, <3.0 mA)	 390 580 60	 — — —	 580 730 —	mV
Logic levels side B Logic low input voltage Logic high input voltage Logic low output voltage	 I2CV$_{IL}$ (Side B) I2CV$_{IH}$ (Side B) I2CV$_{OL}$ (Side B)	 IBSCL = 35 mA	 — 0.7*BVDD —	 — — —	 0.3*BVDD — 0.5	V
SCL and SDA logic high leakage	IASDA, IBSDA IASCL, IBSCL	ASDA, ASCL = AVDD BSDA, BSCL = BVDD	—	4.0	7.0	µA
Pin capacitance ASDA, BSDA, ASCL, BSCL	CA CB		— —	10 10	— —	pF
Timing Specifications						
Maximum I²C bus frequency	Fmax		—	—	1.7	MHz
Propagation delay 5 V Operation Side A to side B rising[3] Side A to side B falling Side B to side A rising Side B to side A falling 3.3 V Operation Side A to side B rising Side A to side B falling Side B to side A rising Side B to side A falling	 t_{PHAB} t_{PLAB} t_{PHBA} t_{PLBA} t_{PHAB} t_{PLAB} t_{PHBA} t_{PLBA}	No bus capacitance See Figure 14 on page 18 R1 = 1400 Ω R1 = 1400 Ω R2 = 499 Ω R2 = 499 Ω R1 = 806 Ω R1 = 806 Ω R2 = 499 Ω R2 = 499 Ω	 — — — — — — — —	 23.0 15.0 44.5 13.0 26.0 15.5 30.5 17.0	 29.0 19.5 53.5 18.5 34.0 22.5 38.0 28.0	ns
Pulse width distortion PWD = |tPHAB – tPLAB| and |tPHBA – tPLBA| 5 V Operation Side A low to side B low[4] Side B low to side A low 3.3 V operation Side A low to side B low[4] Side B low to side A low	 PWDAB PWDBA PWDAB PWDBA	No bus capacitance See Figure 12 on page 16 R1 = 1400 Ω R2 = 499 Ω R1 = 806 Ω R2 = 499 Ω	 — — — —	 8.0 32.0 10.0 14.0	 11.0 36 14.0 17	ns

1. V_{IL} < 0.410 V, V_{IH} > 0.540 V.
2. I2CΔV (Side A) = I2CV$_{OL}$ (Side A) – I2CVT (Side A). To ensure no latch-up on a given bus, I2CΔV (Side A) is the minimum difference between the output logic low level of the driving device and the input logic threshold.
3. Side A measured at 0.6 V.

Table 9. Electrical Characteristics for Unidirectional Non-I²C Digital Channels (Si86S602/05/06)

3.0 V < VDD < 5.5 V. T_A = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input hysteresis	VHYS		0.1*xVDD	—	—	V
High level input voltage	V_{IH}		0.7*xVDD	—	—	V
Low level input voltage	V_{IL}		—	—	0.3*xVDD	V
High level output voltage	V_{OH}	Ioh = –4 mA	AVDD, BVDD –0.4	—	—	V
Low level output voltage	V_{OL}	Iol = 4 mA	—	—	0.4	V
Input leakage current	I_L		-10	—	+10	µA
Output impedance	Z_O		—	50	—	Ω
Timing Characteristics						
Maximum data rate			0	—	150	Mbps
Minimum pulse width		Minimum pulse width guaranteed to be transmitted to the output.	6.7	—	—	ns
Propagation delay	t_{PHL}, t_{PLH}	See Figure 12 on page 16 and Figure 14 on page 18	6	10	15	ns
Pulse width distortion |tPLH – tPHL|	PWD	See Figure 12 on page 16 and Figure 14 on page 18	—	—	3	ns
Propagation delay skew[1]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew	t_{PSK}		—	1.5	4	ns
Output rise time	t_r	C3 = 15 pF See Figure 12 on page 16 and Figure 14 on page 18	—	2.5	—	ns
Output fall time	t_f	C3 = 15 pF See Figure 12 on page 16 and Figure 14 on page 18	—	2.5	—	ns
Peak eye diagram jitter	$t_{JIT(PK)}$		—	350	—	ps

1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

Table 10. Electrical Characteristics for All I²C and Non-I²C Channels

3.0 V < VDD < 5.5 V. T_A = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD undervoltage threshold	VDDUV+	VDD1, VDD2 rising	2.10	2.18	2.25	V
VDD undervoltage threshold	VDDUV–	VDD1, VDD2 falling	1.98	2.05	2.12	V
VDD undervoltage hysteresis	VDDHYS		105	131	160	mV
Common mode transient immunity	CMTI	VI = VDD or 0 V VCM = 1500 V (See Figure 13 on page 17)	100	—	—	kV/µs
Input power loss to valid default output	t_{SD}	See Figure 6 on page 6	—	8	12	ns
Start-up time[1]	t_{START}	See Figure 6 on page 6	—	—	300	µs

1. Start-up time is the time period from the application of power to valid data at the output.

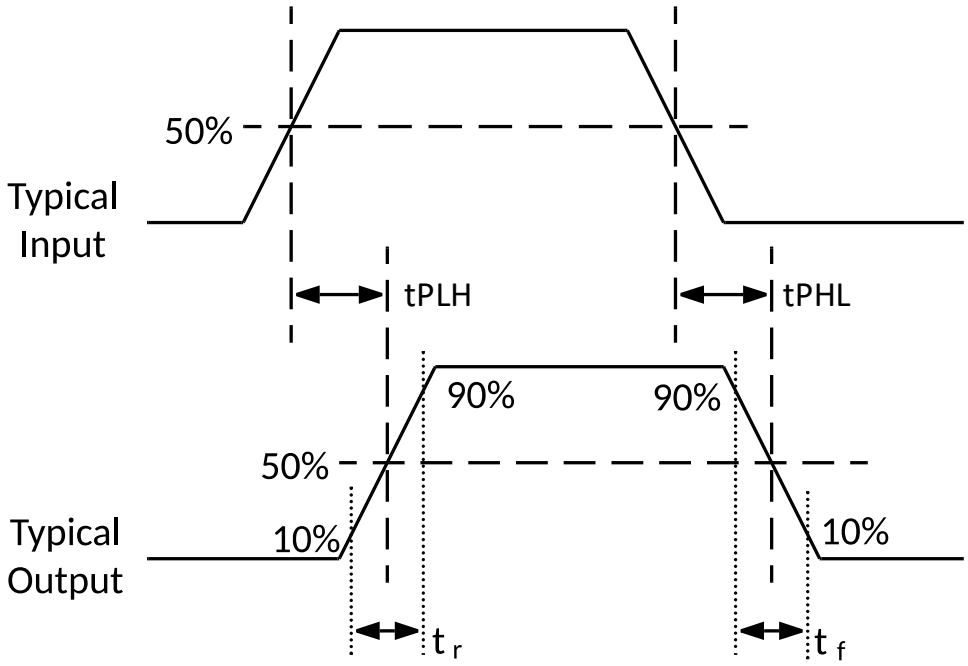

Figure 12. Propagation Delay Timing for Uni-Directional Channels

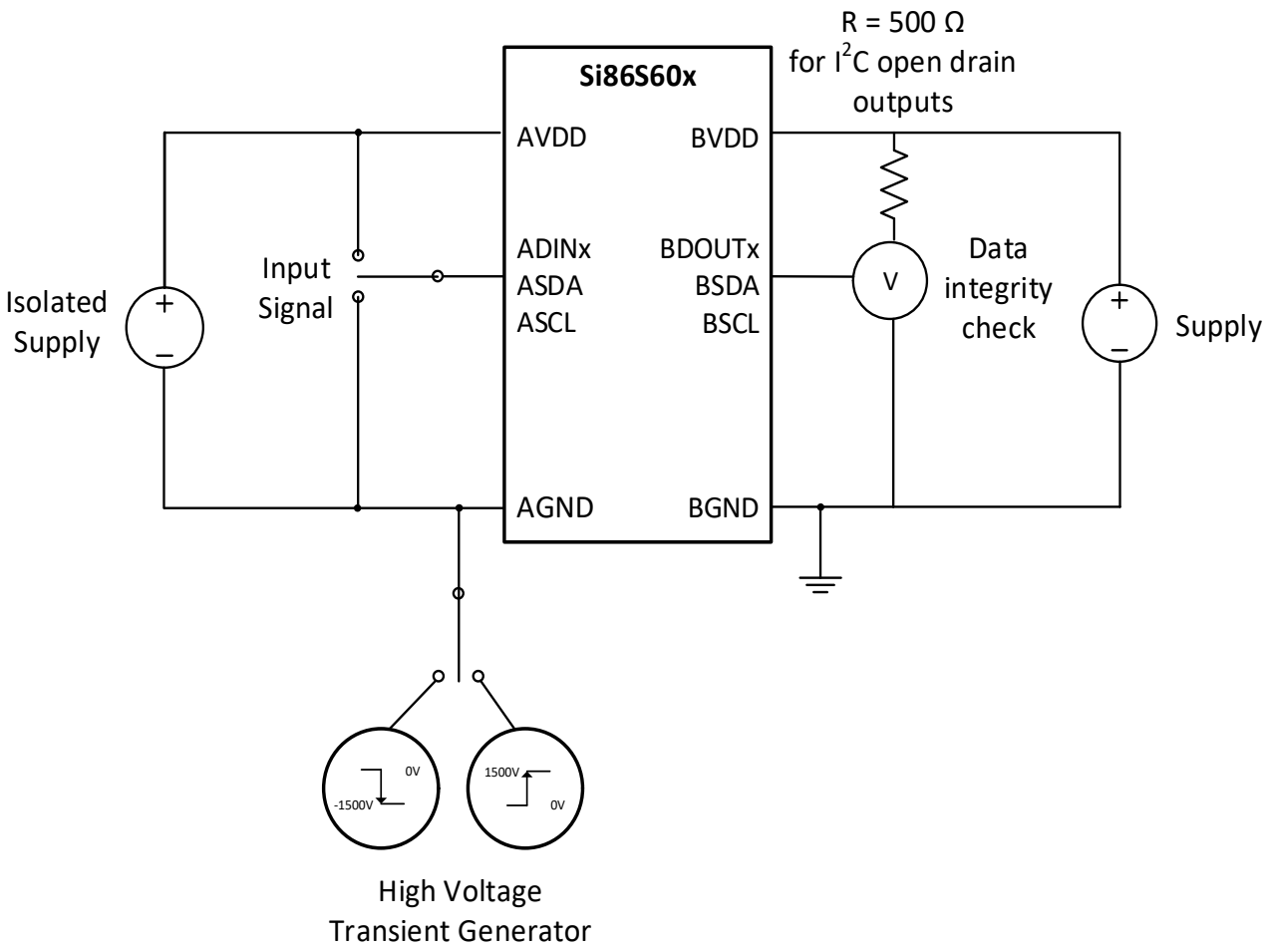

Figure 13. Common-Mode Transient Immunity Test Diagram

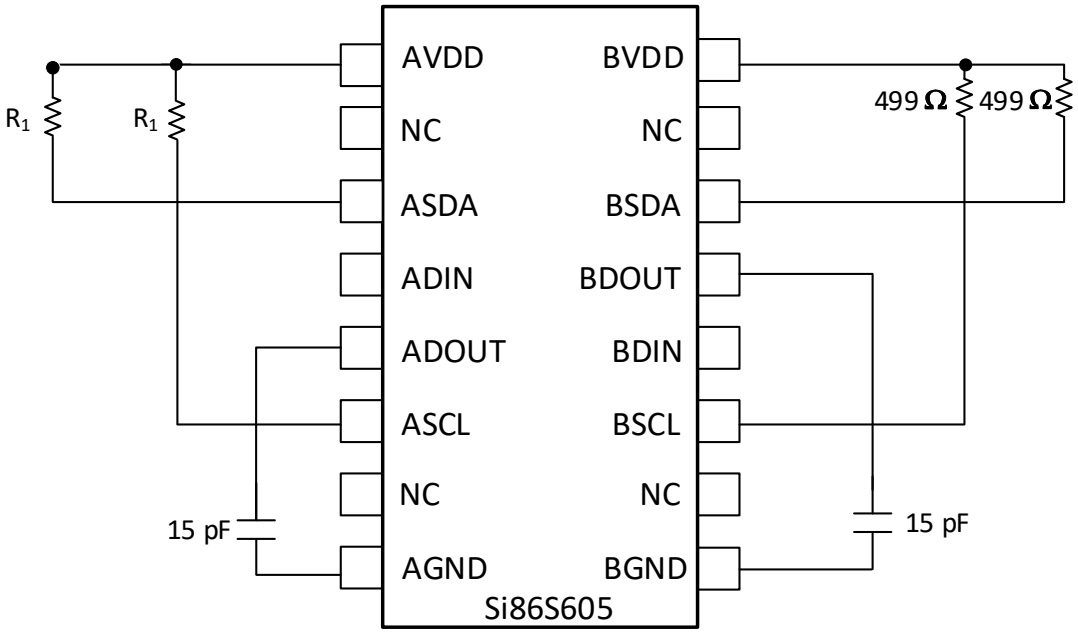

Figure 14. Simplified Timing Test Diagram

5. Safety Certifications and Specifications

Table 11. Regulatory Information (Pending)[1]

CSA
The Si86S60x is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} working voltage and 2 MOPP (Means of Patient Protection).
VDE
The Si86S60x is certified under VDE. For more details, see File 5028467.
60747-17: Up to 2121 Vpeak for reinforced insulation working voltage.
UL
The Si86S60x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si86S60x is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see Ordering Information.

Table 12. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value				Unit
			WB SOIC-16	QSOP-16	SSO-8	NB SOIC-8	
Nominal external air gap (clearance)	CLR		8.0	3.6	8.0	3.9	mm
Nominal external tracking (creepage)	CRP		8.0	3.6	8.0	3.9	mm
Minimum internal gap (internal clearance)	DTI		0.036	0.036	0.036	0.036	mm
Tracking resistance	CTI or PTI	IEC60112	600	600	600	600	V_{RMS}
Erosion depth	ED		0.019	0.031	0.019	0.04	mm
Resistance (input-output) [1]	R_{IO}	Test voltage = 500 V, 25 °C	10^{12}	10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	2.0	2.0	1.0	1.0	pF
Input capacitance[2]	C_I		4.0	4.0	4.0	4.0	pF

1. To determine resistance and capacitance, the Si86Sx is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 13. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification			
		WB SOIC-16	QSOP-16	SSO-8	NB SOIC-8
Material group		I	I	I	I
Overvoltage category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV	I-IV	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-III	I-IV	I-III
	Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-II	I-IV	I-II
	Rated mains voltage ≤ 1000 V_{RMS}	I-III	I	I-III	I

Table 14. IEC 60747-17 Insulation Characteristics for Si86S60x [1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16/ SSO-8	NB SOIC-8/ QSOP-16	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	1500	445	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	2121	630	V_{peak}
Apparent charge	q_{pd}	Method b: At routine test (100% production) and precon-ditioning (type test); V_{ini} = 1.2 x V_{IOTM}, tini = 1 s; $V_{pd(m)}$ = 1.875 x V_{IORM}, tm = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, tm = tini (method b2)	≤5	≤5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	8484	5302/3535	V_{peak}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile	10400	10400	V_{peak}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile	8000	5000	V_{peak}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 15. UL 1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16/ SSO-8	NB SOIC-8/ QSOP-16	
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	6000	3750/2500	V_{RMS}

Table 16. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max				Unit
			WB SOIC-16	QSOP-16	SSO-8	NB SOIC-8	
Safety temperature	T_S		150	150	150	150	°C
Safety input, output, or supply current	I_S	Refer to θ_{JA} in Table 17, Thermal Characteristics. V_{DD} = 5.5 V, T_J = 150 °C, T_A = 25 °C	345	311	253	221	mA
Safety input, output, or total power	P_S		1894	1712	1389	1214	mW

1. Maximum value allowed in the event of a failure; also see the thermal derating curves in Figure 15 on page 21, Figure 16 on page 21, Figure 17 on page 21, and Figure 18 on page 21.

Table 17. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	QSOP-16	SSO-8	NB SOIC-8	Unit
IC junction-to-air thermal resistance	θ_{JA}	66	73	90	103	°C/W
IC junction-to-board thermal resistance	θ_{JB}	35	43	47	45	
IC junction-to-case thermal resistance	θ_{JC}	24	31	27	26	
Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board	Ψ_{JB}	33	43	43	42	

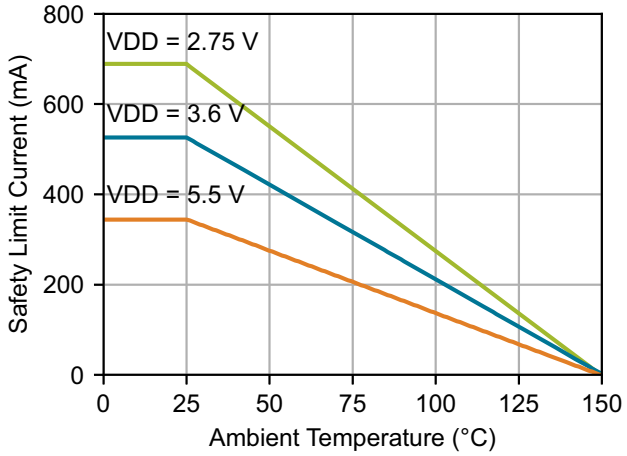

Figure 15. WB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Current

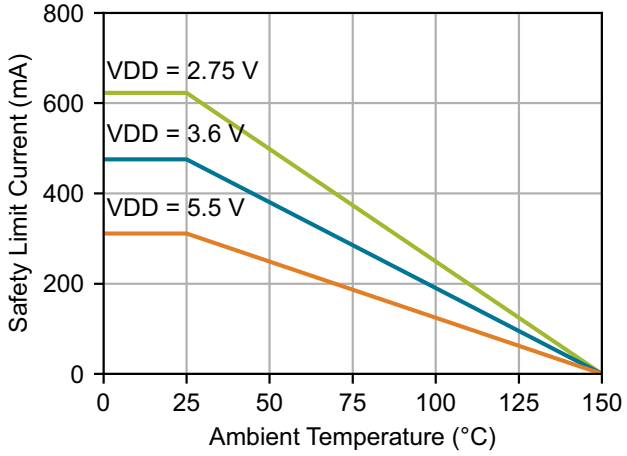

Figure 16. QSOP-16 Thermal Derating Curve, Dependence of Safety Limiting Current

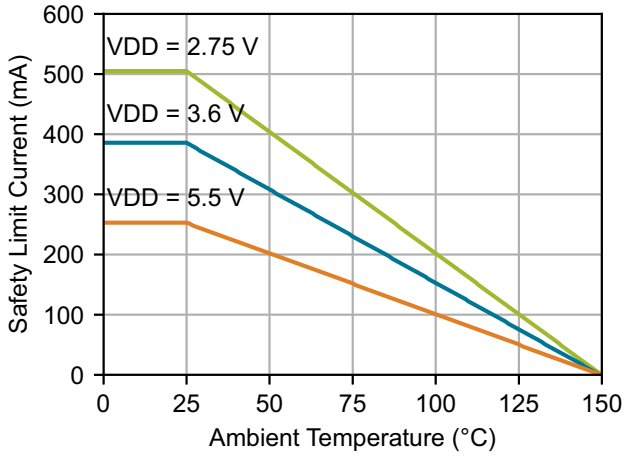

Figure 17. SSO-8 Thermal Derating Curve, Dependence of Safety Limiting Current

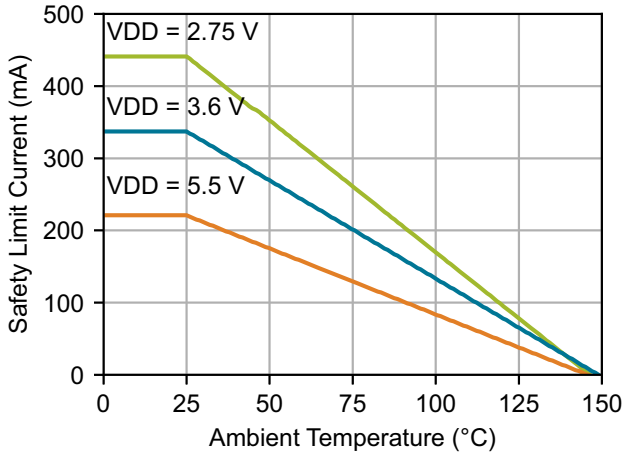

Figure 18. NB SOIC-8 Thermal Derating Curve, Dependence of Safety Limiting Current

6. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to the tables in Section 4. Electrical Specifications for more information.

Note that, for Figure 19, because of the closed-feedback loop anti-latch protection scheme, the Side A bus is driven by the isolator Side A output driver to stay at V_{OL} level for two periods of channel propagation delay when the controller on Side A bus releases the bus. The bump in Figure 19 illustrates the transition process. The I^2C bus is at a low state, and both Side A and B outputs of the isolator are low. When the controller on Side A releases the bus by outputting Hi-Z, the Side A bus is held by the isolator Side A output driver to be at V_{OL} level, which is greater than the input threshold V_{IL} level by design. This triggers the Side B output driver to release the Side B bus after a propagation delay, which, in turn, triggers the Side A output driver to release the Side A bus by another propagation delay. After that, the Side A bus will be pulled up to AVDD level by the external pull-up resistor.

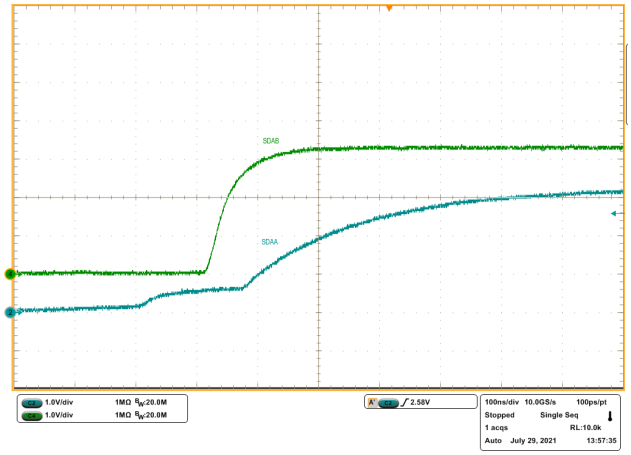

Figure 19. I^2C Side A Pulling Up

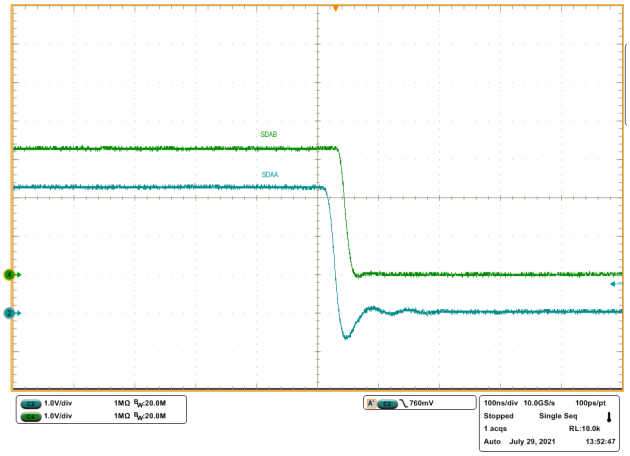

Figure 20. I^2C Side A Pulling Down

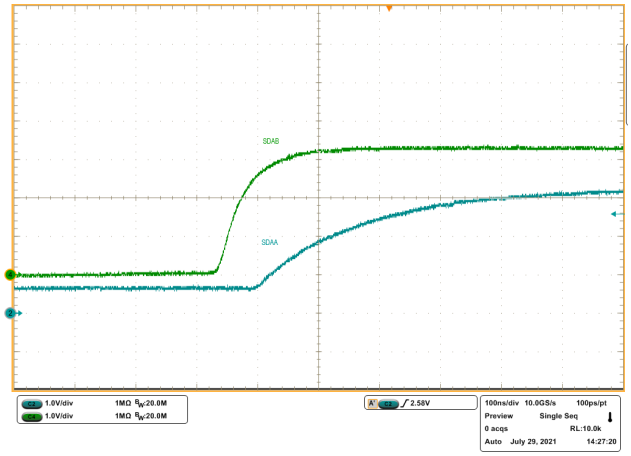

Figure 21. I^2C Side B Pulling Up

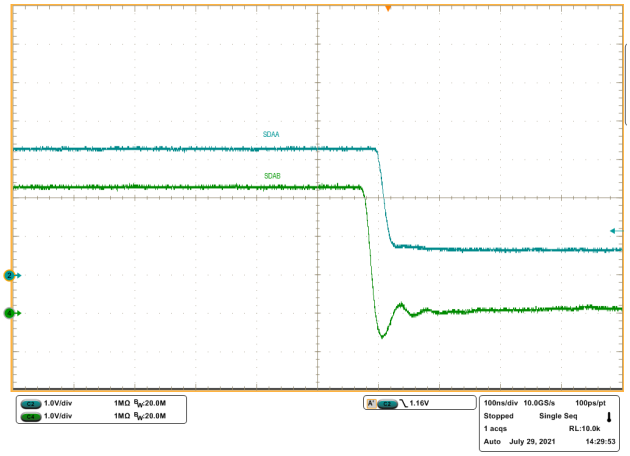

Figure 22. I^2C Side B Pulling Down

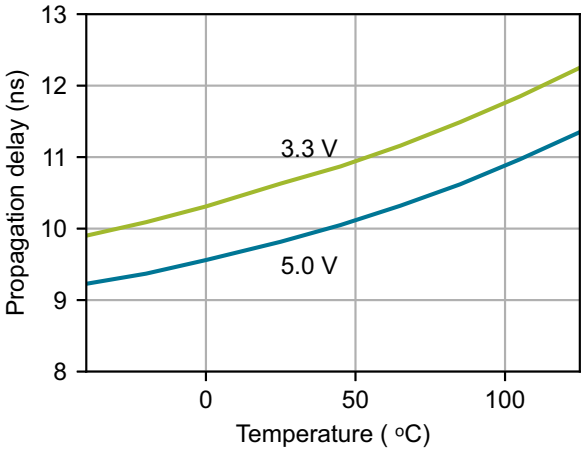

Figure 23. Non-I²C Channel Propagation Delay vs. Temperature

7. Package Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly. The Si86S60x are rated to Moisture Sensitivity Level 2 (MSL2) at 260 °C for all packages except SSO-8 and WB SOIC-16, which are rated to Moisture Sensitivity Level 2A (MSL2A) at 260 °C. They can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, “PCB Design and SMT Assembly/Rework Guidelines,” Document Number 101752. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: JEDEC Standard J-STD-020.

8. Package Outline

8.1. Package Outline (WB SOIC-16)

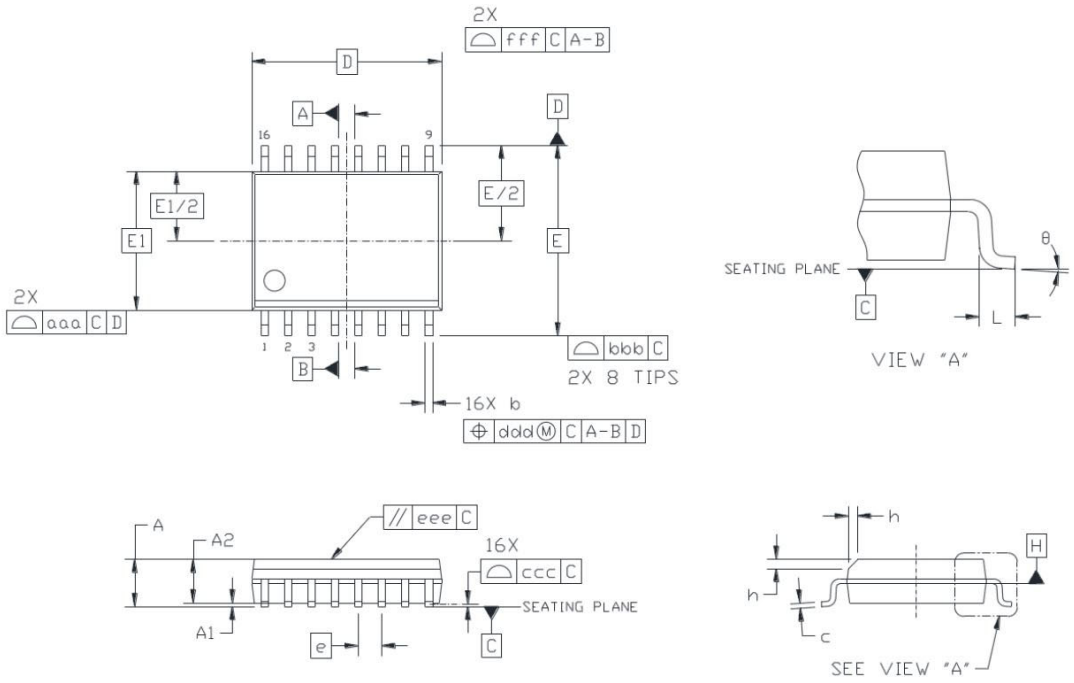

Figure 24. WB SOIC-16

Table 18. WB SOIC-16 Package Diagram Dimensions[1,2,3,4]

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

8.2. Package Outline (QSOP-16)

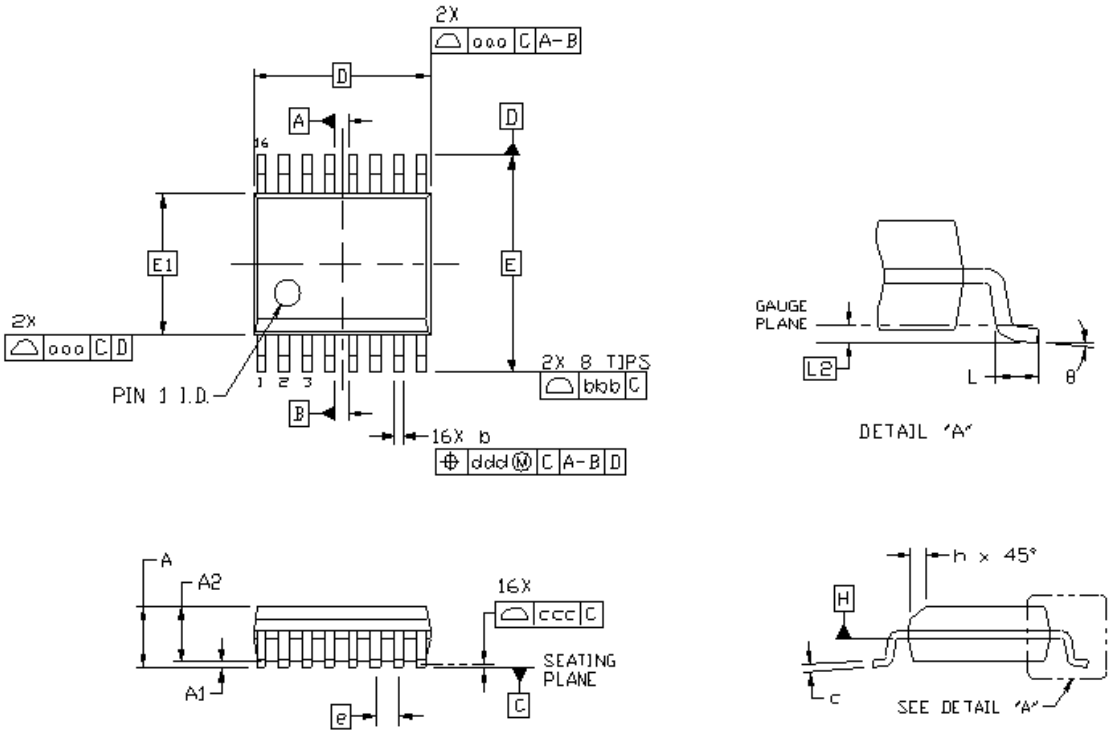

Figure 25. QSOP-16

Table 19. QSOP-16 Package Diagram Dimensions[1, 2, 3, 4]

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	4.89 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3. Package Outline (SSO-8)

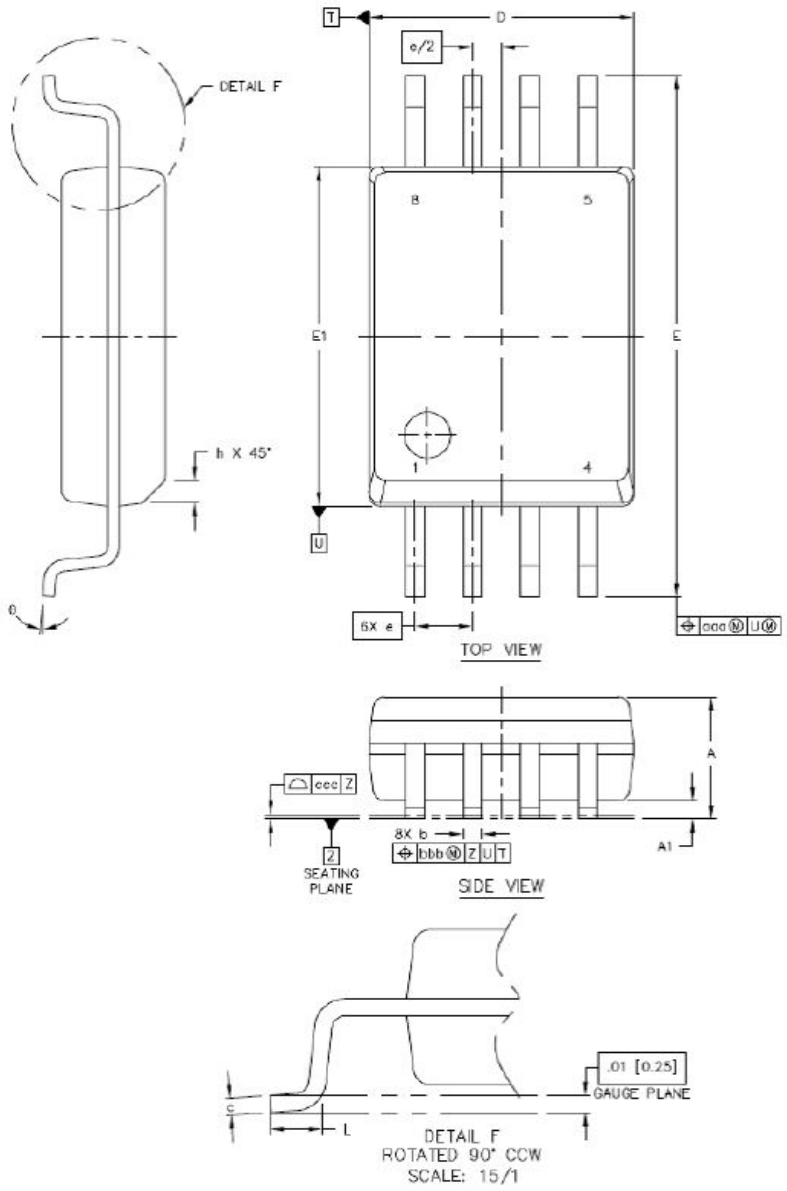

Figure 26. SSO-8 Package

Table 20. SSO-8 Package Diagram Dimensions[1, 2, 3]

Dimension	MIN	MAX
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.20	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
h	0.25	0.76
θ	0°	8°
aaa	--	0.25
bbb	--	0.25
ccc	--	0.10

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

8.4. Package Outline (NB SOIC-8)

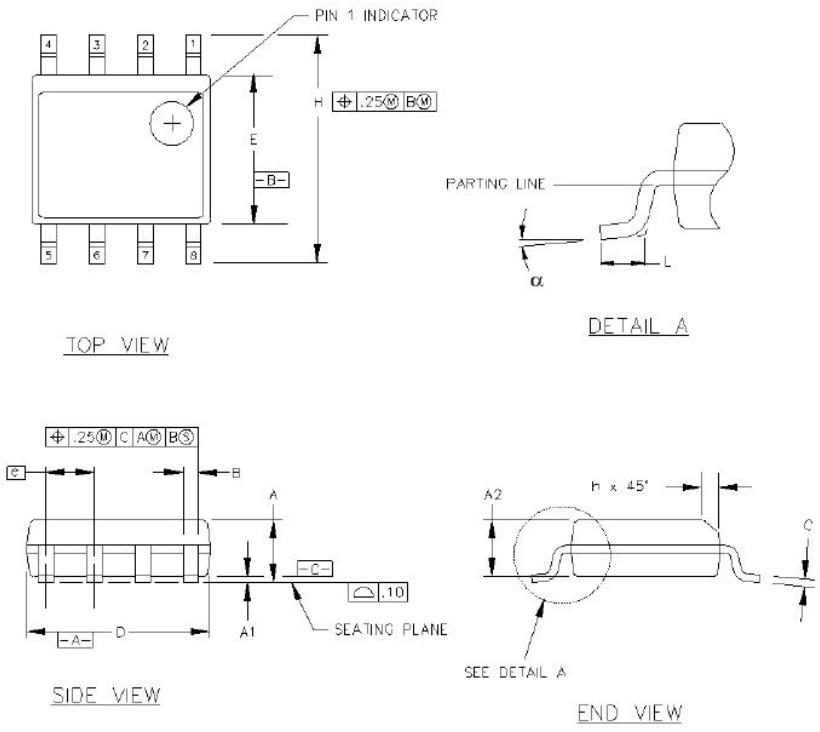

Figure 27. NB SOIC-8 Package

Table 21. NB SOIC-8 Package Diagram Dimensions[1, 2, 3, 4]

Dimension	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. This drawing conforms to JEDEC Outline MS-102.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for Small Body Components.

9. Land Pattern

9.1. Land Pattern (WB SOIC-16)

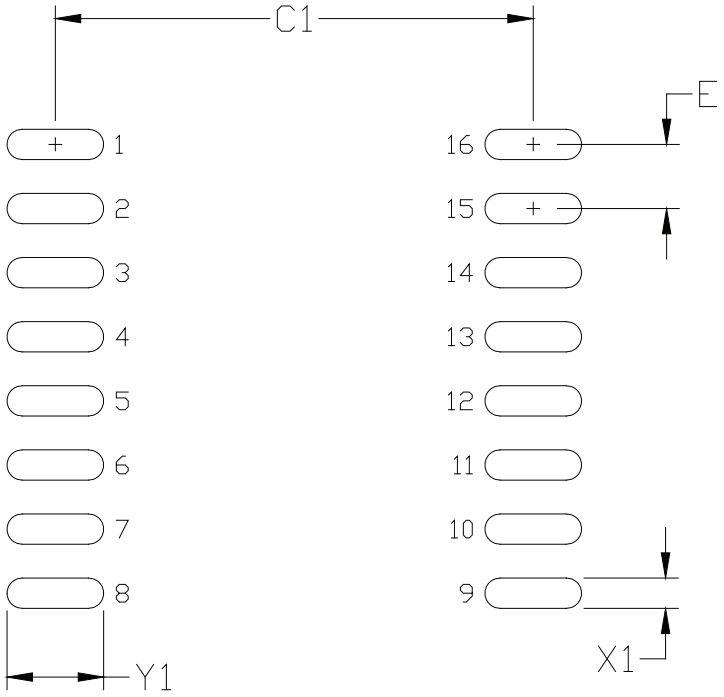

Figure 28. WB SOIC-16 PCB Land Pattern

Table 22. WB SOIC-16 Land Pattern Dimensions[1, 2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.80
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9.2. Land Pattern (QSOP-16)

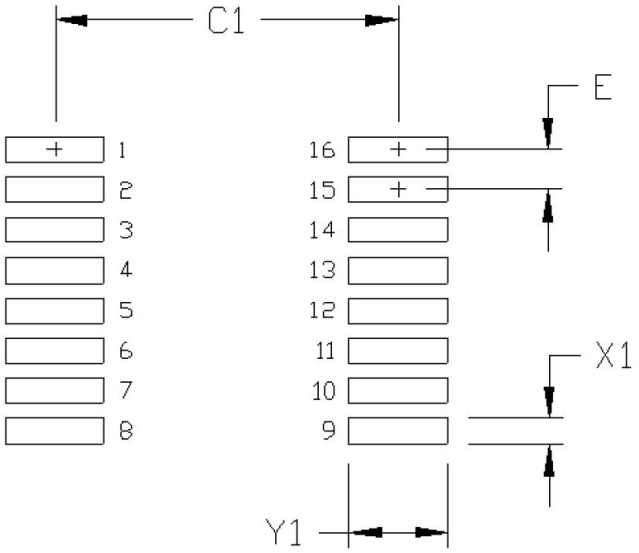

Figure 29. QSOP-16 PCB Land Pattern

Table 23. QSOP-16 Land Pattern Dimensions[1, 2]

Dimension	Feature	mm
C1	Pad column spacing	5.40
E	Pad row pitch	0.635
X1	Pad width	0.40
Y1	Pad length	1.55

1. This Land pattern design is based on IPC-7351 pattern SOP63P602X173-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9.3. Land Pattern (SSO-8)

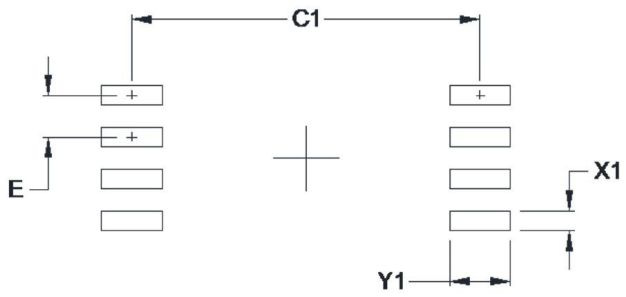

Figure 30. SSO-8 Land Pattern

Table 24. SSO-8 Land Pattern Dimensions

Symbol	mm
C1	10.60
E	1.27
X1	0.60
Y1	1.85

General:

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is based on Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.4. Land Pattern (NB SOIC-8)

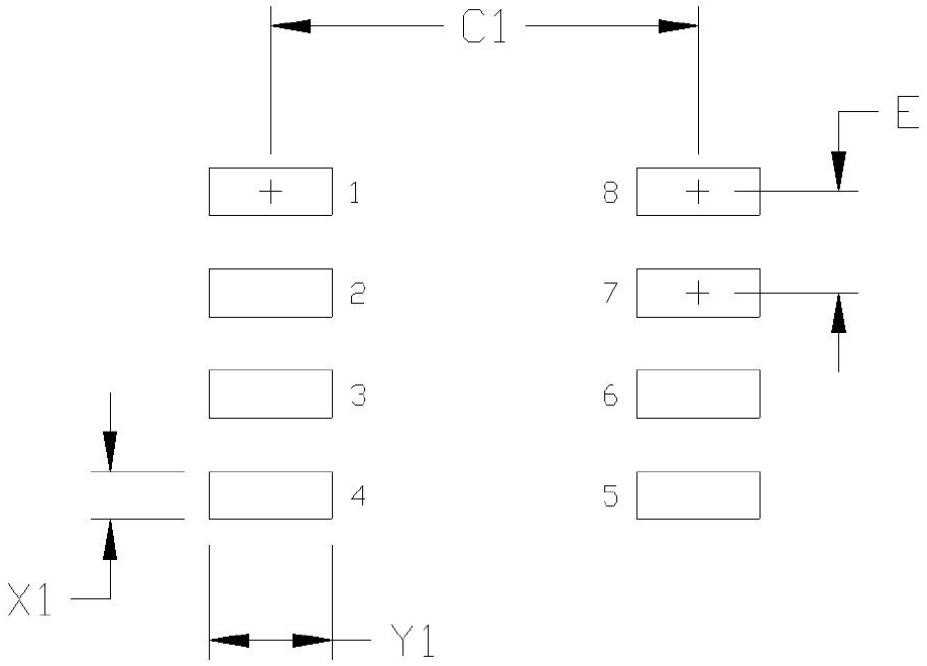

Figure 31. NB SOIC-8 Land Pattern

Table 25. NB SOIC-8 Land Pattern Dimensions

Symbol	mm
C1	5.40
E	1.27
X1	0.60
Y1	1.55

General:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Top Marking

10.1. Top Marking (WB SOIC-16)

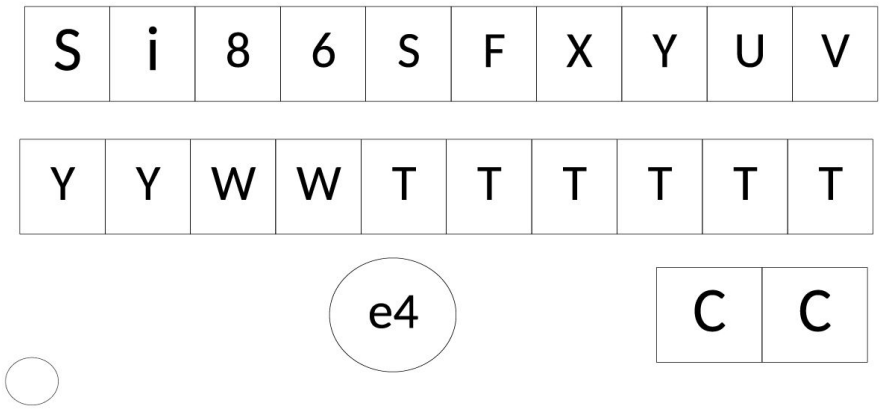

Figure 32. WB SOIC-16 Top Marking

Table 26. WB SOIC-16 Top Marking Explanation

Line 1 marking:	Base part number ordering options (See Section 11. Ordering Information for more information)	Si86S = Isolator product series F = product family 6 = Industry standard footprint XY= Channel configuration 05 = Bi-directional SDA and SCL; 1 forward and 1 reverse uni-directional 06 = Bi-directional SDA and SCL; 2 forward uni-directional U = Speed grade A = 1.7 MHz V = Isolation rating E = 6.0 kV_{RMS}
Line 2 Marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
	TTTTTT	Manufacturing code from assembly house
Line 3 marking:	Circle = 1.5 mm diameter (center justified)	“e4” Pb-Free Symbol
	CC	Country of Origin ISO Code Abbreviation
Note: Automotive-grade part numbers are indicated on the shipping label.		

10.2. Top Marking (QSOP-16)

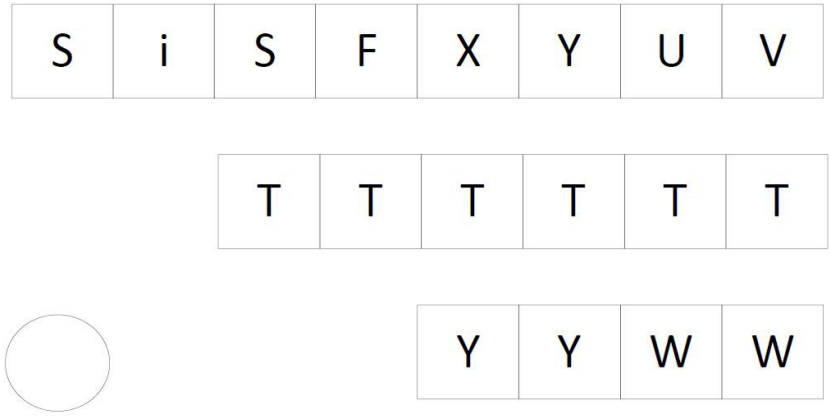

Figure 33. QSOP-16 Top Marking

Table 27. QSOP-16 Top Marking Explanation

Line 1 marking:	Base part number ordering options (See Section 11. Ordering Information for more information)	SiS = Si86S Isolator product series F = product family 6 = Industry standard footprint XY= Channel configuration 05 = Bi-directional SDA and SCL; 1 forward and 1 reverse uni-directional 06 = Bi-directional SDA and SCL; 2 forward uni-directional U = Speed grade A = 1.7 MHz V = Isolation rating B = 2.5 kV_{RMS}
Line 2 marking:	TTTTTT	Manufacturing code from assembly house
Line 3 marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
Note: Automotive-grade part numbers are indicated on the shipping label.		

10.3. Top Marking (SSO-8)

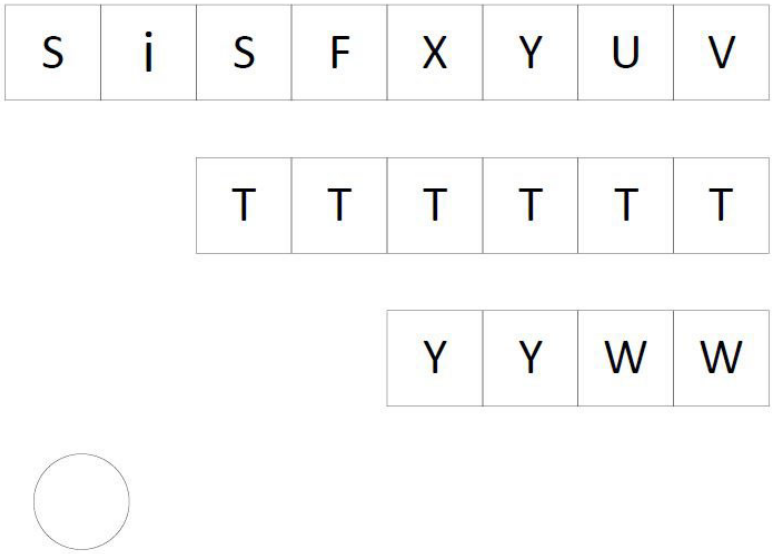

Figure 34. SSO-8 Top Marking

Table 28. SSO-8 Top Marking Explanation

Line 1 marking:	Base part number ordering options (See Section 11. Ordering Information for more information)	SiS = Si86S Isolator product series F = product family 6 = Industry standard footprint XY = Channel configuration 00 = Bi-directional SDA and SCL 02 = Bi-directional SDA and uni-directional SCL U = Speed grade A = 1.7 MHz V = Isolation rating E = 6.0 kV_{RMS}
Line 2 Marking:	TTTTTT	Manufacturing code from assembly house
Line 3 marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
Note: Automotive-grade part numbers are indicated on the shipping label.		

10.4. Top Marking (NB SOIC-8)

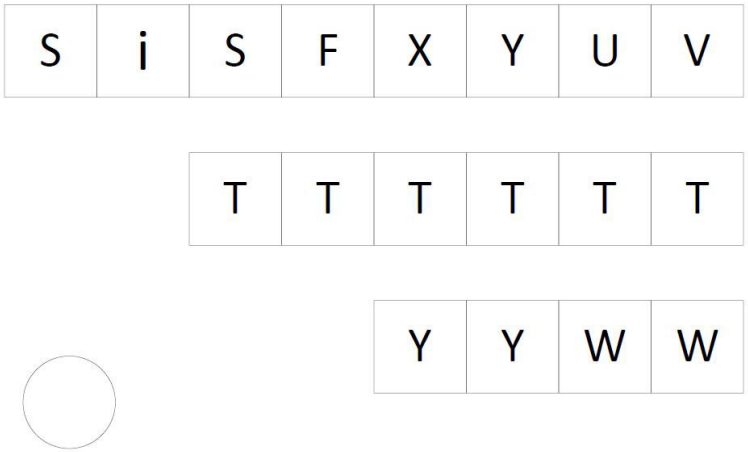

Figure 35. NB SOIC-8 Top Marking

Table 29. NB SOIC-8 Top Marking Explanation

Line 1 marking:	Base part number ordering options (See Section 11. Ordering Information for more information)	SiS = Si86S isolator product series F = product family 6 = Industry standard footprint XY = Channel configuration 00 = Bi-directional SDA and SCL 02 = Bi-directional SDA and uni-directional SCL U = Speed grade A = 1.7 MHz V = Isolation rating C = 3.75 kV_{RMS}
Line 2 Marking:	TTTTTT	Manufacturing code from assembly house
Line 3 marking:	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
Note: Automotive-grade part numbers are indicated on the shipping label.		

11. Ordering Information

Industrial and Automotive Grade Ordering Part Numbers (OPNs)

Industrial-grade devices (part numbers having an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an “-A” in their suffix) are built using automotive-specific flows and additional statistical process controls at all steps in the manufacturing process, to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listings. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps. Automotive-Grade devices (with an “-A” suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with an “-I” suffix) version counterparts.

Refer to Top Marking section for product decoder.

Table 30. Ordering Guide [1, 2, 3, 4]

Ordering Part Number (OPN)	Automotive OPNs[5]	Number of Bidirectional I^2C Channels	Number of Unidirectional Non-I^2C Channels	Isolation Rating (kV_{RMS})	Package
Si86S600AC-IS	Si86S600AC-AS	2	0	3.75	NB SOIC-8
Si86S600AE-IS4	Si86S600AE-AS4	2	0	6	SSO-8
Si86S602AC-IS	Si86S602AC-AS	1	1	3.75	NB SOIC-8
Si86S602AE-IS4	Si86S602AE-AS4	1	1	6	SSO-8
Si86S605AB-IU	Si86S605AB-AU	2	1 Forward 1 Reverse	2.5	QSOP-16
Si86S605AE-IS2	Si86S605AE-AS2	2	1 Forward 1 Reverse	6	WB SOIC-16
Si86S606AB-IU	Si86S606AB-AU	2	2 Forward	2.5	QSOP-16
Si86S606AE-IS2	Si86S606AE-AS2	2	2 Forward	6	WB SOIC-16

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. Temperature range is –40 to 125 °C.
5. In the top markings of each device, the Manufacturing Code represented by “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

12. Revision History

Revision	Date	Description
B	August, 2023	Added clarification statement about Automotive grade products in Description section on front page. Added maximum ratings for output current in: Table 5, “Absolute Maximum Ratings,” on page 12. Typo and formatting corrections made in: Table 14, “IEC 60747-17 Insulation Characteristics for Si86S60x,” on page 20, Table 15, “UL 1577 Insulation Characteristics,” on page 20, and Table 16, “IEC 60747-17 Safety Limiting Values,” on page 20. Updated “9.1. Land Pattern (WB SOIC-16)” on page 30.
A	April, 2023	Reformatted to new standards.