DATA SHEET

Si86S61x/S62x/SOx: Single and Dual Channel Digital Isolators

Industrial Applications

- Industrial automation systems
- Medical electronics
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Automotive Applications

- Onboard chargers
- Battery management systems
- Charging stations
- Traction inverters
- Hybrid electric vehicles
- Battery electric vehicles

Features

- High-speed operation: DC to 150 Mbps
- No start-up initialization required
- Wide supply voltage: 2.25 to 5.5 V
- Up to 6000 V_{RMS} isolation
- Reinforced IEC 60747-17 rating
- High electromagnetic immunity
- Schmitt trigger + CMOS threshold inputs
- Selectable fail-safe mode:
  Default high or low output (ordering option)
- Precise timing (typical)
  - 10 ns propagation delay
  - 3.5 ns pulse width distortion
- Transient Immunity of 100 kV/µs (min)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

- AEC-Q100 qualification
- Wide temperature range
  - –40 to +125 °C
- RoHS-compliant packages
  - NB SOIC-8
  - SSO-8
- Automotive-grade OPNs available
  - AIAG compliant PPAP documentation support
  - IMDS and CAMDS listing support

Safety Regulatory Approvals (Pending)

- UL 1577 recognized
  - Up to 6000 V_{RMS} for 1 minute
- CSA certification conformity
  - 62368-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval, GB4943.1

Description

The Skyworks family of robust, low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. All versions have CMOS thresholds and Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors. Data rates up to 150 Mbps are supported, and all devices achieve typical propagation delays of 10 ns. This family includes inverted output product options. Options also include a choice of isolation ratings (3.75 and 6 kV_{RMS}) and options for fail-safe operating mode to control the default output state during power loss. All products are safety certified by UL, CSA, VDE, and CQC. Products in wide-body packages support voltages of 6.0 kV_{RMS} with 1 minute withstand capability per UL 1577. Automotive Grade is available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

1. Pin Descriptions

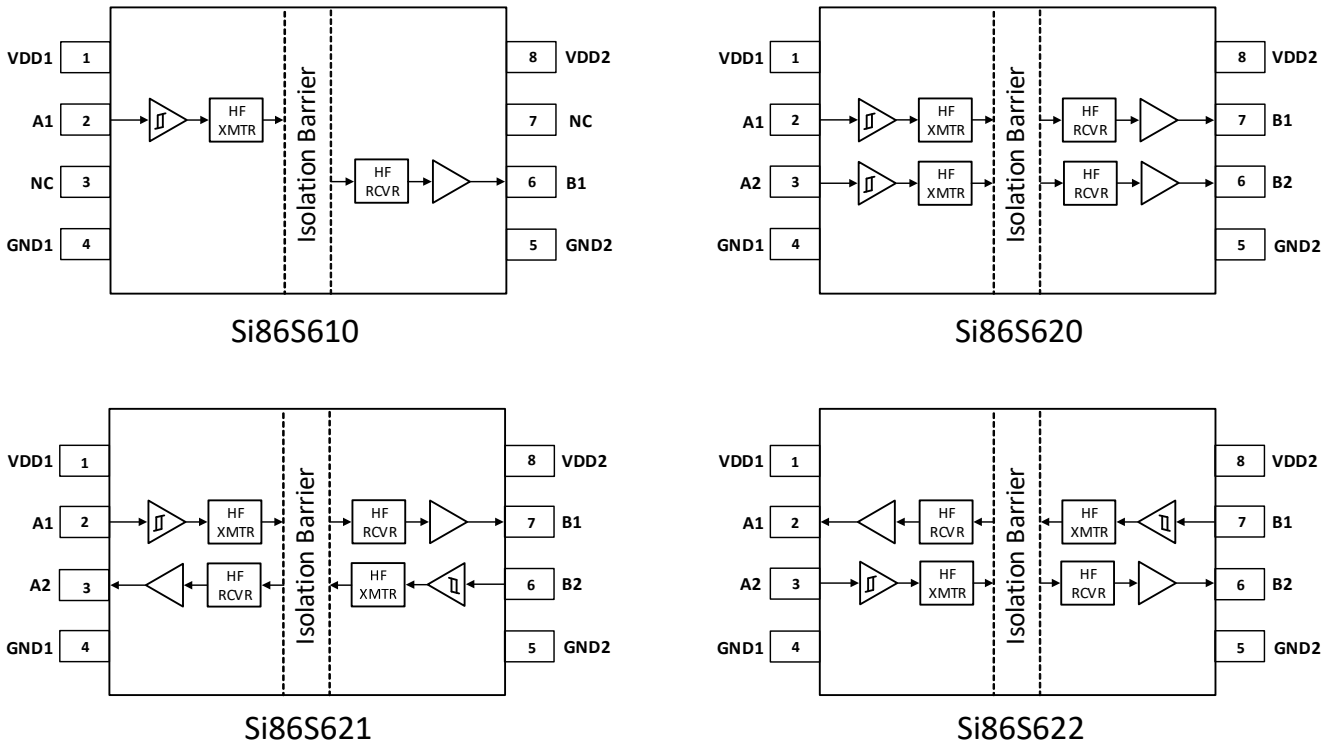

Figure 1. Si86S61x/2x/Ox Pinout

Table 1. Si86S61x/2x/Ox Pin Description

Name	Type	Description
VDD1	Supply	Side A power supply
GND1	Ground	Side A ground
A1 – A2	Digital I/O	Side A digital I/O
NC	No connect	Do not connect pin
GND2	Ground	Side B ground
B1 – B2	Digital I/O	Side B digital I/O
VDD2	Supply	Side B power supply

2. Technical Description

2.1. Theory of Operation

The operation of an Si86S61x/2x/Ox channel is analogous to an optocoupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si86S61x/2x/Ox channel is shown in Figure 2.

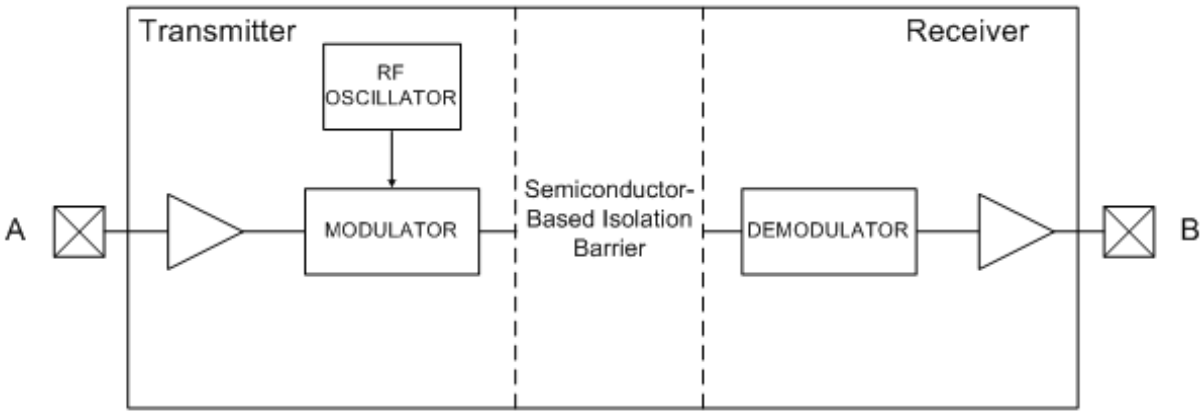

Figure 2. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying.

The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and improved immunity to magnetic fields, see Figure 3.

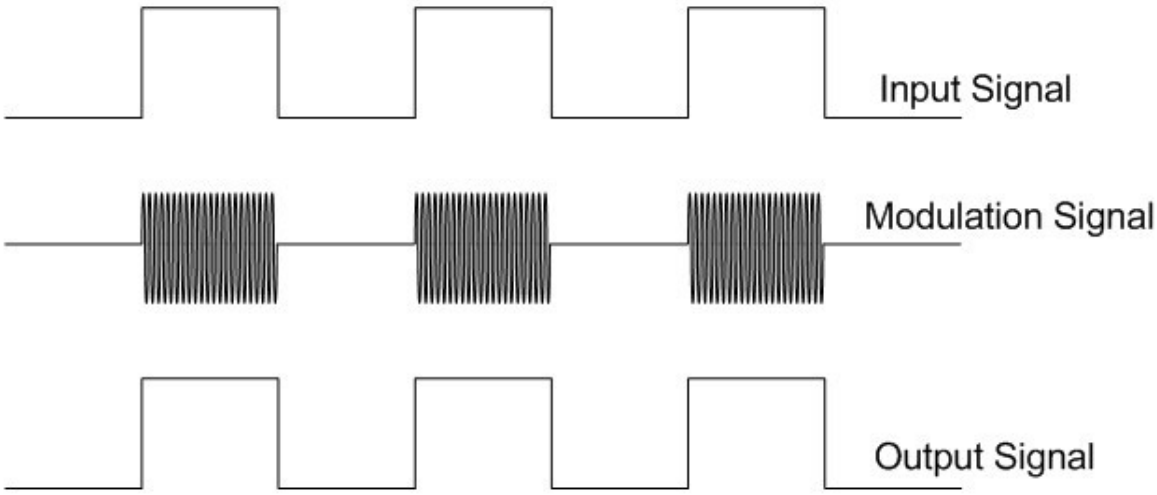

Figure 3. Modulation Scheme

3. Device Operation and System Overview

Device behavior during start-up, normal operation, and shutdown is shown below, where UVLO+ and UVLO– are the respective positive-going and negative-going thresholds. Refer to the following table to determine outputs when power supply (VDD) is not present.

Table 2. Si86S6x/Ox Logic Operation

VI Input[1,2,3]	VDDI State[1,4,5]	VDDO State[1,4,5]	VO Output[1,2,3]	Comments
H	P	P	H/L	Normal operation for Si86S6x/SOx options. The Si86SOx options are inverting outputs.
L	P	P	L/H	
X	UP	P	L[6]	Default low options.
			H[6]	Default high options.
X	P	UP	UD[7]	Upon transition of VDDO from un-powered to powered, V_O returns to correct state. Refer to Note 7 below.

1. VI and VO are the input and output terminals of any one channel. VDDI and VDDO are the power supplies on the respective input and output sides.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
4. “Powered” state (P) is defined as 2.25 V < VDD < 5.5 V.
5. “Unpowered” state (UP) is defined as VDD < 2.25 V.
6. This is the selectable fail-safe operating mode (ordering option). Some devices have default output state = H, and some have default output state = L. For default high devices, the data channels have pull-ups on inputs/outputs. For default low devices, the data channels have pull-downs on inputs/outputs.
7. UD = Undetermined. Refer to "Timing diagram for startup" below notes section, the start-up time from un-powered state, below 1.7 V (RSTB) threshold to powered state, is 0.3 ms. If VDDO only dips below 2.1 V but stays above RSTB level, the start-up time is 1 µs.

3.1. Device Startup, UVLO, and Reset Functionality

Outputs are held low during power-up until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs. The start-up time of the device is estimated to be 0.3 ms due to the device initialization time. During this time, the outputs will have a 100 kΩ pulldown resistor that will pull the outputs low. After stabilization, the outputs will transition to the default output state indicated by the particular product option.

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, referring to the figure below, Side A unconditionally enters UVLO when VDD1 falls below VDD1(UVLO–) and exits UVLO when VDD1 rises above VDD1(UVLO+). Side B operates the same as Side A with respect to its VDD2 supply.

Along with UVLO, each side has its own self biased circuitry that can detect supply going low enough and issue a complete reset of the part. This is done to avoid loss of device configuration for the particular product option. Referring to the figure below, Side A goes into reset as soon as VDD1 goes below RSTB- (~1.7 V) and comes out of reset when VDD1 goes above RSTB+. When the supply voltage is above RSTB+ the device configuration is reloaded. Side B operates the same as Side A with respect to its VDD2 supply.

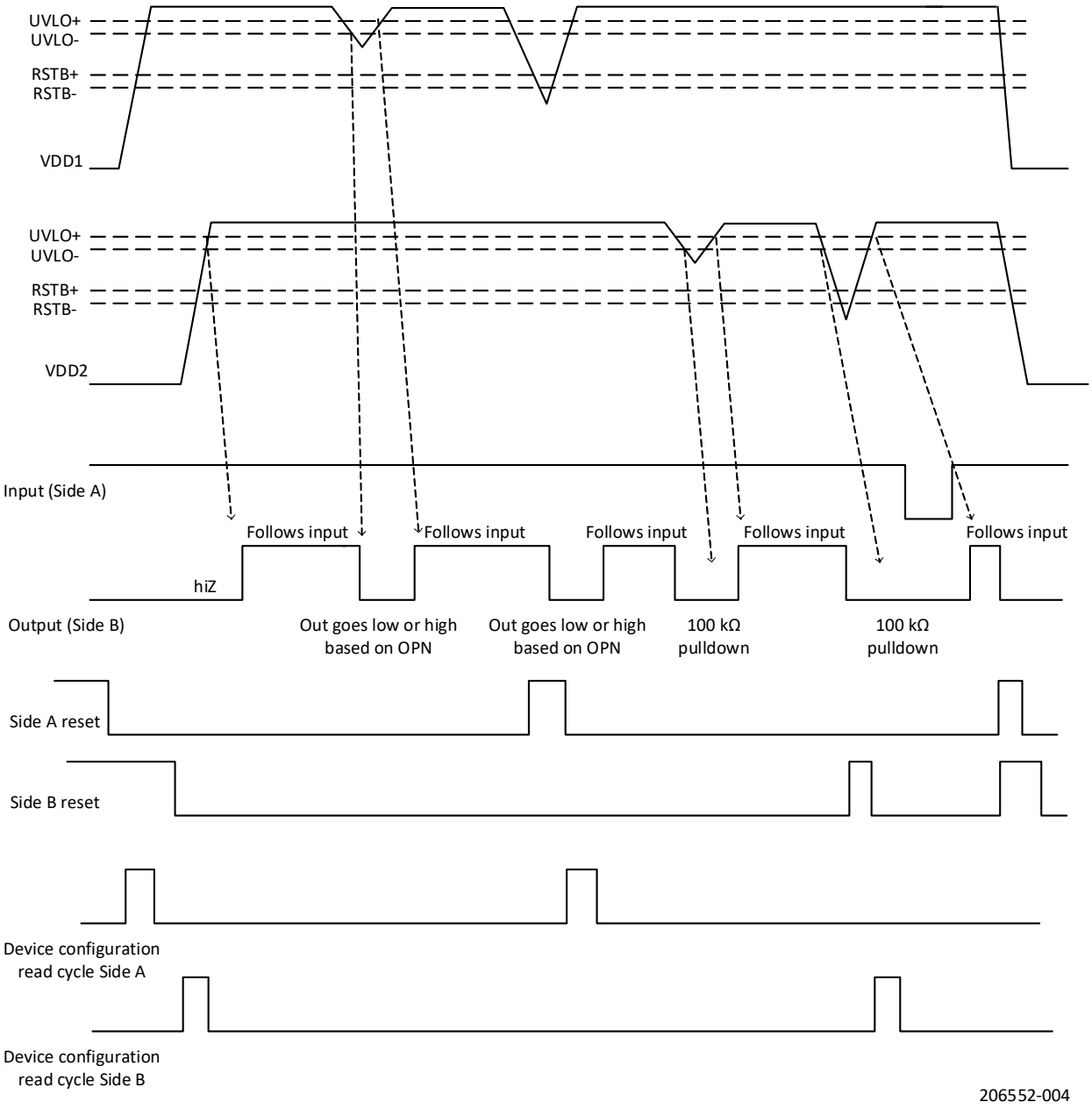

Figure 4. Startup Device Behavior

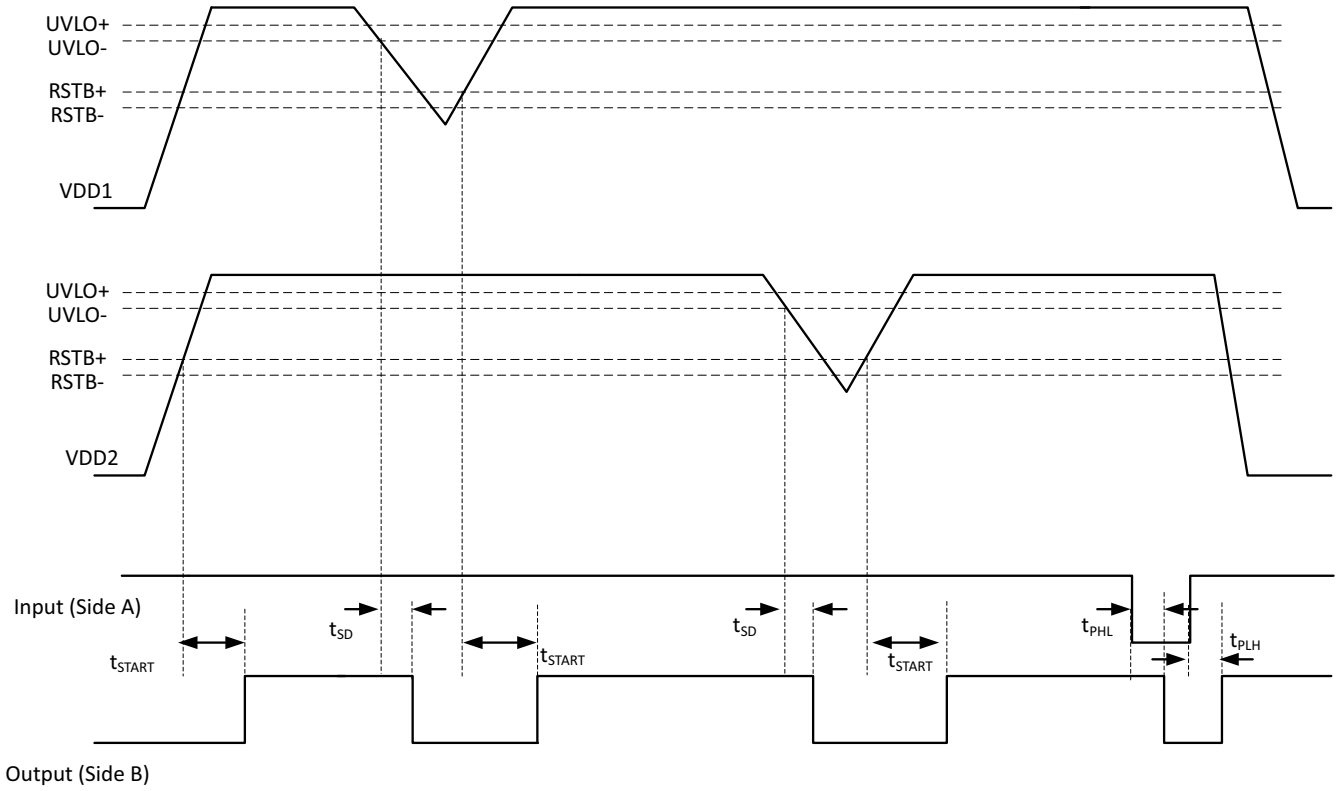

Figure 5. Device Behavior During Normal Operation

3.2. Layout Considerations

To ensure safety in the end-user application, high-voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low-voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and provide a sufficiently large high voltage breakdown protection rating (commonly referred to as working voltage protection). These requirements also detail the component standards (UL1577, IEC 60747-17), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 62368-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.2.1. Supply Bypass

The Si86S61x/2x/Ox family requires 0.1 and 10 µF bypass capacitors between VDD1 and GND1 and VDD2 and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50 to 300 Ω) in series with the inputs and outputs if the system is excessively noisy.

3.2.2. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled-impedance PCB traces.

3.3. Fail-Safe Operating Mode

Si86S61x/2x/Ox devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is not powered) can either be a logic high or logic low when the output supply is powered. See Table 2 for more information.

3.4. Device Features and System Overview

3.4.1. Input Noise Filters with Deglitch Times of 36 ns

The Si86S62x family is orderable with input deglitch filters which have delay times of 36 ns. These filters remove undesirable noise pulses (glitches) from the input signal so that the isolator only produces an output for a valid input. Any input pulse which lasts less than the deglitch time will not be passed by the filter. Any other input pulse will be passed by the filter and delayed by the filter delay time, as shown below. Figure 6 shows a positive noise pulse, but negative pulses will also be filtered out.

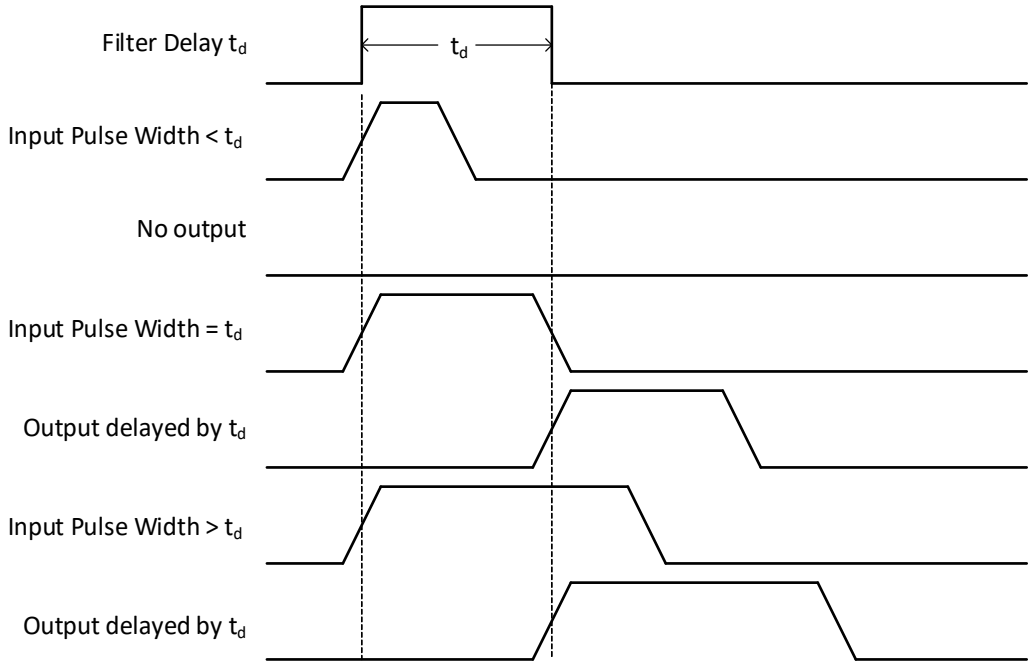

Figure 6. Input Noise Filter Functionality

4. Electrical Specifications

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	–65	150	°C
Operating temperature	T_A	–40	125	°C
Junction temperature	T_J	—	150	°C
Supply voltage	VDD1, VDD2	–0.5	7.0	V
Supply voltage ramp-up	VDD1, VDD2	—	1	V/µs
Input voltage	V_I	–0.5	VDD + 0.5	V
Output voltage	V_O	–0.5	VDD + 0.5	V
Output current drive	I_O	–10	+10	mA
ESD	HBM	—	8	kV
	CDM	—	2	kV
	IEC 61000-4-2 contact discharge[2]	—	8000	V
Lead solder temperature (10 s)		—	260	°C

1. Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.
2. This test is performed across the isolation barrier with device in a two terminal configuration, with pins on each side shorted together. Tested per IEC 61000-4-2 contact discharge.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 4. Recommended Operating Conditions[1]

Parameter	Symbol	Min	Typ	Max	Unit
Junction operating temperature	T_J	—	—	150	°C
Ambient operating temperature	T_A	–40	25	125	°C
Supply voltage	VDD1, VDD2	2.25	—	5.5	V

1. The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage. The maximum junction temperature is a limitation, and the maximum ambient temperature for any given condition can be calculated as shown in 6.1. Estimating Maximum Ambient Temperature

Table 5. Electrical Characteristics (General)

T_A = –40 to 125 °C, VDD1, VDD2 as specified in Recommended Operating Conditions Table above.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD undervoltage threshold	VDD_{UV+}	VDD1, VDD2 rising	2.10	2.18	2.25	V
VDD undervoltage threshold	$VDD_{UV–}$	VDD1, VDD2 falling	1.98	2.05	2.12	V
VDD undervoltage hysteresis	VDD_{HYS}		105	131	160	mV
Input hysteresis	V_{HYS}		0.15 x VDDx	—	—	V
High level input voltage	V_{IH}		0.7 x VDDx	—	—	V
Low level input voltage	V_{IL}		—	—	0.3 x VDDx	V
High level output voltage	V_{OH}	I_{OH} = –4 mA	VDD1, VDD2–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 4 mA	—	—	0.4	V
Output impedance	Z_O		—	50	—	Ω

Table 6. Electrical Characteristics (VDD = 5.0 V)

VDD1 = 5.0 ±10%, VDD2 = 5.0 V ±10%, T_A = -40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S610Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	 0.46 0.97 1.05 1.00	 0.54 1.20 1.22 1.22	mA
IDD1 IDD2		All inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	0.75 1.01	0.88 1.24	mA
Si86S620/O20Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	 0.52 1.54 1.69 1.60	 0.62 1.93 1.97 1.97	mA
IDD1 IDD2		All inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	1.16 1.61	1.28 2.00	mA
Si86S621/O21Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	 1.05 1.05 1.68 1.67	 1.29 1.29 1.98 1.97	mA
IDD1 IDD2		All inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	1.39 1.39	1.67 1.67	mA
Si86S622Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	 1.04 1.04 1.68 1.66	 1.28 1.28 2.01 1.98	mA
IDD1 IDD2		All Inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	1.39 1.37	1.69 1.66	mA
Timing Characteristics						
Data rate Si86SxxxB/Ex			—	—	150	Mbps
Data rate Si86SxxxF/Hx			—	—	10	Mbps
Pulse width Si86SxxxB/Ex		Minimum pulse width that is guaranteed to be transmitted to output.	6.7	—	—	ns
Pulse width Si86SxxxF/Hx		Minimum pulse width that is guaranteed to be transmitted to output.	100	—	—	ns
Propagation delay Si86SxxxB/Ex	t_{PHL}, t_{PLH}	See Propagation Delay Timing, Figure 7	5	9	13.5	ns
Pulse width distortion Si86SxxxB/Ex $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Propagation Delay Timing, Figure 7	—	—	4.5	ns
Propagation delay skew part-to-part Si86SxxxB/Ex	$t_{PSK(P-P)}$ [1]		—	2.0	4.5	ns
Channel-channel skew Si86SxxxB/Ex	t_{PSK}		—	0.8	3	ns
Propagation delay Si86SxxxF/Hx	t_{PHL}, t_{PLH}	See Propagation Delay Timing, Figure 7	30.5	36	41.5	ns
Pulse width distortion Si86SxxxF/Hx $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Propagation Delay Timing, Figure 7	—	—	4.5	ns
Propagation delay skew part-to-part Si86SxxxF/Hx	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew Si86SxxxF/Hx	t_{PSK}		—	0.7	3.5	ns
Output rise time	t_r	C_L= 15 pF See Propagation Delay Timing, Figure 7	—	2.5	—	ns
Output fall time	t_f	C_L = 15 pF See Propagation Delay Timing, Figure 7	—	2.5	—	ns

Table 6. Electrical Characteristics (VDD = 5.0 V) (Continued)

VDD1 = 5.0 ±10%, VDD2 = 5.0 V ±10%, T_A = -40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Peak eye diagram jitter	$t_{JIT(PK)}$		—	350	—	ps
Common mode Transient immunity Si86SxxxB/Ex Si86SxxxF/Hx	CMTI	See Figure 8. Common-Mode Transient Immunity Test Circuit VI = VDD or 0 V VCM = ±1500 V	 100 150	 — —	 — —	kV/µs
Input power loss to valid default output	t_{SD}	See Device Behavior During Normal Operation, Figure 5	—	8.0	12	ns
Start-up time[2]	t_{START}	See Device Behavior During Normal Operation, Figure 5	—	—	300	µs
Input leakage current	I_L		–8	—	+8	µA

1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and fn ambient temperature.
2. Start-up time is the time period from the application of power to the appearance of valid data at the output. The device initialization time is included in the 300 µs specification.

Table 7. Electrical Characteristics (VDD = 3.3 V)

VDD1 = 3.3 V ±10%, VDD2 = 3.3 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S610Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 —	 0.43 0.94 1.02 0.97	 0.50 1.17 1.19 1.19	mA
IDD1 IDD2		All Inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	0.72 0.75	0.84 0.88	mA
Si86S620/O20Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 —	0.49 1.51 1.66 1.57	0.58 1.89 1.92 1.93	mA
IDD1 IDD2		All Inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	1.07 1.11	1.24 1.28	mA
Si86S621/O21Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 —	1.00 1.00 1.63 1.63	1.23 1.23 1.93 1.93	mA
IDD1 IDD2		All Inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	1.34 1.34	1.61 1.61	mA
Si86S622Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 —	1.03 1.03 1.65 1.63	1.26 1.26 1.97 1.97	mA
IDD1 IDD2		All Inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	1.35 1.35	1.62 1.62	mA
Timing Characteristics						
Data rate Si86SxxxB/Ex			—	—	150	Mbps
Data rate Si86SxxxF/Hx			—	—	10	Mbps
Pulse width Si86SxxxB/Ex		Minimum pulse width that is guaranteed to be transmitted to output.	6.7	—	—	ns
Pulse width Si86SxxxF/Hx		Minimum pulse width that is guaranteed to be transmitted to output.	100	—	—	ns
Propagation delay Si86SxxxB/Ex	t_{PHL}, t_{PLH}	See Propagation Delay Timing, Figure 7	5	9	14	ns

Table 7. Electrical Characteristics (VDD = 3.3 V) (Continued)

VDD1 = 3.3 V ±10%, VDD2 = 3.3 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pulse width distortion Si86SxxxB/Ex $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Propagation Delay Timing, Figure 7	—	—	4.5	ns
Propagation delay skew part-to-part Si86SxxxB/Ex	$t_{PSK(P-P)}$[1]		—	2.0	4.5	ns
Channel-channel skew Si86SxxxB/Ex	t_{PSK}		—	0.7	4	ns
Propagation delay Si86SxxxF/Hx	t_{PHL}, t_{PLH}	See Propagation Delay Timing, Figure 7	30.5	36	41.5	ns
Pulse width distortion Si86SxxxF/Hx $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Propagation Delay Timing, Figure 7	—	—	4.5	ns
Propagation delay skew part-to-part Si86SxxxF/Hx	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew Si86SxxxF/Hx	t_{PSK}		—	0.85	3.0	ns
Output rise time	t_r	C_L = 15 pF See Propagation Delay Timing, Figure 7	—	2.5	—	ns
Output fall time	t_f	C_L = 15 pF See Propagation Delay Timing, Figure 7	—	2.5	—	ns
Peak eye diagram jitter	$t_{JIT(PK)}$		—	350	—	ps
Common-mode transient immunity Si86SxxxB/Ex Si86SxxxF/Hx	CMTI	See Common-Mode Transient Immunity Test Circuit, Figure 8 VI = VDD or 0 V VCM = ±1500 V	 100 150	 — —	 — —	kV/µs
Input power loss to valid default output	t_{SD}	See Device Behavior During Normal Operation, Figure 5	—	8.0	12	ns
Start-up time[2]	t_{START}	See Device Behavior During Normal Operation, Figure 5	—	—	300	µs
Input leakage current	I_L		–7	—	+7	µA

1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and fn ambient temperature.
2. Start-up time is the time period from the application of power to the appearance of valid data at the output. The device initialization time is included in the 300 µS specification.

Table 8. Electrical Characteristics (VDD = 2.5 V)

IDD1 = 2.5 V ±10%, IDD2 = 2.5 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si86S610Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 —	 0.41 0.92 1.00 0.95	 0.49 1.15 1.17 1.17	mA
IDD1 IDD2		All Inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	0.71 0.95	0.83 1.17	mA
Si86S620/O20Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 —	 0.47 1.49 1.64 1.55	 0.57 1.88 1.90 1.91	mA
IDD1 IDD2		All Inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	1.06 1.54	1.22 1.92	mA
Si86S621/O21Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	 —	 1.00 1.00 1.63 1.63	 1.23 1.22 1.92 1.92	mA

Table 8. Electrical Characteristics (VDD = 2.5 V) (Continued)

IDD1 = 2.5 V ±10%, IDD2 = 2.5 V ±10%, T_A = –40 to 125 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IDD1 IDD2		All Inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	1.32 1.32	1.59 1.59	mA
Si86S622Bx, Ex IDD1 IDD2 IDD1 IDD2		 VI = 0(Bx), 1(Ex) VI = 0(Bx), 1(Ex) VI = 1(Bx), 0(Ex) VI = 1(Bx), 0(Ex)	—	 1.01 1.01 1.63 1.61	 1.24 1.24 1.95 1.93	mA
IDD1 IDD2		All Inputs = 500 kHz square wave, C_L = 15 pF on all outputs	—	1.33 1.31	1.60 1.59	mA
Timing Characteristics						
Data rate Si86SxxxB/Ex			—	—	150	Mbps
Data rate Si86SxxxF/Hx			—	—	10	Mbps
Pulse width Si86SxxxB/Ex		Minimum pulse width that is guaranteed to be transmitted to output.	6.7	—	—	ns
Pulse width Si86SxxxF/Hx		Minimum pulse width that is guaranteed to be transmitted to output.	100	—	—	ns
Propagation delay Si86SxxxB/Ex	t_{PHL}, t_{PLH}	See Propagation Delay Timing, Figure 7	6.5	9.5	17	ns
Pulse width distortion Si86S6xxxB/Ex $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Propagation Delay Timing, Figure 7	—	—	4.5	ns
Propagation delay skew part-to-part Si86SxxxB/Ex	$t_{PSK(P-P)}$[1]		—	2.0	4.5	ns
Channel-channel skew Si86SxxxB/Ex	t_{PSK}		—	0.65	3.5	ns
Propagation delay Si86SxxxF/Hx	t_{PHL}, t_{PLH}	See Propagation Delay Timing, Figure 7	31.5	36.5	45	ns
Pulse width distortion Si86SxxxF/Hx $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Propagation Delay Timing, Figure 7	—	—	4.5	ns
Propagation delay skew part-to-part Si86SxxxF/Hx	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-channel skew Si86SxxxF/Hx	t_{PSK}		—	0.85	3	ns
Output rise time	t_r	C_L = 15 pF See Propagation Delay Timing, Figure 7	—	2.5	—	ns
Output fall time	t_f	C_L = 15 pF See Propagation Delay Timing, Figure 7	—	2.5	—	ns
Peak eye diagram jitter	$t_{JIT(PK)}$		—	350	—	ps
Common mode transient immunity Si86SxxxB/Ex Si86SxxxF/Hx	CMTI	See Common-Mode Transient Immunity Test Circuit, Figure 8 VI = VDD or 0 V VCM = ±1500 V	 100 150	 — —	 — —	kV/µs
Input power loss to valid default output	t_{SD}	See Device Behavior During Normal Operation, Figure 5	—	8.0	12	ns
Start-up time[2]	t_{START}	See Device Behavior During Normal Operation, Figure 5	—	—	300	µs
Input leakage current	I_L		–7	—	+7	µA

1. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and fn ambient temperature.
2. Start-up time is the time period from the application of power to the appearance of valid data at the output. The device initialization time is included in the 300 µs specification.

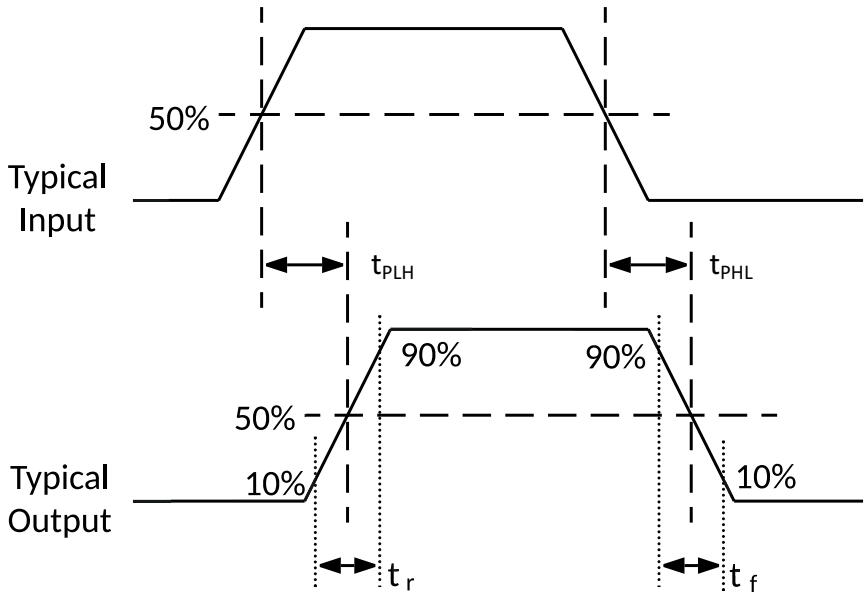

Figure 7. Propagation Delay Timing

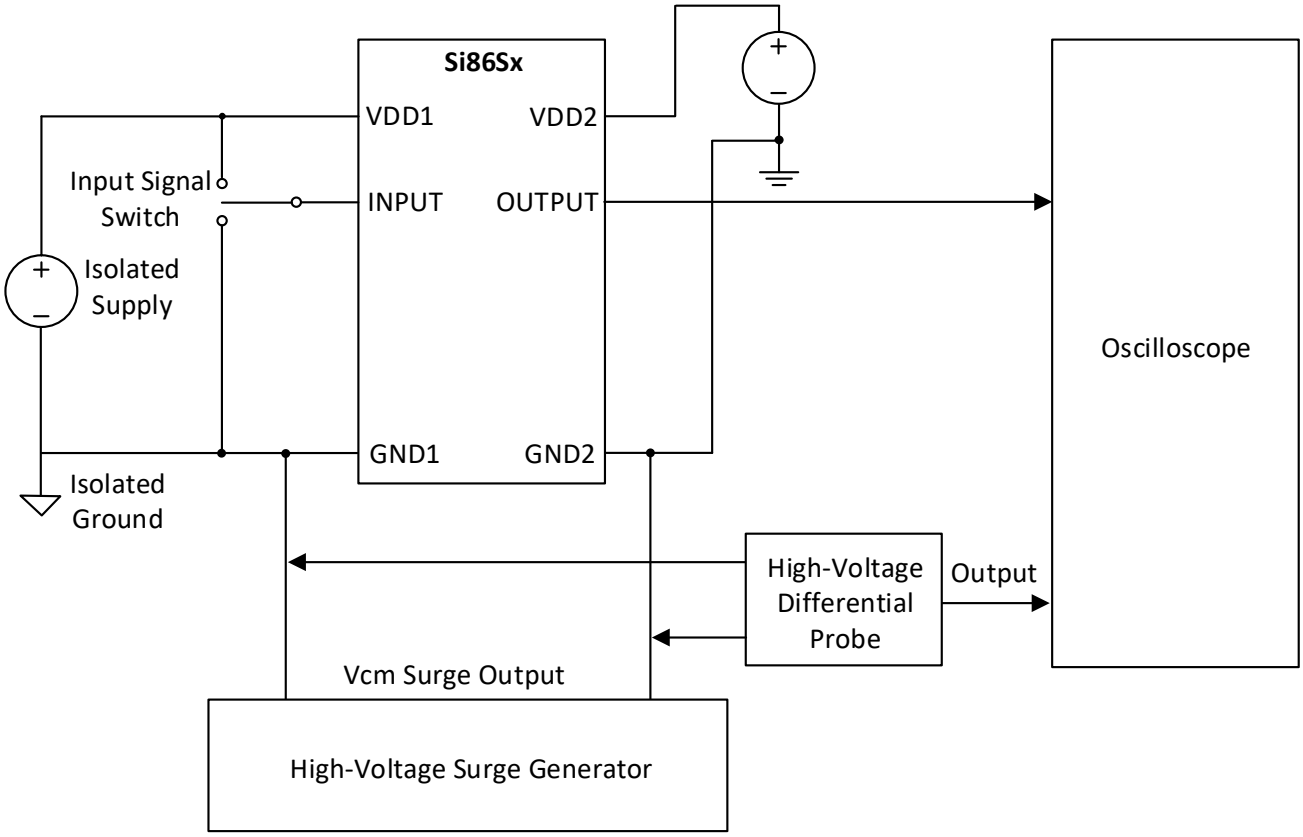

Figure 8. Common-Mode Transient Immunity Test Circuit

5. Safety Certifications and Specifications

Table 9. Regulatory Information (Pending)[1]

CSA
The Si86S61x/2x/Ox is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} working voltage and 2 MOPP (Means of Patient Protection).
VDE
The Si86S61x/2x/Ox is certified under VDE. For more details, see File 5028467.
60747-17: Up to 2121 Vpeak for reinforced insulation working voltage.
UL
The Si86S61x/2x/Ox is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si86S61x/2x/Ox is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see 11. Ordering Information .

Table 10. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			SSO-8	NB SOIC-8	
Nominal external air gap (clearance)	CLR		8.0	3.9	mm
Nominal external tracking (creepage)	CRP		8.0	3.9	mm
Minimum internal gap (internal clearance)	DTI		0.036	0.036	mm
Tracking resistance	CTI or PTI	IEC60112	600	600	V_{RMS}
Erosion depth	ED		0.019	0.04	mm
Resistance (input-output) [1]	R_{IO}	Test voltage = 500 V at 25 °C	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	1.0	1.0	pF
Input capacitance[2]	C_I		4.0	4.0	pF

1. To determine resistance and capacitance, the Si86Sx is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 11. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification	
		SSO-8	NB SOIC-8
Material group		I	I
Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	I-IV
	Rated mains voltage ≤300 V_{RMS}	I-IV	I-III
	Rated mains voltage ≤600 V_{RMS}	I-IV	I-II
	Rated mains voltage ≤1000 V_{RMS}	I-III	I

Table 12. IEC 60747-17 Insulation Characteristics for Si86S61x/2x/Ox[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			SSO-8	NB SOIC-8	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	1500	445	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	2121	630	V_{peak}
Apparent charge	q_{pd}	Method b: At routine test (100% production) and preconditioning (type test); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	≤5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	8484	5302	V_{peak}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile	10400	10400	V_{peak}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile	8000	5000	V_{peak}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 13. UL 1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			SSO-8	NB SOIC-8	
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	6000	3750	V_{RMS}

Table 14. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max		Unit
			SSO-8	NB SOIC-8	
Safety temperature	T_S		150	150	°C
Safety input, output, or supply current	I_S	Refer to θ_{JA} in Table 15, Thermal Characteristics. V_{DD} = 5.5 V, T_J = 150 °C, T_A = 25 °C.	253	221	mA
Safety input, output, or total power	P_S		1389	1214	mW

1. Maximum value allowed in the event of a failure; also see the thermal derating curves in Figure 9 and Figure 10.

Table 15. Thermal Characteristics

Parameter	Symbol	SSO-8	NB SOIC-8	Unit
IC junction-to-air thermal resistance	θ_{JA}	90	103	°C/W
IC junction-to-board thermal resistance	θ_{JB}	47	45	
IC junction-to-case thermal resistance	θ_{JC}	27	26	
Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board	Ψ_{JB}	43	42	

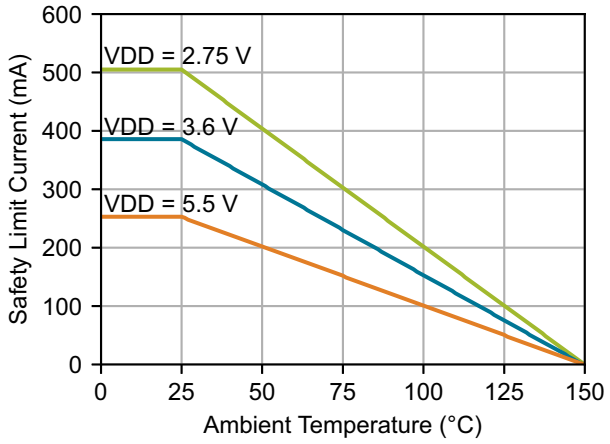

Figure 9. SSO-8 Thermal Derating Curve, Dependence of Safety Limiting Current

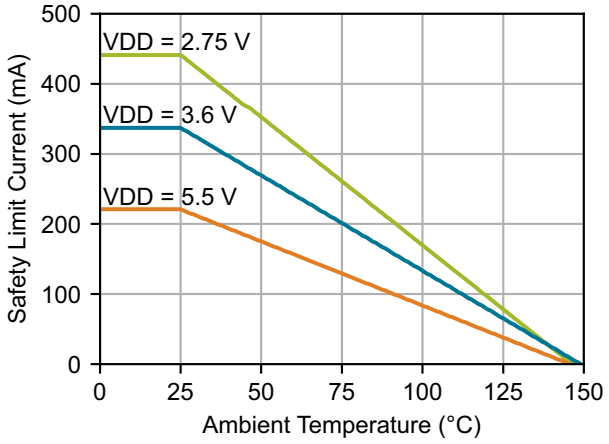

Figure 10. NB SOIC-8 Thermal Derating Curve, Dependence of Safety Limiting Current

6. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Electrical Characteristics tables for actual specification limits. All typical characteristics data is valid for nominal VDD and ambient temperature of 25 °C.

For typical IDD, refer to the Isolator Power Consumption Calculator.

6.1. Estimating Maximum Ambient Temperature

$T_{A(max)} = T_{Jmax} – P \times \theta_{JA}$. θ_{JA} values are specified in Table 15 on page 16.
P = total power dissipated by package in W. Values for any OPN and operating condition can be obtained using the Isolator Power Consumption Calculator.

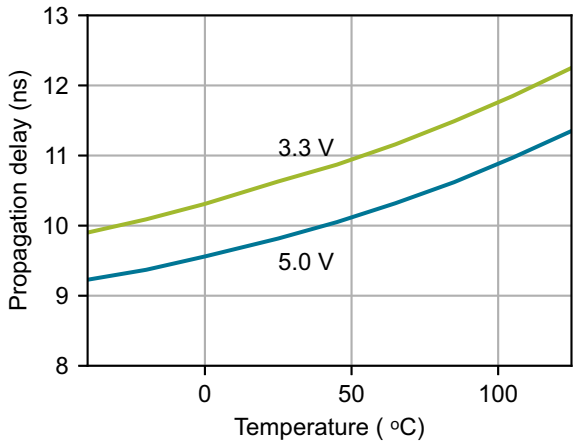

Figure 11. Si86Sx Propagation Delay vs. Temperature

7. Package Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The Si86S61x/S62x/SOx are rated to Moisture Sensitivity Level 2 (MSL2) for the NB SOIC-8 packages and MSL 2A (MSL2A) for the SSO-8 packages at 260 °C. They can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, “PCB Design & SMT Assembly/Rework Guidelines for MCM-L Packages,” document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

8. Package Dimensions

8.1. Package Outline, SSO-8

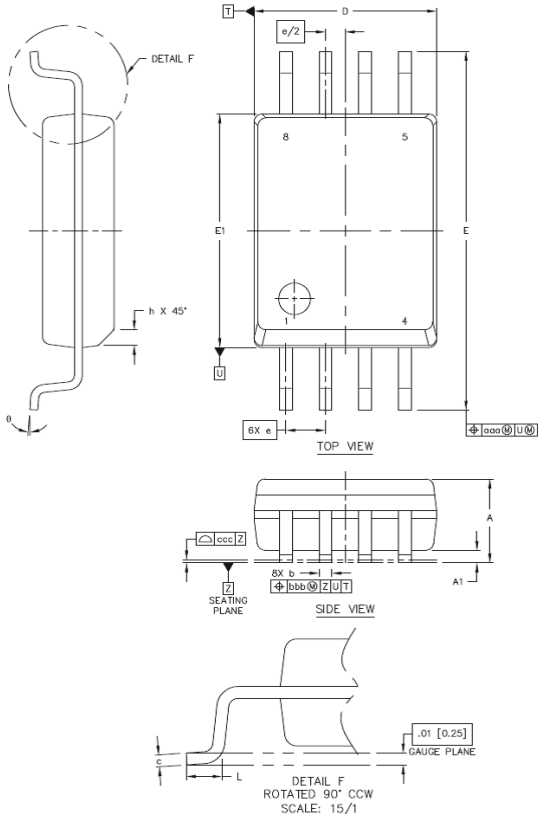

Figure 12. SSO-8 Package

Table 16. SSO-8 Package Dimensions[1]

Dimension	Min	Max
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.20	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
h	0.25	0.76
θ	0°	8°
aaa	—	0.25
bbb	—	0.25
ccc	—	0.10

1. All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and tolerancing per ANSI Y14.5M-1994. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

8.2. Package Outline, Narrow Body SOIC-8

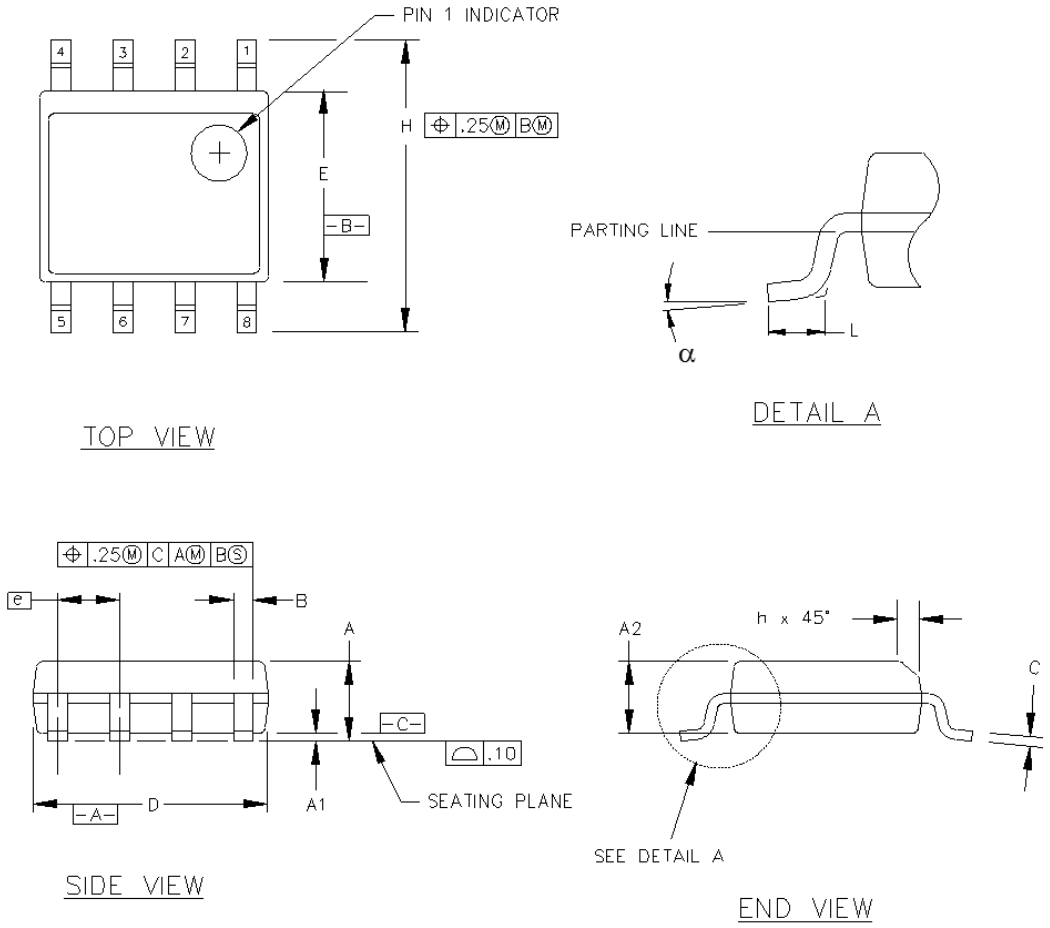

Figure 13. NB SOIC-8 Package

Table 17. NB SOIC-8 Package Diagram Dimensions[1]

Dimension	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

1. All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and tolerancing per ANSI Y14.5M-1982. This drawing conforms to JEDEC Outline MS-102. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for small body components.

9. Land Pattern, SSO-8

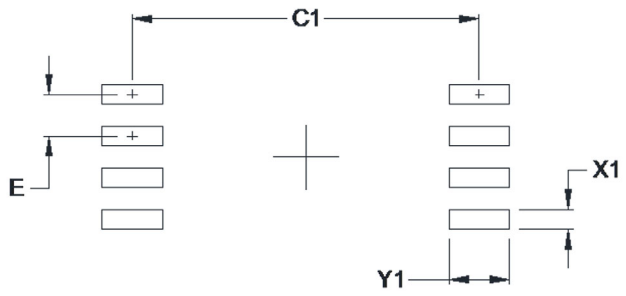

Figure 14. SSO-8 Land Pattern

Table 18. SSO-8 Land Pattern Dimensions[1]

Symbol	mm
C1	10.60
E	1.27
X1	0.60
Y1	1.85

1. **General**
   All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.
   This land pattern design is based on the IPC-7351 guidelines.
   Solder Mask Design
   All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
   Stencil Design
   A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
   The stencil thickness should be 0.125 mm (5 mils).
   The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
   Card Assembly
   A no-clean, Type-3 solder paste is recommended.
   The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

9.1. Land Pattern, NB SOIC-8

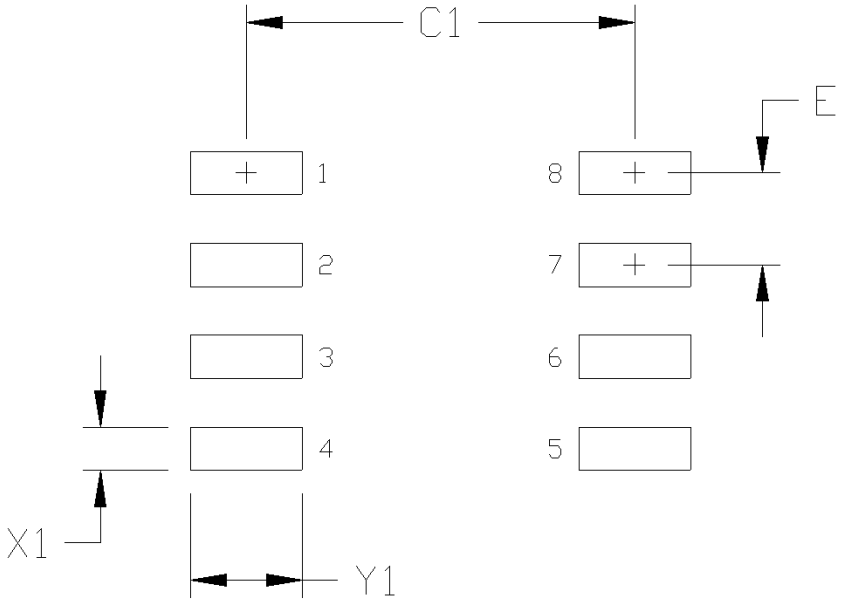

Figure 15. NB SOIC-8 Land Pattern

Table 19. NB SOIC-8 Land Pattern Dimensions[1]

Symbol	mm
C1	5.40
E	1.27
X1	0.60
Y1	1.55

1. This land pattern design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion). All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Top Marking

10.1. SSO-8 Typical Top Marking

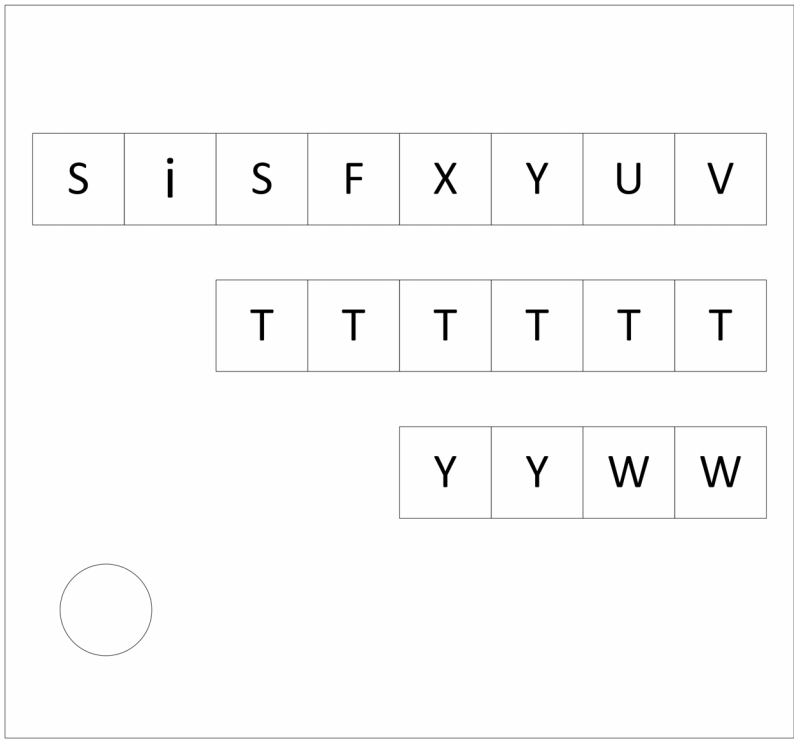

Figure 16. SSO-8 Top Marking

Table 20. SSO-8 Top Marking Explanation

Line 1 marking	Base part number ordering options (See Ordering Guide for more information)	Si86S = Isolator product series F = Product family 6 = Non-inverting outputs O = Inverting outputs X = Total number of channels Y = Total number of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 36 ns deglitch H = Output default high, 36 ns deglitch V = Isolation rating E = 6.0 kV_{RMS}
Line 2 marking	TTTTTT	Manufacturing code from assembly house
Line 3 marking	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
Automotive-grade part numbers are indicated on the shipping label.		

10.2. Narrow Body (NB) SOIC-8 Top Marking

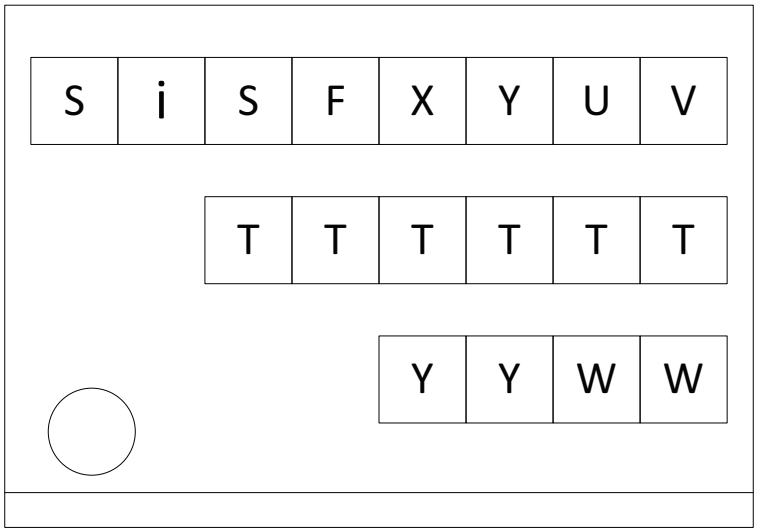

Figure 17. NB SOIC-8 Top Marking

Table 21. NB SOIC-8 Top Marking Explanation

Line 1 marking	Base part number ordering options (See 1. Ordering Guide for more information)	Si86S = Isolator product series F = Product family 6 = Non-inverting outputs O = Inverting outputs X = Total number of channels Y = Total number of reverse channels (right to left) U = Default and deglitch option B = Output default low, no deglitch E = Output default high, no deglitch F = Output default low, 36 ns deglitch H = Output default high, 36 ns deglitch V = Isolation rating C = 3.75 kV_{RMS}
Line 2 marking	TTTTTT	Manufacturing code from assembly house
Line 3 marking	YY	Year of manufacturing at assembly house
	WW	Work week of manufacturing at assembly house
Automotive-grade part numbers are indicated on the shipping label.		

11. Ordering Information

Industrial and Automotive Grade Ordering Part Numbers (OPNs)

Industrial-grade devices (part numbers having an "-I" in their suffix) are built using well controlled, high quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an "-A" in their suffix) are built using automotive-specific flows and additional statistical process controls at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listings. Automotive-Grade devices (with an "-A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with an "-I" suffix) version counterparts.

Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Refer to Top Marking section for the product decoder.

Table 22. Ordering Guide[1,2,3,4]

Ordering Part Numbers (OPNs)	Automotive OPNs[5]	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV_{RMS})	Package
Non-Inverting Output							
Si86S610BC-IS	Si86S610BC-AS	1	0	0	Low	3.75	NB SOIC-8
Si86S610BE-IS4	Si86S610BE-AS4	1	0	0	Low	6	SSO-8
Si86S610EC-IS	Si86S610EC-AS	1	0	0	High	3.75	NB SOIC-8
Si86S610EE-IS4	Si86S610EE-AS4	1	0	0	High	6	SSO-8
Si86S620BC-IS	Si86S620BC-AS	2	0	0	Low	3.75	NB SOIC-8
Si86S620BE-IS4	Si86S620BE-AS4	2	0	0	Low	6	SSO-8
Si86S620EC-IS	Si86S620EC-AS	2	0	0	High	3.75	NB SOIC-8
Si86S620EE-IS4	Si86S620EE-AS4	2	0	0	High	6	SSO-8
Si86S621BC-IS	Si86S621BC-AS	1	1	0	Low	3.75	NB SOIC-8
Si86S621BE-IS4	Si86S621BE-AS4	1	1	0	Low	6	SSO-8
Si86S621EC-IS	Si86S621EC-AS	1	1	0	High	3.75	NB SOIC-8
Si86S621EE-IS4	Si86S621EE-AS4	1	1	0	High	6	SSO-8
Si86S622BC-IS	Si86S622BC-AS	1	1	0	Low	3.75	NB SOIC-8
Si86S622BE-IS4	Si86S622BE-AS4	1	1	0	Low	6	SSO-8
Si86S622EC-IS	Si86S622EC-AS	1	1	0	High	3.75	NB SOIC-8
Si86S622EE-IS4	Si86S622EE-AS4	1	1	0	High	6	SSO-8
Si86S620FC-IS	Si86S620FC-AS	2	0	36	Low	3.75	NB SOIC-8
Si86S620FE-IS4	Si86S620FE-AS4	2	0	36	Low	6	SSO-8
Si86S620HC-IS	Si86S620HC-AS	2	0	36	High	3.75	NB SOIC-8
Si86S620HE-IS4	Si86S620HE-AS4	2	0	36	High	6	SSO-8
Si86S621FC-IS	Si86S621FC-AS	1	1	36	Low	3.75	NB SOIC-8
Si86S621FE-IS4	Si86S621FE-AS4	1	1	36	Low	6	SSO-8
Si86S621HC-IS	Si86S621HC-AS	1	1	36	High	3.75	NB SOIC-8
Si86S621HE-IS4	Si86S621HE-AS4	1	1	36	High	6	SSO-8

Table 22. Ordering Guide[1,2,3,4] (Continued)

Ordering Part Numbers (OPNs)	Automotive OPNs[5]	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Deglitch Filter Delay (ns)	Default Output State	Isolation Rating (kV_{RMS})	Package
Inverting Output							
Si86SO20BC-IS	Si86SO20BC-AS	2	0	0	Low	3.75	NB SOIC-8
Si86SO20BE-IS4	Si86SO20BE-AS4	2	0	0	Low	6	SSO-8
Si86SO20EC-IS	Si86SO20EC-AS	2	0	0	High	3.75	NB SOIC-8
Si86SO20EE-IS4	Si86SO20EE-AS4	2	0	0	High	6	SSO-8
Si86SO21BC-IS	Si86SO21BC-AS	1	1	0	Low	3.75	NB SOIC-8
Si86SO21BE-IS4	Si86SO21BE-AS4	1	1	0	Low	6	SSO-8
Si86SO21EC-IS	Si86SO21EC-AS	1	1	0	High	3.75	NB SOIC-8
Si86SO21EE-IS4	Si86SO21EE-AS4	1	1	0	High	6	SSO-8

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.
3. An “R” at the end of the part number denotes tape and reel packaging option.
4. Temperature range is –40 to 125 °C.
5. In the top markings of each device, the Manufacturing Code represented by “TTTTTT” contains, as its first character, a letter in the range N through Z to indicate Automotive-Grade.

12. Revision History

Revision	Date	Description
B	August, 2023	Corrected max PWD specifications in: "4. Electrical Specifications" on page 8. Added maximum ratings for output current in: Table 3, "Absolute Maximum Ratings," on page 8. Typo and formatting corrections made in: Table 12, "IEC 60747-17 Insulation Characteristics for Si86S61x/2x/Ox," on page 15 and Table 13, "UL 1577 Insulation Characteristics," on page 15.
A	April, 2023	Initial release.