SJA1105P/Q/R/S

5-port automotive Ethernet switch

Rev. 1 — 24 November 2017 Product data sheet

1 General description

The SJA1105P/Q/R/S safe and secure automotive gigabit Ethernet switch family extends the capabilities of the SJA1105/SJA1105T [1] switches with improved security-related features, extended interface options, and ISO 26262 ASIL-A compliance.

The SJA1105P/Q/R/S is a 5-port automotive Ethernet switch supporting IEEE Audio Video Bridging (AVB) and Time-Sensitive Networking (TSN) standards. Each of the five ports can be individually configured to operate at 10/100/1000 Mbit/s. This feature provides the flexibility to connect any Fast/Gigabit/optical PHY or MCU/MPU to any of the ports. Examples of external PHYs are the TJA1100 and TJA1102 IEEE 100BASE-T1 PHYs from NXP Semiconductors ([2] and [3]).

The new frame white/blacklisting, port-reachability and address learning restriction features, available on all SJA1105P/Q/R/S variants, improve switch security by limiting data processing to known frames and data sources and preventing the forwarding of erroneous or malicious data.

The updated MII/RMII/RGMII interfaces offer extended IO voltages such as 1V8 and 3V3 RGMII. Furthermore, the SGMII interface available on the /R and /S variants extends the connectivity options of the switch. The /P and /Q variants do not feature an SGMII port and remain 100 % pin-compatible with the SJA1105/SJA1105T switches.

The SJA1105P/Q/R/S switch family was developed according to the ISO 26262 standard. ASIL-A compliance reduces the safety-critical ECU design load. Additional documentation, including a safety manual, is available on request.

The switches are compatible with the IEEE AVB standard. The /Q and /S variants support extended TSN features such as 802.1Qbv. NXP-original AUTOSAR drivers and AVB SW stack are available for this series.

2 Features and benefits

2.1 General features

- 5-port store and forward architecture
- Each port individually configurable for 10/100 Mbit/s when operated as MII/RMII and 10/100/1000 Mbit/s when operated as RGMII or SGMII
- Independent I/O voltage domains: selectable 1.8/2.5/3.3 V operation for MII/RMII/RGMII; selectable 1.8/2.5/3.3 V for host interfacing; 1.2 V core voltage domains
- Small footprint: LFBGA159 (12 mm × 12 mm) package
- Automotive Grade 2 ambient operating temperature: -40 °C to +105 °C
- Automotive product qualification in accordance with AEC-Q100 Rev-H
- ISO-26262, ASIL-A

2.2 Ethernet switching and AVB features

- IEEE 802.3 compliant
- 128 kB frame buffer
- 1024 entry TCAM for collision-free MAC address learning
- 2 kB frame length handling
- IEEE 802.1Q defined tag support
- 4096 VLANs supported
- Egress tagging/untagging on a per-VLAN basis per port
- Priority-based QoS handling as specified in IEEE 802.1Q
- Per-port priority remapping and 8 configurable egress queues per port
- Optional double-tagging support
- Hardware support for IEEE 802.1AS timestamping and IEEE 802.1Qav AVB traffic shaping
- 16 credit-based shapers available according to IEEE 802.1Qav; shapers can be freely allocated to any priority queue on a per port basis
- Support for SR Class A, Class B, and Class C traffic
- IEEE 1588v2 one-step sync forwarding in hardware
- Frame mirroring and retagging for enhanced diagnostics
- Statistics for dropped frames and buffer load
- RFC2819 support for counters

2.3 Ethernet security

- IEEE 802.1X hardware support for EAP filtering, reachability and disabling address learning
- Extensive filtering rules for frame forwarding- Retagging/ Tunneling/ Double Tagging
- Address learning space can be configured for static and learned addresses
- Enhanced support for address learning restrictions for security
- Ingress rate-limiting on a per-port basis for Unicast/Multicast and Broadcast traffic
- Broadcast storm protection

2.4 TT and TSN features (SJA1105/Q/S only)

- IEEE 802.1Qbv time-aware traffic
- IEEE 802.1Qci per-stream policing (pre-standard)
- Support for ring-based redundancy (for time-triggered traffic only)
- 1024 deterministic Ethernet flows with per-flow based:
  - Time-triggered traffic transmission
  - Ingress policing and reception window check
  - Statistics

2.5 Interface features

- MII/RMII for interfacing with 10/100 Mbit/s PHYs/host processor (Fast Ethernet)
- RGMII for interfacing with 10/100/1000 Mbit/s PHYs/host processor/cascading (Gigabit Ethernet); internal delay for interface connection without external delay components

- SGMII for interfacing with 10/100/1000 Mbit/s PHYs/host processor/cascading
- MAC and PHY modes for interfacing (MII/RMII/RGMII/SGMII) directly with another switch or host processor
- Programmable drive strength for MII/RMII/RGMII interfaces
- SPI for host processor access

2.6 Other features

- 25 MHz system clock input from crystal oscillator or AC-coupled single-ended clock
- 25 MHz reference clock output
- Device reset input from host processor
- Synchronization output for cascading devices
- IEEE 1149.1/1149.6 compliant JTAG interface for TAP controller access and BSCAN

3 Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
SJA1105PEL [2]	LFBGA159	plastic low profile fine-pitch ball grid array package; 159 balls	SOT1427-1
SJA1105QEL [2]			
SJA1105REL			
SJA1105SEL			

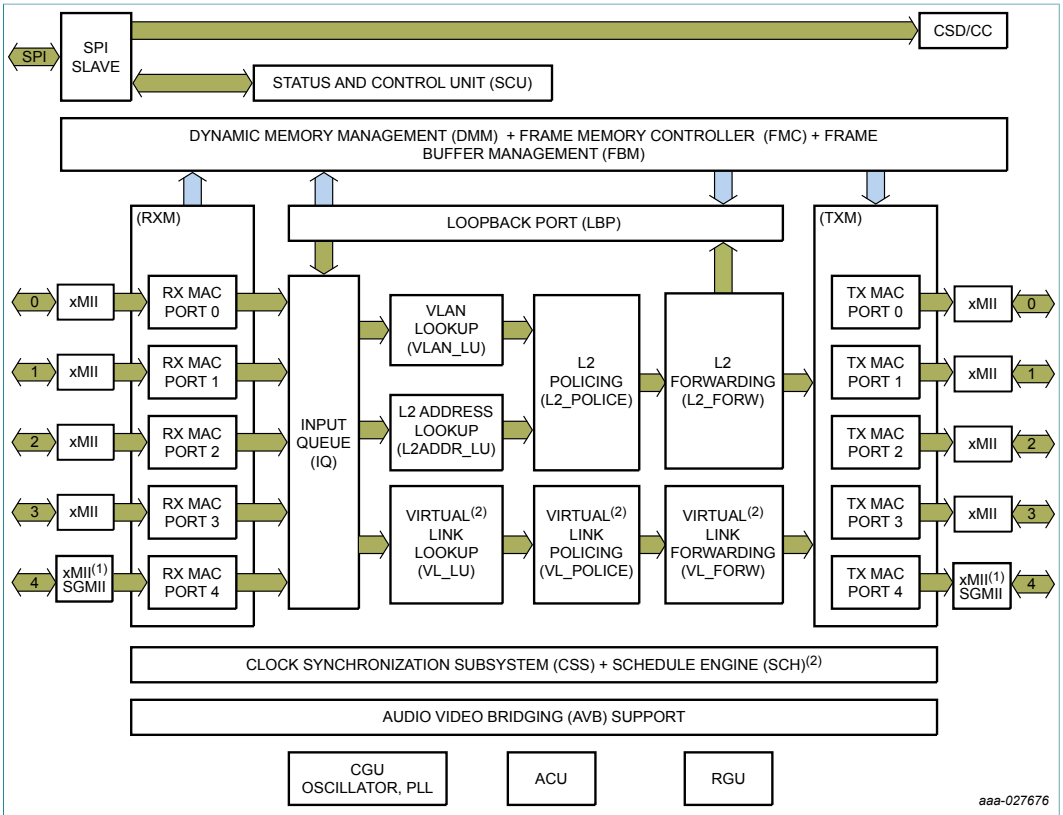
[1] 'EL' is the LFBGA159 package code.
[2] Pin compatible with SJA1105 and SJA1105T.

Table 2. SJA1105PQRS family overview

	MII/RMII/RGMII ports	SGMII ports	TSN/TTEthernet	RGMII-ID	TCAM
SJA1105P[1]	5	0	no	yes	yes
SJA1105Q[1]	5	0	yes	yes	yes
SJA1105R	4	1	no	yes	yes
SJA1105S	4	1	yes	yes	yes

[1] Pin compatible with SJA1105 and SJA1105T.

4 Block diagram



1. SGMII port in SJA1105R/S.
2. SJA1105Q/S only.

Figure 1. Block diagram

5 Pinning information

5.1 Pinning

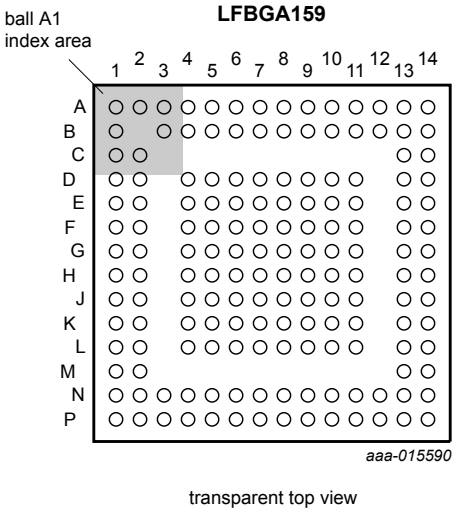


Figure 2. Pin configuration diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSS	MII0_ TXD0	MII0_ TX_ER	MII1_ RX_DV	MII1_ RXD2	MII1_ RXD0	MII1_ TX_CLK	MII1_ TXD3	MII1_ TXD1	MII1_ TX_ER	MII2_ RX_DV	MII2_ RXD2	MII2_ RXD0	VSS
B	MII0_ TXD1		MII1_ RX_ER	MII1_ RXD3	MII1_ RXD1	MII1_ RX_CLK	MII1_ TX_EN	MII1_ TXD2	MII1_ TXD0	MII2_ RX_ER	MII2_ RXD3	MII2_ RXD1	VSS	MII2_ RX_CLK
C	MII0_ TXD3	MII0_ TXD2											MII2_ TX_EN	MII2_ TX_CLK
D	MII0_ TX_CLK	MII0_ TX_EN		VDDIO_ MII0	VDDIO_ MII1	VDD_ CORE	VDDIO_ MII1	VDDIO_ MII1	VDD_ CORE	VDDIO_ MII2	VDDIO_ MII2		MII2_ TXD2	MII2_ TXD3
E	MII0_ RXD0	MII0_ RX_CLK		VDDIO_ MII0	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_ MII2		MII2_ TXD0	MII2_ TXD1
F	MII0_ RXD2	MII0_ RXD1		VDD_ CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ CORE		MII3_ RX_ER	MII2_ TX_ER
G	MII0_ RX_DV	MII0_ RXD3		VDDIO_ MII0	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_ MII3		MII3_ RXD3	MII3_ RX_DV
H	CLK_ OUT	MII0_ RX_ER		VDDIO_ CLO	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_ MII3		MII3_ RXD1	MII3_ RXD2
J	VDDA_ PLL	VSSA_ PLL		VDD_ CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ CORE		MII3_ RX_CLK	MII3_ RXD0
K	VDDA_ OSC	OSC_IN		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_ MII3		MII3_ TX_EN	MII3_ TX_CLK
L	OSC_ OUT	VSSA_ OSC		i.c.	VDDIO_ HOST	VDD_ CORE	VSS	VDDIO_ MII4	VDD_ CORE	VDDIO_ MII4	VDDIO_ MII4		MII3_ TXD2	MII3_ TXD3
M	TRST_N	TDI											MII3_ TXD0	MII3_ TXD1
N	TCK	VSS	TDO	PTP_ CLK	SDI	SS_N	MII4_ TXD1	MII4_ TXD3	MII4_ TX_CLK	MII4_ RXD0	MII4_ RXD2	MII4_ RX_DV	VSS	MII3_ TX_ER
P	VSS	TMS	RST_N	SDO	SCK	MII4_ TX_ER	MII4_ TXD0	MII4_ TXD2	MII4_ TX_EN	MII4_ RX_CLK	MII4_ RXD1	MII4_ RXD3	MII4_ RX_ER	VSS

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Figure 3. Pin configuration: SJA1105P and SJA1105Q

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSS	MII0_ TXD0	MII0_ TX_ER	MII1_ RX_DV	MII1_ RXD2	MII1_ RXD0	MII1_ TX_CLK	MII1_ TXD3	MII1_ TXD1	MII1_ TX_ER	MII2_ RX_DV	MII2_ RXD2	MII2_ RXD0	VSS
B	MII0_ TXD1		MII1_ RX_ER	MII1_ RXD3	MII1_ RXD1	MII1_ RX_CLK	MII1_ TX_EN	MII1_ TXD2	MII1_ TXD0	MII2_ RX_ER	MII2_ RXD3	MII2_ RXD1	VSS	MII2_ RX_CLK
C	MII0_ TXD3	MII0_ TXD2											MII2_ TX_EN	MII2_ TX_CLK
D	MII0_ TX_CLK	MII0_ TX_EN		VDDIO_ MII0	VDDIO_ MII1	VDD_ CORE	VDDIO_ MII1	VDDIO_ MII1	VDD_ CORE	VDDIO_ MII2	VDDIO_ MII2		MII2_ TXD2	MII2_ TXD3
E	MII0_ RXD0	MII0_ RX_CLK		VDDIO_ MII0	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_ MII2		MII2_ TXD0	MII2_ TXD1
F	MII0_ RXD2	MII0_ RXD1		VDD_ CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ CORE		MII3_ RX_ER	MII2_ TX_ER
G	MII0_ RX_DV	MII0_ RXD3		VDDIO_ MII0	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_ MII3		MII3_ RXD3	MII3_ RX_DV
H	CLK_ OUT	MII0_ RX_ER		VDDIO_ CLO	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_ MII3		MII3_ RXD1	MII3_ RXD2
J	VDDA_ PLL	VSSA_ PLL		VDD_ CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_ CORE		MII3_ RX_CLK	MII3_ RXD0
K	VDDA_ OSC	OSC_IN		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_ MII3		MII3_ TX_EN	MII3_ TX_CLK
L	OSC_ OUT	VSSA_ OSC		i.c.	VDDIO_ HOST	VDD_ CORE	VSS	VDD_ SGMII	VDD_ CORE	VDD_ SGMII	VDD_ SGMII		MII3_ TXD2	MII3_ TXD3
M	TRST_N	TDI											MII3_ TXD0	MII3_ TXD1
N	TCK	VSS	TDO	PTP_ CLK	SDI	SS_N	VSS	VDDA_ SGMII	VSS	SGMII_ RREF	VSS	VDDA_ SGMII	VSS	MII3_ TX_ER
P	VSS	TMS	RST_N	SDO	SCK	VSS	VSS	SGMII_ TXP	SGMII_ TXN	VSS	SGMII_ RXP	SGMII_ RXN	VSS	VSS

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Figure 4. Pin configuration: SJA1105R and SJA1105S

5.2 Pin description

Table 3. Pin description - xMII interface

Symbol	Pin					Type[1]	Description
	Ethernet port [2]						
	0	1	2	3	4 [3]		
VDDIO_MIIx	D4 E4 G4	D5 D7 D8	D10 D11 E11	G11 H11 K11	L8 L10 L11	P P P	3.3 V/2.5 V/1.8 V I/O supply voltages
TX_CLK/ REF_CLK/ TXC	D1	A7	C14	K14	N9	I/O I/O O	TX_CLK: MII interface transmit clock (also configurable as output) REF_CLK: RMII interface reference clock (also configurable as input) TXC: RGMII interface transmit clock
TX_EN/ TX_CTL	D2	B7	C13	K13	P9	O O	TX_EN: MII/RMII interface transmit enable output (active-HIGH) TX_CTL: RGMII interface transmit control output (active-HIGH)
TX_ER	A3	A10	F14	N14	P6	O	MII/RMII interface transmit coding error output (active-HIGH)
TXD0	A2	B9	E13	M13	P7	O	MII/RMII/RGMII interface transmit data output, bit 0
TXD1	B1	A9	E14	M14	N7	O	MII/RMII/RGMII interface transmit data output, bit 1
TXD2	C2	B8	D13	L13	P8	O	MII/RGMII interface transmit data output, bit 2
TXD3	C1	A8	D14	L14	N8	O	MII/RGMII interface transmit data output, bit 3
RX_CLK/ RXC	E2	B6	B14	J13	P10	I/O I	RX_CLK: MII interface receive clock (also configurable as output); RXC: RGMII interface receive clock
RX_ER	H2	B3	B10	F13	P13	I	MII/RMII interface receive error input (active-HIGH); must be connected to VSS if not used
RX_DV/ CRS_DV/ RX_CTL	G1	A4	A11	G14	N12	I I I	RX_DV: MII interface receive data valid input (active-HIGH); CRS_DV: RMII interface carrier sense/data valid input (active-HIGH) RX_CTL: RGMII interface receive control input (active-HIGH)
RXD0	E1	A6	A13	J14	N10	I	MII/RMII/RGMII interface receive data input, bit 0
RXD1	F2	B5	B12	H13	P11	I	MII/RMII/RGMII interface receive data input, bit 1
RXD2	F1	A5	A12	H14	N11	I	MII/RGMII interface receive data input, bit 2
RXD3	G2	B4	B11	G13	P12	I	MII/RGMII interface receive data input, bit 3

[1] I: digital input; O: digital output; P: power supply.
[2] MII/RMII/RGMII I/O pins are floating until the configuration is loaded and the interface is decided; all digital output pins are in "Fast speed mode" after reset unless otherwise indicated.
[3] MII/RMII/RGMII on port 4 available in SJA1105P/Q only. SJA1105R/S features a hardwired SGMII PHY on this port.

Table 4. Pin description - hardwired SGMII interface:SJA1105R/S

Symbol	Pin	Type[1]	Description
VDD_SGMII	L8, L10, L11	P	1.2 V core supply voltage for SGMII PHY (must be derived from the VDD_CORE supply)
VDDA_SGMII	N8, N12	P	2.5 V analog supply voltage for SGMII PHY
SGMII_RXN	P12	AI	SGMII differential receive negative [2]

Symbol	Pin	Type[1]	Description
SGMII_RXP	P11	AI	SGMII differential receive positive
SGMII_TXN	P9	AO	SGMII differential transmit negative [2]
SGMII_TXP	P8	AO	SGMII differential transmit positive
SGMII_RREF	N10	AO	SGMII calibration resistor output

[1] I: digital input; O: digital output; AI: analog input; AO: analog output; P: power supply.
[2] SGMII positive/negative polarities can be swapped in software to allow for MAC-MAC configurations.

Table 5. Pin description - core supply and ground

Symbol	Pin	Type[1]	Description
VDD_CORE	D6, D9, F4, F11, J4, J11, L6, L9	P	1.2 V core supply voltage
VSS	A1, A14, B13, E5, E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10,G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7,J8, J9, J10, K4, K5, K6, K7, K8, K9, K10, L7, N2, N13, P1, P14	G	supply ground (all variants)
	N7, N9, N11, P6, P7, P10, P13	G	supply ground (SJA1105R/S only)

[1] P: power supply; G: ground.

Table 6. Pin description - general

Symbol	Pin[1]	Type[2]	Description
RST_N	P3	I	reset input (active-LOW, hysteresis, VDDIO_HOST)
PTP_CLK	N4	I/O	sync in/out or PTP clock (if input: active-HIGH, VDDIO_HOST)
VDDIO_HOST	L5	P	host interface supply voltage for SPI, JTAG, CLK_OUT, PTP_CLK and RST_N (1.8 V, 2.5 V, 3.3 V)
i.c.	L4	G	internally connected; must be connected to ground
Clock generation (CGU)			
VDDA_OSC	K1	P	oscillator supply voltage (1.2 V)
VSSA_OSC	L2	G	oscillator supply ground
VDDA_PLL	J1	P	PLL supply voltage (1.2 V)
VSSA_PLL	J2	G	PLL supply ground
VDDIO_CLO	H4	P	clock output interface supply voltage (1.8 V, 2.5 V, 3.3 V)
CLK_OUT	H1	O	clock output (VDDIO_CLO)
OSC_IN	K2	AI	oscillator input
OSC_OUT	L1	AO	oscillator output
SPI interface			
SCK	P5	I	SPI clock (hysteresis, weak pull-down, VDDIO_HOST)
SDI	N5	I	SPI data input (hysteresis, weak pull-up, VDDIO_HOST)
SDO	P4	O	SPI data output (VDDIO_HOST)

Symbol	Pin[1]	Type[2]	Description
SS_N	N6	I	SPI slave select (hysteresis, weak pull-up, VDDIO_HOST)
JTAG interface			
TRST_N	M1	I	test reset (active LOW, hysteresis, weak pull-up, VDDIO_HOST)
TDI	M2	I	test data in (hysteresis, weak pull-up, VDDIO_HOST)
TCK	N1	I	test clock (hysteresis, weak pull-up, VDDIO_HOST)
TMS	P2	I	test mode select (hysteresis, weak pull-up, VDDIO_HOST)
TDO	N3	O	test data out (VDDIO_HOST)

[1] All digital output pins are in "Fast speed mode" after reset unless otherwise indicated.
[2] I: digital input; O: digital output; AI: analog input; AO: analog output; P: power supply; G: ground.

6 Functional description

The SJA1105P/Q/R/S is designed to provide a cost-optimized and flexible solution for automotive Ethernet switches. The SJA1105P/Q variants are feature-enhanced, drop-in replacements for the SJA1105/T. In the SJA1105R/S variants, one of the ports provides SGMII capability. These devices can be used in applications requiring SGMII connectivity with a host processor or where multiple devices need to be cascaded.

Each port can be independently configured for 10/100 Mbit/s MII/RMII or 10/100/1000 Mbit/s RGMII operation. The SGMII port on the SJA1105R/S can be configured for 10/100/1000 Mbit/s operation. An SPI-slave interface provides device register access to the host processor. A typical system diagram is shown in Figure 5.

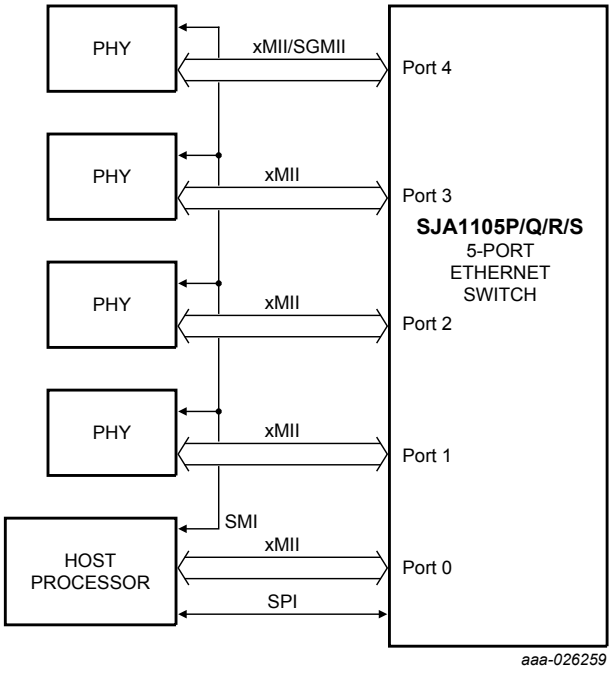


Figure 5. System diagram showing the SJA1105P/Q/R/S Ethernet switch connected to PHYs and a host processor. Port 4 is SGMII on SJA1105R/S

6.1 Functional overview

The SJA1105P/Q/R/S contains the following functional modules (see the block diagram in Figure 1):

6.1.1 Auxiliary Configuration Unit (ACU)

This module contains the pin configuration and status registers. The host can configure the I/O pads of the chip (pull-up/pull-down, speed etc.) and monitor the product configuration and temperature sensor status via these registers.

6.1.2 Clock Generation Unit (CGU)

This module contains the clock inputs, PLL and clock distribution for all internal blocks.

6.1.3 Reset Generation Unit (RGU)

This block resets all internal configuration registers to a pre-defined state at power-up.

6.1.4 Serial Peripheral Interface (SPI)

The host controller manages the device via the SPI.

6.1.5 Status and Control Unit (SCU)

This block contains the SJA1105PQRS status and configuration registers. The host processor accesses these registers via the SPI.

6.1.6 Configuration Stream Decoder/Configuration Controller (CSD/CC)

This block handles the distribution of the configuration stream from the host processor to other modules and performs a CRC check on the configuration blocks.

6.1.7 xMII

This block is a wrapper and multiplexer for the MII interface options. The device supports MII, RMII and RGMII. In the SJA1105R/S, port 4 is hard-wired for SGMII operation.

6.1.8 Dynamic Memory Management (DMM)/Frame Memory Controller (FMC)/ Frame Buffer Management (FBM)

These blocks deal with the storage and handling of frames in the memory buffer. The DMM provides memory handles for ingress frames and holds meta information related to the frames. The DMM releases frame handles for frames that are transmitted or dropped. The FMC converts frame handles into virtual memory addresses and the FBM optimizes the use of on-chip frame memory based on frame size.

6.1.9 Receive MAC (RXM)

The RXM loads the data from the xMII interface block and checks the IFG, the preamble, the SOF delimiter, the CRC and the frame length. It provides timestamps for clock synchronization frames, extracts frame metadata such as MAC addresses and VLAN information, and drops runt and oversized frames. The RXM collects memory handles from the DMM and transfers frame data to the FMC block for writing to memory.

6.1.10 Input Queue (IQ)

The IQ arranges the frame processing order so that the switching fabric behaves in a deterministic manner. If two ports receive an EOF during the same clock cycle, frames received on the port with the lower port ID are processed first.

The switch has a non-blocking, egress queue architecture. The input queue arbitrates access to the switching fabric and not to the egress ports.

6.1.11 VLAN Lookup (VLAN_LU)

The forwarding limitations and tagging/untagging options are determined in the VLAN_LU block.

6.1.12 Address Lookup (L2ADDR_LU)

The forwarding information for frames based on the destination MAC address in combination with the VLAN ID is determined in this block. The lookup table is addressed using a TCAM-based LUT. The table holds dynamically learned and statically configured entries. Dynamically learned entries can be configured to timeout. The address lookup process can be configured to use shared or independent address learning. The TCAM-based LUT can, additionally, be configured as a filter to determine subsequent action for frame processing.

6.1.13 Policing (L2_POLICE)

Ingress policing rules are enforced in the L2_POLICE block. The transmission rate can be limited for any of the eight priority levels and for broadcast traffic at each port. Non-compliant traffic is dropped and is indicated by associated flags and counters.

6.1.14 Forwarding (L2_FORW)

The L2_FORW block forwards frames to the destination ports. It maintains a vector of reachable ports for unicast traffic for each ingress port. In addition, it maintains a vector of destination ports for broadcast traffic and for unknown multicast traffic. This block also maintains a memory partition account for traffic received per port and drops frames if there is insufficient space. This block also handles priority remapping and egress queue priority mapping.

6.1.15 Transmit MAC (TXM)

This block handles frame output via the xMII interface. It supports eight priority queues and implements strict-priority scheduling. The AVB block can interrupt the scheduling from specific priority queues in case shapers are allocated to queues. When a frame is

selected for transmission, this block gets the frame data from the FMC using the memory handle of the frame. It passes the free memory handle back to the DMM once the frame has been transmitted. It also inserts VLAN tags into packet headers. It can be configured to perform the IEEE 1588v2 transparent clock update for sync frames.

6.1.16 Audio Video Bridging (AVB)

This block implements credit-based traffic shaping according to IEEE802.1Qav and interrupts transmission from priority queues in the TXM when necessary, to ensure that shaping occurs. It also captures high-resolution timestamps for IEEE 802.1AS and IEEE 1588v2 operation. The host processor can adjust the IEEE 1588v2 hardware clock via this block.

6.1.17 Loopback Port (LBP)

This block uses an internal port to replicate a frame internally and change the VLAN tag to support ingress and egress retagging of traffic. The replicated frame-handling information is fed back to the IQ which processes the frame in the same way as a frame from a regular traffic port.

6.1.18 Virtual Link Lookup (VL_LU); SJA1105Q/S only

The VL_LU block performs a lookup of time-triggered and rate-constrained traffic based on the configured Virtual Link Multicast addresses, the VLAN ID and the VLAN priority identifying time-triggered or rate-constrained traffic.

6.1.19 Virtual Link Policing (VL_POLICE); SJA1105Q/S only

The VL_POLICE block executes policing functions based on the time-triggered Ethernet or rate-constrained traffic rule set. Policing mechanisms can be configured individually per flow (i.e. per virtual link). Time-triggered Ethernet policing verifies that a frame received by the switch was sent at the correct point in time by the neighboring node. Non-compliant frames are dropped and are indicated by associated flags and counters.

6.1.20 Virtual Link Forwarding (VL_FORW); SJA1105Q/S only

The VL_FORW block forwards time-triggered or rate-constrained traffic to the destination ports. Time-triggered traffic is stored in this module until the running traffic schedule fires a transmit trigger for the respective Virtual Link. Rate-constrained traffic is immediately routed to the destination ports. All time-triggered frames are dropped if synchronization is lost.

6.1.21 Clock Synchronization Subsystem (CSS) and Schedule Engine (SCH); SJA1105Q/S only

This block implements the clock synchronization protocol and executes the message schedules.

6.2 Media Independent Interfaces (xMII)

The xMII interfaces can be configured to support a wide variety of PHYs and host controllers. Each port can be configured for MAC-to-PHY or MAC-to-MAC communication. The following configurations are supported:

MII: 25 MHz clock for 100 Mbit/s or 2.5 MHz for 10 Mbit/s operation, 14 interface signals, full duplex only [4]

RMII: 50 MHz clock for 100 Mbit/s and 10 Mbit/s operation, 8 interface signals (reference clock can be an input to both devices or may be driven from MAC to PHY), full duplex only [5]

RGMII: 125 MHz clock (both edges) for 1000 Mbit/s, 25 MHz for 100 Mbit/s or 2.5 MHz for 10 Mbit/s operation, 12 interface signals; full duplex only [6] [7]

SGMII: 1.25 Gbit/s LVDS for 10/100/1000 Mbit/s data transmission, 4 interface signals [8]

The interfaces can operate under the following conditions:

Table 7. Supported xMII interface operating conditions

Interface	I/O Voltage			I/O Slew Rate			
	1.8 V	2.5 V	3.3 V	High Speed	Fast Speed	Medium Speed	Slow Speed
MII	●	●	●	-	●	●	●
RMII	-	●	●	-	●	●	●
RGMII	●	●	●	●	●	-	-
SGMII	not applicable						

Depending on how the switch is configured, the following interface signals are available at each of the five ports (SGMII signals on SJA1105R/S port 4 are fixed and are not multiplexed):

Table 8. xMII pin multiplexing

MII (14 interface signals)	RMII (8 interface signals)	RGMII (12 interface signals)
TX_CLK	REF_CLK	TXC
TX_EN	TX_EN	TX_CTL
TX_ER [1]	TX_ER [1]	-
TXD0	TXD0	TXD0
TXD1	TXD1	TXD1
TXD2	-	TXD2
TXD3	-	TXD3
RX_CLK	-	RXC
RX_ER [1]	RX_ER [1]	-
RX_DV	CRS_DV	RX_CTL
RXD0	RXD0	RXD0
RXD1	RXD1	RXD1

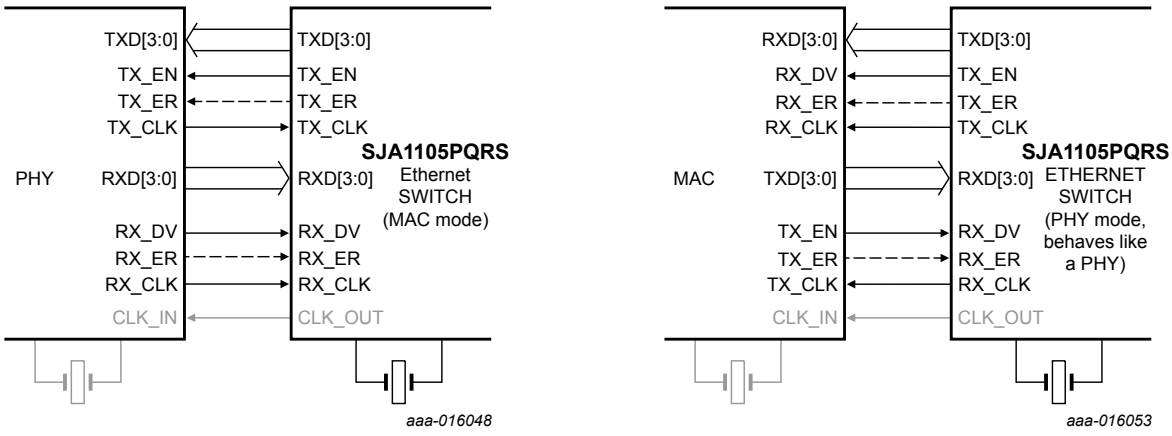
MII (14 interface signals)	RMII (8 interface signals)	RGMII (12 interface signals)
RXD2	-	RXD2
RXD3	-	RXD3

[1] TX_ER and RX_ER are optional; unused inputs must be connected to VSS.

6.2.1 MII signaling

Figure 6 shows the PHY-MAC (i.e. PHY to switch) and MAC-MAC (i.e. processor to switch) connections in an MII interface. Data is exchanged in 4-bit wide data nibbles TXD[3:0] and RXD[3:0]. Data transmission is synchronous with the transmit (TX_CLK) and receive (RX_CLK) clocks. For the PHY-MAC interface, both clock signals are provided by the PHY and are typically derived from an external crystal running at a nominal 25 MHz (±100 ppm) or from the CLK_OUT signal on the switch. When the Ethernet Switch is configured for MAC-MAC communication, the switch provides the clocks and acts like a PHY.

Note that RX_ER must be connected to VSS when not used.



a. PHY-MAC interface

b. MAC-MAC interface

Figure 6. MII interface connections

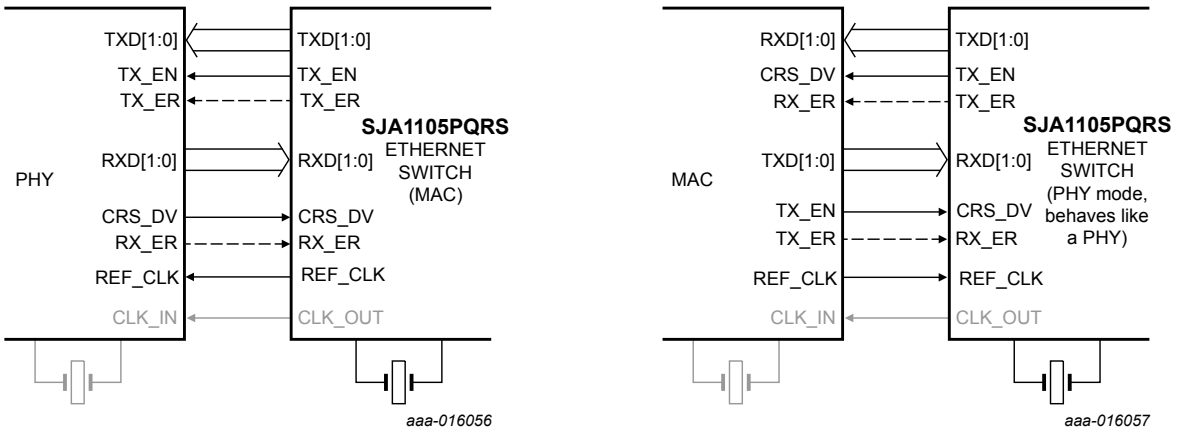
6.2.2 RMII signaling

RMII data is exchanged via 2-bit data signals TXD[1:0] and RXD[1:0] as shown in Figure 7. Transmit and receive signals are synchronized with the shared reference clock, REF_CLK.

In both the PHY-MAC (i.e. PHY to switch) and MAC-MAC (i.e. processor to switch) configurations, the REF_CLK output on the Ethernet switch can provide the shared reference clock.

To achieve the same data rate as MII, the interface is clocked at a nominal 50 MHz (±50 ppm) for 100 Mbit/s and 10 Mbit/s operation.

Note that RX_ER must be connected to VSS when not used.



a.PHY-MAC interface

b.MAC-MAC interface

Figure 7. RMII interface connections

6.2.3 RGMII signaling

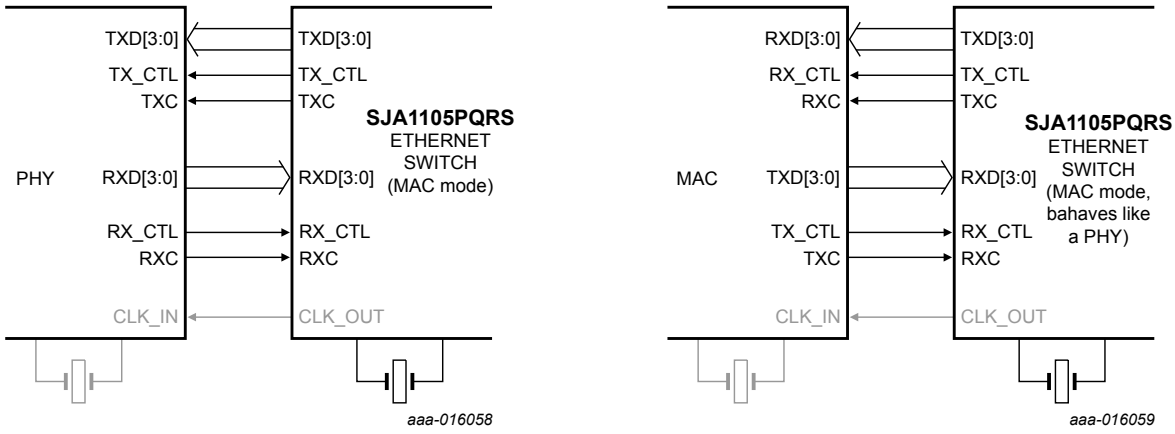
The PHY-MAC (i.e. PHY to switch) and MAC-MAC (i.e. processor to switch) connections in an RGMII-configured interface are shown in Figure 8. The RGMII protocol is intended to be an alternative to the IEEE 802.3z GMII standard (not supported on the SJA1105P/Q/R/S). The objective is to reduce the number of pins needed to connect the MAC and PHY in a cost-effective and technology-independent way. RGMII has the added advantage over RMII in that it supports Gigabit operation.

In order to achieve a reduced pin count, the number of data signals and associated control signals is reduced. Control signals are multiplexed together and transmitted data is synchronized with both clock edges (double data rate).

RGMII is a symmetrical interface. For 1000 Mbit/s, 100 Mbit/s and 10 Mbit/s operation, the clocks operate at 125 MHz, 25 MHz and 2.5 MHz (±50 ppm) respectively. The TXC signal is always generated by the MAC. The PHY generates the RXC.

Note that RGMII v1.3 [6] requires an external delay of between 1.5 ns and 2 ns on TXC and RXC. One of the enhancements in the SJA1105P/Q/R/S compared with the SJA1105/T is support for timing as defined in the RGMII v2.0 specification [7]. The updated version of the specification introduces an internal delay option, removing the need to implement an external delay.

The maximum interconnect delay is limited to 1 ns. Therefore, the maximum supported trace length is approximately 15 cm.



a.PHY-MAC interface

b.MAC-MAC interface

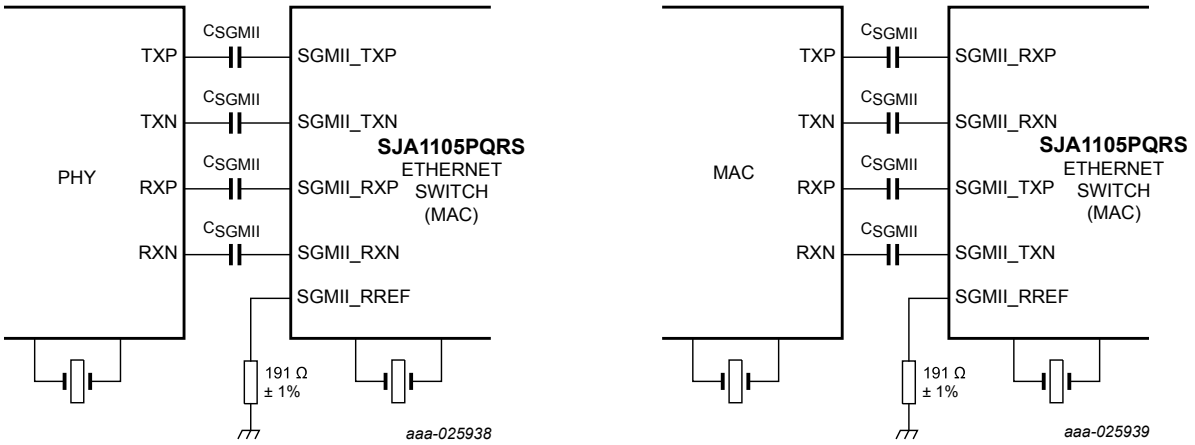
An optional integrated delay on TXC and RXC is available in the SJA1105P/Q/R/S

Figure 8. RGMII interface connections

6.2.4 SGMII signaling

The PHY-MAC (i.e. PHY to switch) and MAC-MAC (i.e. processor to switch) connections on an SGMII-configured interface are shown in Figure 9. The SGMII protocol [8] is intended as an alternative to the RGMII standard. It uses fewer interface signals and provides better EMC performance. Port 4 on SJA1105R/S is an SGMII 4-wire interface. It implements clock data recovery so no additional clock pairs are needed (6-wire interface is not supported). SGMII must always be AC coupled with a capacitor (C_{SGMII}, 100 nF). The SJA1105R/S is AC-compliant with the SGMII specification. For SGMII operation, an external calibration resistor (191 Ω ±1 %) must be connected to SGMII_RREF.

The SGMII interface implements (optional) Auto-Negotation. In this mode, PHY and MAC handshake the supported interface capabilities to determine optimal operating conditions. SGMII Auto-Negotiation can be disabled to force the interface into the desired operating mode to improve the start-up time.



a.PHY-MAC interface

b.MAC-MAC interface

Figure 9. SGMII 4-wire interface connections

6.3 SPI interface

The SJA1105P/Q/R/S provides an SPI bus slave as the host control interface. The host can control/configure the SJA1105P/Q/R/S by accessing the configuration address space and the programming address space.

This interface acts as a slave in a synchronous serial data link that conforms with the SPI standard as defined in the SPI Block Guide from Motorola [9]. The interface operates in SPI Transfer mode 1 (CPOL = 0, CPHA = 1).

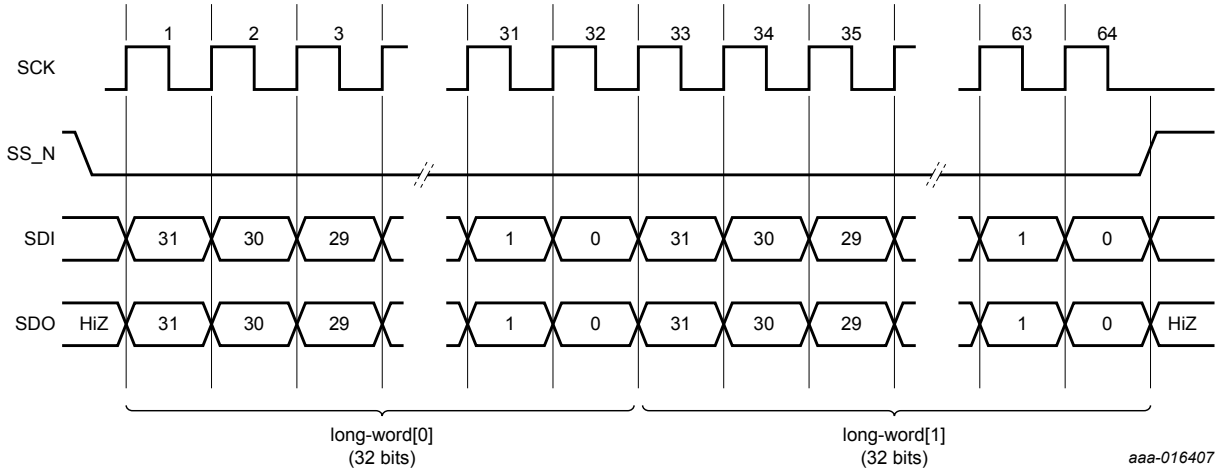


Figure 10. SPI transfer timing (example)

An example SPI timing diagram is shown in Figure 10. Data is captured on the falling edge of the clock and transmitted on the rising edge. Both master and slave must operate in the same mode.

After the SS_N signal has been asserted, the SPI clock signal (SCK) must be stable for at least 40 ns before being asserted. At the end of the SPI transaction, the SPI clock signal (SCK) must be stable for at least 40 ns before the SS_N signal is de-asserted.

The SPI clock signal (SCK) must be stable for at least half a clock period between the reception of on the SDI input and the transmission on the SDO output.

When CGU registers are read, a 64 ns delay must be inserted between the control and data phases to allow the device to retrieve the data. Alternatively, the access can be performed at a frequency below 17.8 MHz. In addition, a read-after-write time of >130 ns between an SPI write and read transaction to the same register must be guaranteed. See the SJA1105P/Q/R/S software user manuals [10] for further details on the data format.

The number of SPI clock cycles must be between 64 and 2080 and be a multiple of 32. In order to ensure support for a wide a range of microcontrollers, the SPI interface can operate at a supply voltage of 3.3 V, 2.5 V or 1.8 V (determined by the voltage connected to VDDIO_HOST).

7 Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(osc)}$	oscillator analog supply voltage		-0.5	+1.6	V
$V_{DDA(PLL)}$	PLL analog supply voltage		-0.5	+1.6	V
V_{DDC}	core supply voltage		-0.5	+1.6	V
$V_{DD(host)}$	host supply voltage		-0.5	+5	V
$V_{DD(clk)}$	clock supply voltage		-0.5	+5	V
$V_{DD(MII)}$	MII supply voltage		-0.5	+5	V
$V_{DDA(SGMII)}$	SGMII analog supply voltage		-0.5	+5	V
$V_{DDD(SGMII)}$	SGMII digital supply voltage		-0.5	+1.6	V
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM); 100 pF, 1.5 kΩ [1]	-2000	+2000	V
		Charged Device Model (CDM) [2]			
		corner balls	-750	+750	V
		other balls	-500	+500	V
T_j	junction temperature		-40	+125	°C
T_{stg}	storage temperature		-55	+150	°C

[1] According to AEC-Q100-002.
[2] According to AEC-Q100-011.

8 Thermal characteristics

Table 10. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer board (JESD51-9); 20 % PCB metalization	24.0	K/W
$R_{th(j-lead)}$	thermal resistance from junction to lead		12.3	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		0.4	K/W

9 Static characteristics

Table 11. Static characteristics

T_j = -40 °C to +125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltages; see Figure 20						
Clock and host interface supply (pins VDDIO_CLO and VDDIO_HOST)						
$V_{DD(clk)}$	clock supply voltage	3.3 V signaling	3.00	3.30	3.60	V
		2.5 V signaling	2.30	2.50	2.70	V
		1.8 V signaling	1.65	1.80	1.95	V
$V_{DD(host)}$	host supply voltage	3.3 V signaling	3.00	3.30	3.60	V
		2.5 V signaling	2.30	2.50	2.70	V
		1.8 V signaling	1.65	1.80	1.95	V
MII/RMII/RGMII interface supply (pins VDDIO_MII0 to VDDIO_MII4)						
$V_{DD(MII)}$	MII supply voltage	3.3 V signaling	3.00	3.30	3.60	V
		2.5 V signaling	2.30	2.50	2.70	V
		1.8 V signaling	1.65	1.80	1.95	V
SGMII interface supply (pins VDD_SGMII and VDDA_SGMII)						
$V_{DDA(SGMII)}$	SGMII analog supply voltage		2.3	2.5	2.7	V
$V_{DDD(SGMII)}$	SGMII digital supply voltage		1.14	1.2	1.32	V
Core, oscillator and PLL supply (pins VDD_CORE, VDDA_OSC and VDDA_PLL)						
V_{DDC}	core supply voltage	see Figure 20	1.14	1.2	1.32	V
$V_{DDA(osc)}$	oscillator analog supply voltage		1.1	1.2	1.3	V
$V_{DDA(PLL)}$	PLL analog supply voltage		1.1	1.2	1.3	V
Supply currents						
Clock and host interface supply (pins VDDIO_CLO and VDDIO_HOST)						
$I_{DD(host)RMS}$	host supply current (RMS)	SPI running at 25 MHz; JTAG port at 16 MHz; C_L = 25 pF				
		$V_{DD(host)}$ = 3.30 V	-	-	2.1	mA
		$V_{DD(host)}$ = 2.50 V	-	-	1.6	mA
		$V_{DD(host)}$ = 1.80 V	-	-	1.2	mA
$I_{DD(clk)RMS}$	clock supply current (RMS)	C_L = 25 pF				
		$V_{DD(clk)}$ = 3.30 V	-	-	3.9	mA
		$V_{DD(clk)}$ = 2.50 V	-	-	3.0	mA
		$V_{DD(clk)}$ = 1.80 V	-	-	2.2	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MII interface supply (pins VDDIO_MII0 to VDDIO_MII4)						
$I_{DD(MII)RMS}$	MII supply current (RMS)	MII-PHY mode at 100 Mbit/s; C_L = 29 pF; worst-case alternating data pattern				
		3.3 V operation	-	-	15.4	mA
		2.5 V operation	-	-	11.6	mA
		1.8 V operation	-	-	8.4	mA
		RMII-MAC mode at 100 Mbit/s; C_L = 29 pF; worst-case alternating data pattern				
		3.3 V operation	-	-	15.8	mA
		2.5 V operation	-	-	11.9	mA
		RGMII mode at 1 Gbit/s; C_L = 22 pF; worst-case alternating data pattern				
		3.3 V operation	-	-	84	mA
		2.5 V operation	-	-	63.1	mA
		1.8 V operation	-	-	45.6	mA
SGMII interface supply (pins VDD_SGMII and VDDA_SGMII)						
$I_{DDA(SGMII)RMS}$	SGMII analog supply current (RMS)		-	20.2	-	mA
$I_{DDD(SGMII)RMS}$	SGMII digital supply current (RMS)		-	17.6	-	mA
Core, oscillator and PLL supply (pins VDD_CORE, VDDA_OSC and VDDA_PLL)						
I_{DDC}	core supply current		-	-	200	mA
$I_{DDA(PLL)}$	PLL analog supply current	single-phase per PLL	-	-	1.2	mA
		multi-phase per PLL	-	-	1.6	mA
$I_{DDA(osc)}$	oscillator analog supply current	slave mode; 25 MHz input clock	-	700	-	µA
		oscillation mode; 25 MHz crystal	-	350	-	µA
$I_{startup(osc)}$	oscillator start-up current		0.2	1.0	2.5	mA
Power-On Reset (POR)						
$V_{trip(POR)}$	power-on reset trip voltage	HIGH level	0.65	0.76	1.01	V
		LOW level	0.60	0.72	0.91	V
Oscillator (pins OSC_IN and OSC_OUT)						
Crystal oscillator mode						
C_{shunt}	shunt capacitance		-	-	7	pF
$C_{L(ext)}$	external load capacitance	per pin [1]	-	10	-	pF
Clock mode						
$C_{cpl(ext)}$	external coupling capacitor		-	100	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(OSC\_IN)}$	input voltage on pin OSC_IN	RMS value	0.20	-	$V_{DDA(OSC)}$	V
I/O pins						
pins SPI, JTAG, CLK_OUT, PTP_CLK, RST_N						
V_{IH}	HIGH-level input voltage	3.3 V signaling	2.0	-	VDDx + 0.5[2]	V
		2.5 V signaling	1.7	-	VDDx + 0.5[2]	V
		1.8 V signaling	0.65 ×V_{DDx}[2]	-	V_{DDx} +0.5[2]	V
V_{IL}	LOW-level input voltage	3.3 V signaling	-0.5	-	+0.8	V
		2.5 V signaling	-0.5	-	+0.7	V
		1.8 V signaling	-0.5	-	0.35 ×V_{DDx}[2]	V
V_{OH}	HIGH-level output voltage	3.3 V signaling	2.8	-	3.4	V
		2.5 V signaling	2.1	-	2.5	V
		1.8 V signaling	1.4	-	1.8	V
V_{OL}	LOW-level output voltage	3.3 V signaling	0.19	-	0.25	V
		2.5 V signaling	0.19	-	0.25	V
		1.8 V signaling	0.19	-	0.25	V
$V_{hys(i)}$	input hysteresis voltage	CFG_PAD_xxx[yyy_IH] = 1; see [Ref. 8]	0.1 × V_{DDx}[2]	-	-	V
$R_{pu(weak)}$	weak pull-up resistance		40	50	57	kΩ
$R_{pd(weak)}$	weak pull-down resistance		40	50	57	kΩ
I_{OSH}	HIGH-level short-circuit output current		-	-	-111.7	mA
I_{OSL}	LOW-level short-circuit output current		-	-	110.2	mA
C_i	input capacitance	1.8 V signaling	-	-	5	pF
Z_o	output impedance		40.0	-	67.5	Ω
RGMII/RMII/MII interface: pins TX_CLK, TX_EN, TX_ER, TXDx, RX_CLK, RX_ER, RX_DV, RXDx						
C_i	input capacitance		-	-	5	pF
Z_o	output impedance	1.8 V signaling				
		low/medium/fast speed mode	36	-	60	Ω
		high-speed mode	26	-	45	Ω
		2.5 V signaling				
		low/medium/fast speed mode	35	-	53	Ω
		high-speed mode	26	-	40	Ω
		3.3 V signaling				
		low/medium/fast speed mode	34	-	50	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		high-speed mode	25	-	38	Ω
V_{IH}	HIGH-level input voltage	3.3 V signaling	2.0	-	$V_{DD(MIIx)}$ + 0.5[3]	V
		2.5 V signaling	1.7	-	$V_{DD(MIIx)}$ + 0.5[3]	V
		1.8 V signaling	0.65 × $V_{DD(MIIx)}$[3]	-	$V_{DD(MIIx)}$ + 0.5[3]	V
V_{IL}	LOW-level input voltage	3.3 V signaling	-0.5	-	+0.8	V
		2.5 V signaling	-0.5	-	+0.7	V
		1.8 V signaling	-0.5	-	+0.35 × $V_{DD(MIIx)}$[3]	V
V_{OH}	HIGH-level output voltage	I_O = 4 mA				
		3.3 V signaling	2.8	-	3.5	V
		2.5 V signaling	2.1	-	2.6	V
		1.8 V signaling	1.4	-	1.8	V
V_{OL}	LOW-level output voltage	I_O = 4 mA				
		3.3 V signaling	0.1	-	0.2	V
		2.5 V signaling	0.1	-	0.2	V
		1.8 V signaling	0.1	-	0.2	V
$V_{hys(i)}$	input hysteresis voltage	CFG_PAD_xxx[yyy_IH] = 1; see [Ref. 8]	0.1 × $V_{DD(MIIx)}$[3]	-	-	V
I_{OSH}	HIGH-level short-circuit output current	1.8 V signaling				
		low/medium/fast speed mode	-	-	-51	mA
		high-speed mode	-	-	-68	mA
		2.5 V signaling				
		low/medium/fast speed mode	-	-	-78	mA
		high-speed mode	-	-	-104	mA
		3.3 V signaling				
		low/medium/fast speed mode	-	-	-118	mA
		high-speed mode	-	-	-157	mA
I_{OSL}	LOW-level short-circuit output current	1.8 V signaling				
		low/medium/fast speed mode	-	-	54	mA
		high-speed mode	-	-	72	mA
		2.5 V signaling				
		low/medium/fast speed mode	-	-	81	mA
		high-speed mode	-		108	mA
		3.3 V signaling				
		low/medium/fast speed mode	-	-	118	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		high-speed mode	-	-	157	mA
SGMII port; symbol and parameter formats in this section are taken from the SGMII specification [Ref. 6]						
$C_{cpl(ext)}$	external coupling capacitor		-	100	-	nF
$R_{cal(SGMII)}$	SGMII calibration resistor	1 % tolerance, 20 mW	-	191	-	Ω
SGMII transmitter						
V_{ring}	output ringing	de-emphasis disabled	-	-	10	%
$\|V_{OD}\|$	output differential voltage	programmable	250	350	500	mV
$\Delta V_{O(dif)}$	differential output voltage variation	between 0 and 1	-	-	10	%
Vos	output offset voltage	[4]	400	500	600	mV
R_o	output impedance (single-ended)		40	50	60	Ω
ΔR_o	mismatch in a pair	between SGMII_TXP and SGMII_TXN	-	-	10	%
I_{sa}, I_{sb}	output current on short to GND		4.5	-	14.8	mA
I_{sab}	output current when a, b are shorted		6.4	-	7.3	mA
SGMII receiver						
V_{idth}	input differential threshold		-	-	87.5	mV
$V_{I(cm)}$	common-mode input voltage	[4]	-	0	-	mV
V_{hyst}	input differential hysteresis		-	0	-	mV
R_{in}	receiver differential input impedance		80	100	120	Ω
Temperature sensor						
|TE|	temperature error (absolute value)		-	2	10	°C
T_{res}	temperature resolution		3	4.77	7	°C
$\Delta T_{sen(range)}$	temperature sensor detection range		-40	-	135	°C

[1] Value is crystal-dependent.
[2] V_{DDx} is $V_{DD(host)}$ for pins SPI, JTAG, PTP_CLK and RST_N; V_{DDx} is $V_{DD(clk)}$ for pin CLK_OUT (see Figure 17).
[3] $V_{DD(MIIx)}$ is the filtered supply voltage for pin VDDIO_MIIx (see Figure 17).
[4] AC-compliant, but not DC-compliant with the SGMII specification.

10 Dynamic characteristics

Table 12. Dynamic characteristics

T_j = -40 °C to +125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rise and fall times						
I/O pins (SPI, JTAG, CLK_OUT, PTP_CLK)		10 cm PCB trace: 50 Ω; $C_{L(trace)}$ = 14 pF; 5 pF far end load				
$t_{r(o)}$	output rise time	3.3 V signaling				
		high-speed mode	0.3	-	0.8	ns
		fast-speed mode	0.5	-	1.3	ns
		medium-speed mode	0.8	-	2.0	ns
		low-speed mode	1.4	-	2.7	ns
		2.5 V signaling				
		high-speed mode	0.3	-	1.1	ns
		fast-speed mode	0.6	-	1.7	ns
		medium-speed mode	1.1	-	2.4	ns
		low-speed mode	1.8	-	3.1	ns
		1.8 V signaling				
		high-speed mode	0.5	-	1.9	ns
		fast-speed mode	0.9	-	2.5	ns
		medium-speed mode	1.5	-	3.2	ns
		low-speed mode	2.2	-	4.1	ns
$t_{f(o)}$	output fall time	3.3 V signaling				
		high-speed mode	0.5	-	1.0	ns
		fast-speed mode	0.5	-	1.0	ns
		medium-speed mode	0.6	-	1.8	ns
		low-speed mode	1.2	-	2.7	ns
		2.5 V signaling				
		high-speed mode	0.5	-	0.9	ns
		fast-speed mode	0.4	-	1.4	ns
		medium-speed mode	0.9	-	2.0	ns
		low-speed mode	1.5	-	3.0	ns
		1.8 V signaling				
		high-speed mode	0.4	-	1.6	ns
		fast-speed mode	0.6	-	2.3	ns
		medium-speed mode	1.3	-	3.0	ns
		low-speed mode	1.9	-	3.9	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RGMII/RMII/MII interface: pins TX_CLK, TX_EN, TX_ER, TXDx, RX_CLK, RX_ER, RX_DV, RXDx; 10 cm PCB trace: 50 Ω; $C_{L(trace)}$ = 21 pF; 5 pF far end load						
$t_{r(o)}$	output rise time	3.3 V signaling				
		high-speed mode	0.2	-	0.5	ns
		fast-speed mode	0.3	-	0.65	ns
		medium-speed mode	0.3	-	0.8	ns
		low-speed mode	0.5	-	1.6	ns
		2.5 V signaling				
		high-speed mode	0.2	-	0.5	ns
		fast-speed mode	0.3	-	0.75	ns
		medium-speed mode	0.3	-	1.0	ns
		low-speed mode	0.9	-	2.3	ns
		1.8 V signaling				
		high-speed mode	0.25	-	0.75	ns
		fast-speed mode	0.3	-	0.9	ns
		medium-speed mode	0.5	-	1.6	ns
		low-speed mode	1.8	-	3.4	ns
$t_{f(o)}$	output fall time	3.3 V signaling				
		high-speed mode	0.3	-	0.5	ns
		fast-speed mode	0.3	-	0.65	ns
		medium-speed mode	0.3	-	0.6	ns
		low-speed mode	0.5	-	1.6	ns
		2.5 V signaling				
		high-speed mode	0.25	-	0.5	ns
		fast-speed mode	0.3	-	0.75	ns
		medium-speed mode	0.3	-	0.8	ns
		low-speed mode	0.6	-	2.1	ns
		1.8 V signaling				
		high-speed mode	0.25	-	0.75	ns
		fast-speed mode	0.3	-	0.7	ns
		medium-speed mode	0.4	-	1.3	ns
		low-speed mode	1.2	-	3.0	ns
Oscillator (pins OSC_IN and OSC_OUT)						
Crystal oscillator mode [1]						
f_{xtal}	crystal frequency		-	25	-	MHz
$t_{startup}$	start-up time	25 MHz crystal; $C_{L(ext)}$ = 10 pF	-	275	800	µs
δ	duty cycle		45	50	55	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{jit(RMS)}$	RMS period jitter time		-	2.6	4	ps
$N_{cy(clk)startup}$	number of start-up clock cycles	until clock is stable;25 MHz crystal;$C_{L(ext)}$ = 8 pF (OSC_IN,OSC_OUT)	-	1000	-	-
Clock mode						
$f_{clk(i)}$	input clock frequency		-	25	-	MHz
$N_{cy(clk)startup}$	number of start-up clock cycles	until clock is stable	-	10	-	-
PLLs						
$t_{(startup)}$	start-up time		-	-	200	µs
$t_{jit(p-p)}$	peak-to-peak jitter		-	-	300	ps
pin RST_N						
t_w	pulse width		5.0	-	-	µs
$t_{(rst-startup)}$	start-up time after reset	until the device is responsive to SPI commands				
		software cold start (from write to RESET_CTRL register)	-	329	-	µs
		software warm start (from write to RESET_CTRL register)	-	2	-	µs
		external reset; from de-activation (rising edge) of RST_N	-	329	-	µs
		POR reset; from VDD_CORE = $V_{trip(POR)}$ HIGH	-	371	-	µs
pin CLK_OUT						
f_{clk}	clock frequency		-	25	-	MHz
δ	duty cycle		40	50	60	%
SPI: pins SS_N, SCK, SDI and SDO						
f_{clk}	clock frequency		0.1	-	25	MHz
δ	duty cycle		45	50	55	%
$t_{su(D)}$	data input set-up time	w.r.t. SCK sampling edge	12.4	-	-	ns
$t_{h(D)}$	data input hold time	w.r.t. SCK sampling edge	18	-	-	ns
$t_{d(clk-data)}$	clock to data delay time	w.r.t. SCK launching edge;high-speed mode; 25 pF load	0	-	14	ns
$t_{SPILEAD}$	SPI enable lead time		40	-	-	ns
t_{SPILAG}	SPI enable lag time		40	-	-	ns
t_{SPIDV}	SPI enable to output data valid time		$0.5T_{clk}$	-	-	ns
$t_{d(W-R)}$	write to read delay time		130	-	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(ctrl-data)}$	control to data delay time		64	-	-	ns
JTAG: pins TRST_N, TDI, TCK, TMS and TDO						
f_{clk}	clock frequency	V_{VDDIO_HOST} = 2.5 V or 3.3 V	0.1	-	16	MHz
		V_{VDDIO_HOST} = 1.8 V	0.1	-	14	MHz
δ	duty cycle	V_{VDDIO_HOST} = 1.8 V, 2.5 V or 3.3 V	40	50	60	%
t_w	pulse width	on pin TRST_N	100	-	-	ns
$t_{su(D)}$	data input set-up time	w.r.t. TCK sampling edge	4	-	-	ns
$t_{h(D)}$	data input hold time	w.r.t. TCK sampling edge	25	-	-	ns
$t_{d(clk-data)}$	clock to data delay time	w.r.t. TCK launching edge;high-speed mode; 25 pF load	0	-	20	ns
MII, RMII and RGMII ports						
MII MAC						
f_{clk}	clock frequency	transmit (TX_CLK) and receive (RX_CLK) clocks; 100 Mbit/s operating speed	-	25	-	MHz
δ	duty cycle	of transmit and receive clocks	35	50	65	%
$t_{su(D)}$	data input set-up time	on pins RXDx, RX_DV and RX_ER w.r.t. rising edge on RX_CLK	10	-	-	ns
$t_{h(D)}$	data input hold time	on pins RXDx, RX_DV and RX_ER w.r.t. rising edge on RX_CLK	10	-	-	ns
$t_{d(clk-data)}$	clock to data delay time	on pins TXDx, TX_EN and TX_ER w.r.t. rising edge on TX_CLK	0	-	25	ns
MII PHY (reverse MII)						
f_{clk}	clock frequency	transmit (TX_CLK) and receive (RX_CLK) clocks; 100 Mbit/s operating speed	-	25	-	MHz
δ	duty cycle	of transmit and receive clocks	35	50	65	%
$t_{su(D)}$	data input set-up time	on pins RXDx, RX_DV and RX_ER w.r.t. rising edge on RX_CLK	10	-	-	ns
$t_{h(D)}$	data input hold time	on pins RXDx, RX_DV and RX_ER w.r.t. rising edge on RX_CLK	0	-	-	ns
$t_{d(clk-data)}$	clock to data delay time	on pins TXDx, TX_EN and TX_ER w.r.t. rising edge on TX_CLK	12	-	25	ns
RMII						
f_{clk}	clock frequency	reference clock (REF_CLK); 100 Mbit/s operating speed	-	50	-	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
δ	duty cycle	of REF_CLK	35	50	65	%
$t_{su(D)}$	data input set-up time	on pins RXDx, CRS_DV and RX_ER w.r.t. rising edge on REF_CLK	4	-	-	ns
$t_{h(D)}$	data input hold time	on pins RXDx, CRS_DV and RX_ER w.r.t. rising edge on REF_CLK	0	-	-	ns
$t_{d(clk-data)}$	clock to data delay time	on pins RXDx, CRS_DV and RX_ER w.r.t. rising edge on REF_CLK; fast speed I/O setting	2	-	10	ns
RGMII; symbol and parameter formats in this section taken from the RGMII specification [Ref. 5]						
f_{clk}	clock frequency	transmit (TXC) and receive (RXC)clocks				
		1 Gbit/s operating speed	-	125	-	MHz
		100 Mbit/s operating speed	-	25	-	MHz
		10 Mbit/s operating speed	-	2.5	-	MHz
δ	duty cycle	of transmit and receive clocks				
		1 Gbit/s operating speed	45	50	55	%
		100/10 Mbit/s operating speed	40	50	60	%
$t_{sk(o)}$	output skew time	at the transmitter w.r.t. edge on TXC; RGMII rev1.3	-0.5	-	+0.5	ns
$t_{sk(I)}$	input skew time	at the receiver w.r.t. edge on TXC; RGMII rev1.3	1.0	-	2.6	ns
T_{setup_T}	data to clock output setup time	at transmitter; RGMII rev 2.0 (internal delay)	1.2	2.0	-	ns
T_{hold_T}	clock to data output hold time	at transmitter; RGMII rev 2.0 (internal delay)	1.2	2.0	--	ns
T_{setupt_R}	clock to data input set-up time	at receiver; RGMII rev 2.0 (internal delay)	1.0	2.0	-	ns
T_{hold_R}	clock to data input hold time	at receiver; RGMII rev 2.0 (internal delay)	1.0	2.0	-	ns
SGMII port; symbol and parameter formats in this section are taken directly from the SGMII specification [Ref. 6]						
Transmitter						
t_r	rise time	20 % to 80 %	65	-	275	ps
t_f	fall time	80 % to 20 %	65	-	275	ps
$\Delta t_{risefall}$	difference between differential rise and fall time		-	-	20	%
t_{skew}	skew time	between two members of a differential pair; skew measured at 50 % of transition	-	20	-	ps
ΔV_{OS}	TX AC offset/common-voltage variation		-	-	50	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DJ	TX deterministic jitter		-	-	51.4	ps
RJ	TX random jitter		-	-	7.4	ps
Receiver						
$V_{icm(tol)}$	input common mode voltage noise tolerance	noise frequency 2 MHz to 200 MHz	-	150	-	mV
J_{TOL}	RX jitter tolerance	$V_{i(dif)}$ = 80 mV (p-p)	-	-	400	ps

[1] A 100 ppm crystal is needed for MII and a 50 ppm crystal for RMII/RGMII.

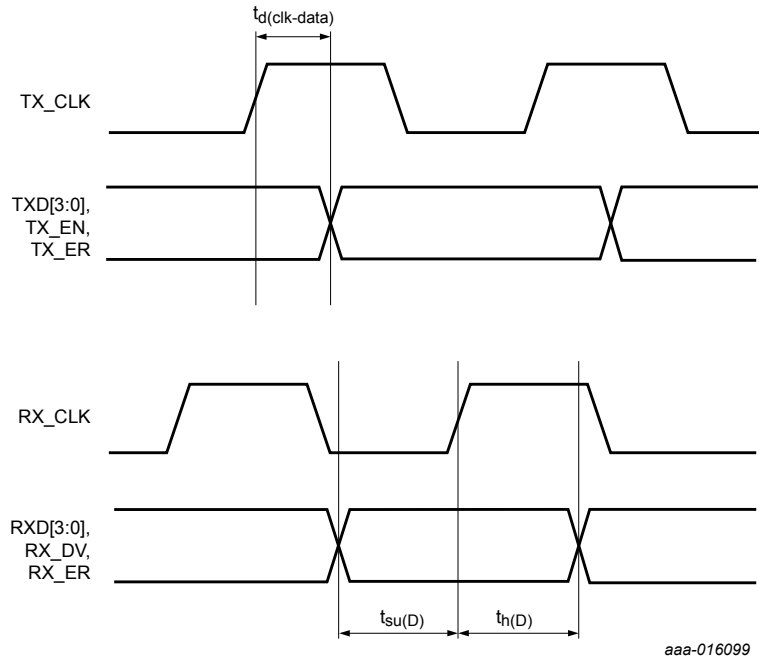


Figure 11. MII timing diagram

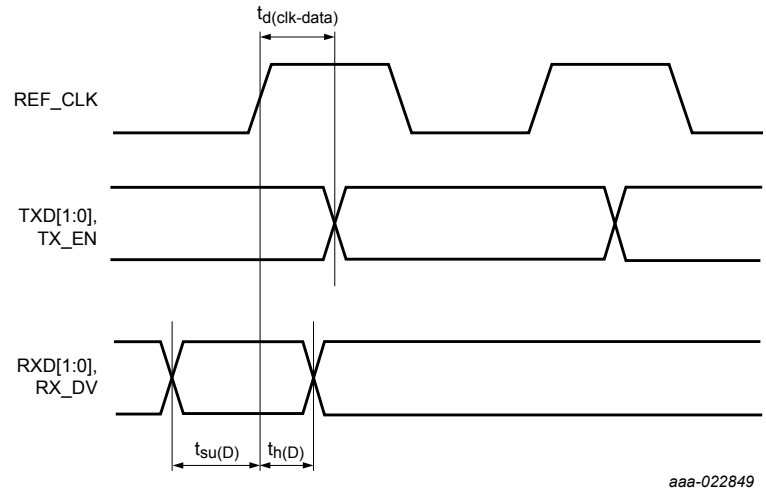


Figure 12. RMII timing diagram

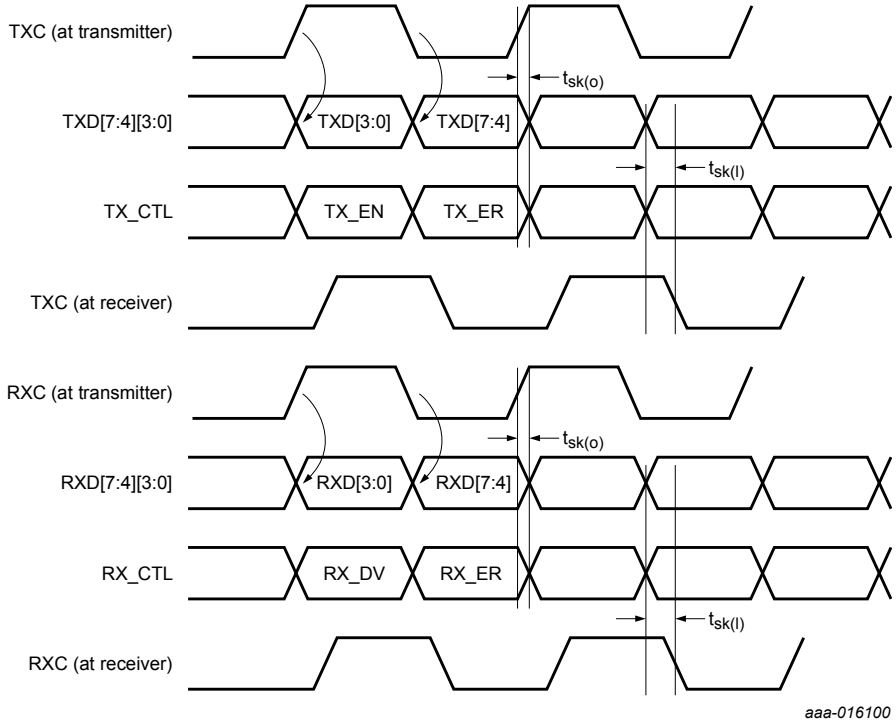


Figure 13. RGMII v1.3 timing diagram

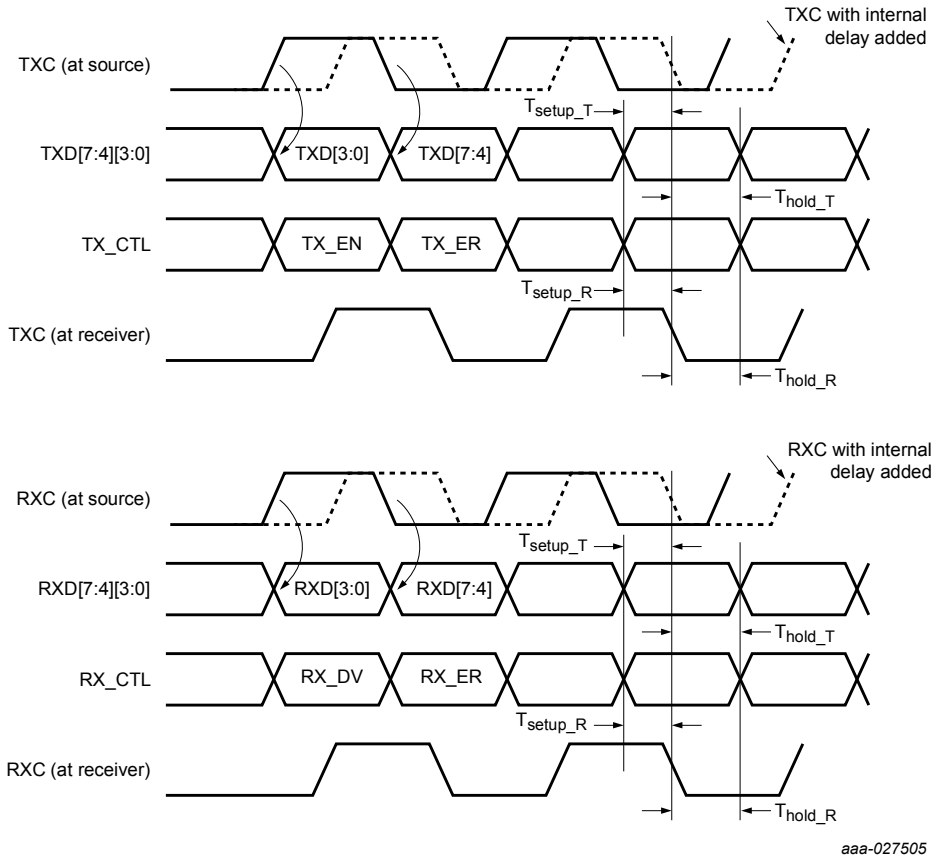
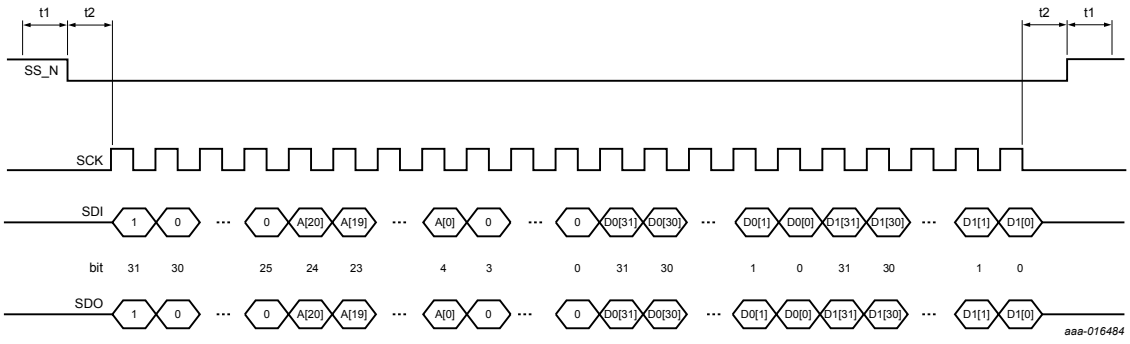


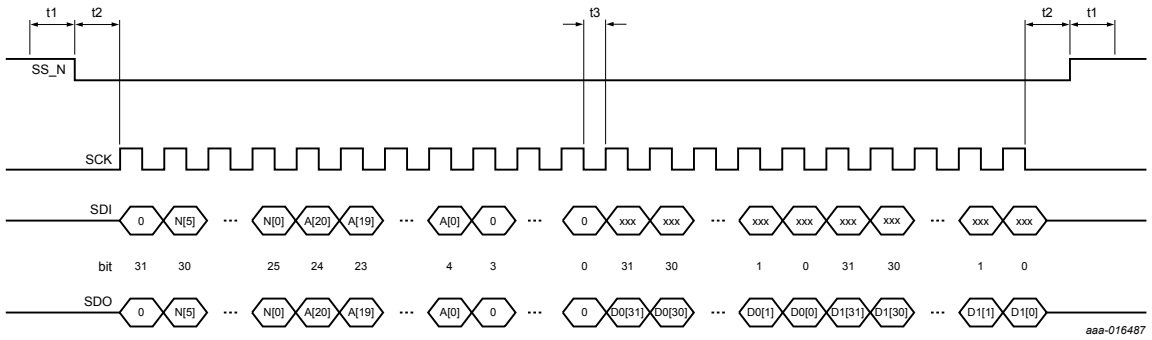
Figure 14. RGMII v2.0 timing diagram



t1: The SPI slave select signal (SS_N) must be stable for at least 0.5 × t_{clk} at the beginning or end of an SPI read or write operation before being asserted/de-asserted.

t2: After the SS_N signal has been asserted at the beginning of an SPI read or write operation, the SPI clock signal (SCK) must be stable for at least 0.5 × t_{clk} before being asserted. At the end of an SPI read or write operation, the SPI clock signal (SCK) must be stable for at least 0.5 × t_{clk} before the SS_N signal is de-asserted.

Figure 15. SPI write timing



t3: The SPI clock signal (SCK) must be stable for at least half a clock period between the reception of longword[0] on the SDI input and the transmission of longword[1] on the SDO output.

Figure 16. SPI read timing

11 Application information

The SJA1105P/Q features a programmable traffic interface. Each of the ports can be configured for 10 Mbit/s or 100 Mbit/s MII/RMII/RGMII, or for 1 Gbit/s RGMII operation. Port 4 is on the SJA1105R/S is a hard-wired SGMII interface.

A typical SJA1105P/Q use case is illustrated in Figure 17.

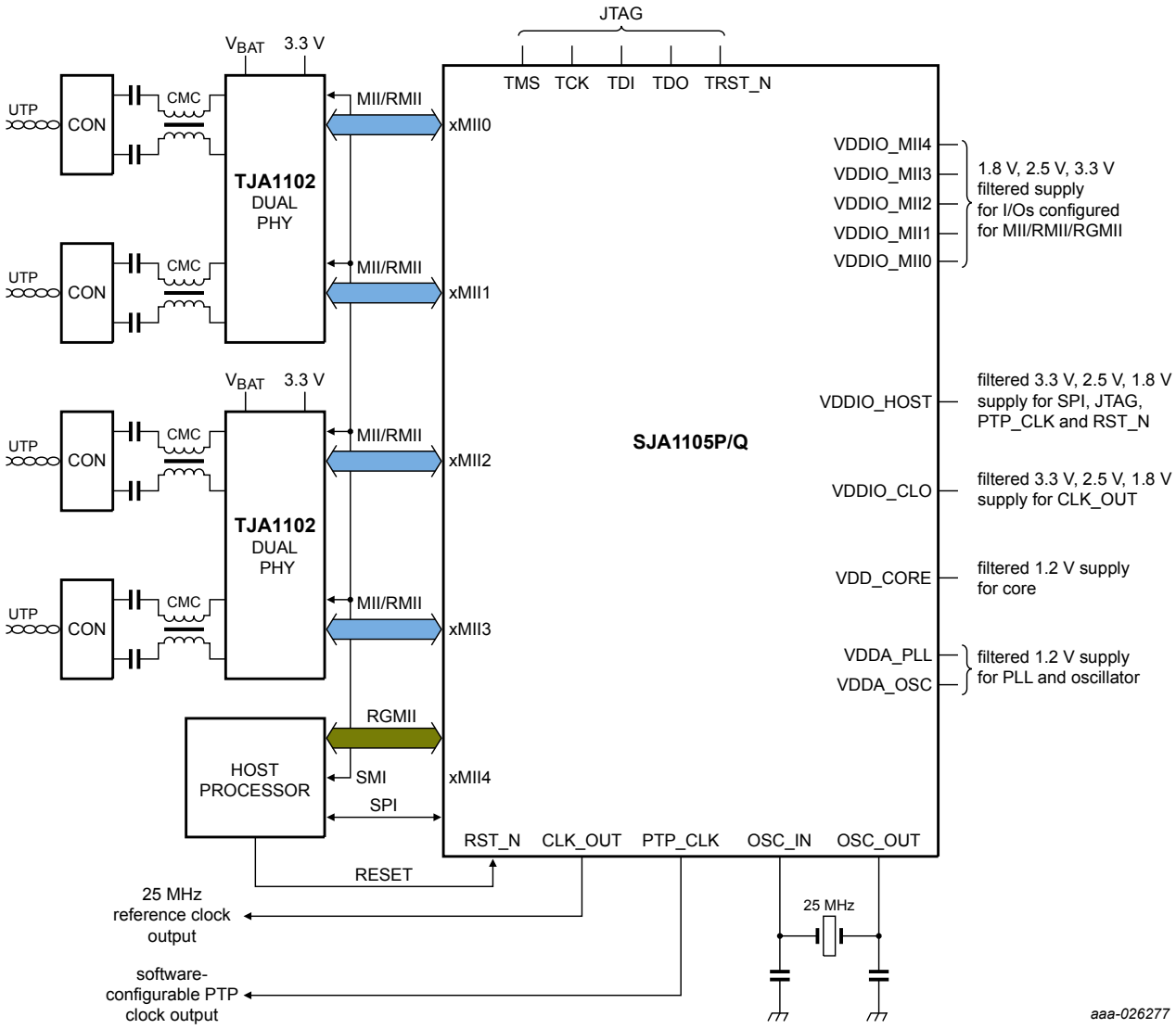


Figure 17. Typical SJA1105P/Q application circuit

In this configuration, two TJA1102 100Base-T1 PHYs are connected to the SJA1105P/Q for MII/RMII operation while a host processor has RGMII connectivity with the SJA1105P/Q. For compatibility with the TJA1102, a VDDIO_MIIx supply of 3.3 V must be selected.

The SPI, JTAG and PTP_CLK interfaces are supplied via VDDIO_HOST. The 25 MHz clock output, CLK_OUT, is supplied from VDDIO_CLO. Both VDDIO_HOST and VDDIO_CLO accept a 1.8 V, 2.5 V or 3.3 V supply. Note that Ethernet connectivity to the host processor is only needed if the system has to support AVB operation or other bridge

management protocols such as STP/RSTP. If such operations are not needed, all the ports can be used for data traffic.

In the configuration shown in Figure 18, two TJA1102 100Base-T1 PHYs are connected to the SJA1105R/S for MII/RMII operation while a host processor has SGMII connectivity with the SJA1105R/S. The SGMII PHY is supplied via a 1.2 V core supply and a 2.5 V analog supply. Note that the SGMII I/O interface operates at voltages specified in the SGMII specification [Ref. 6].

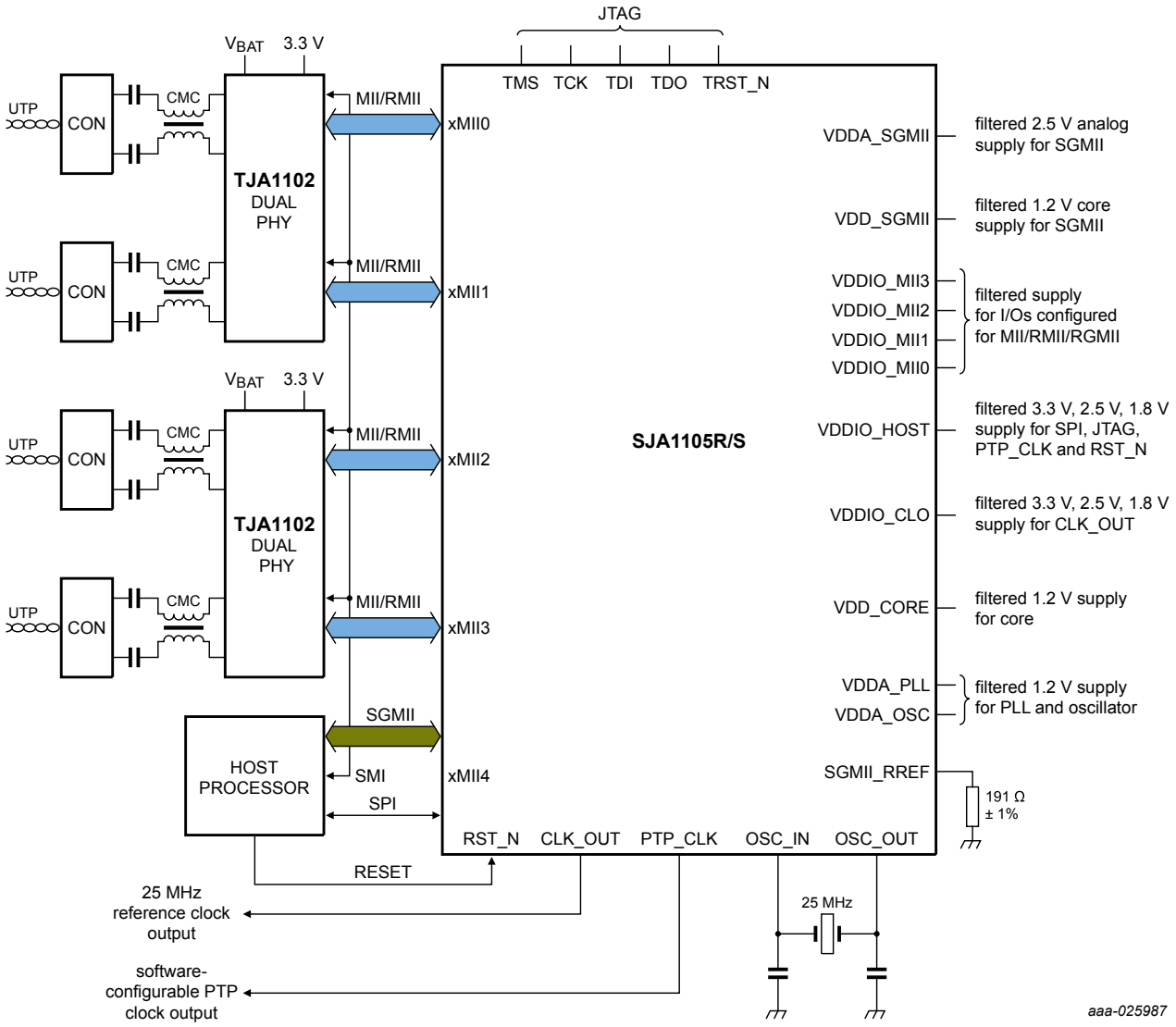


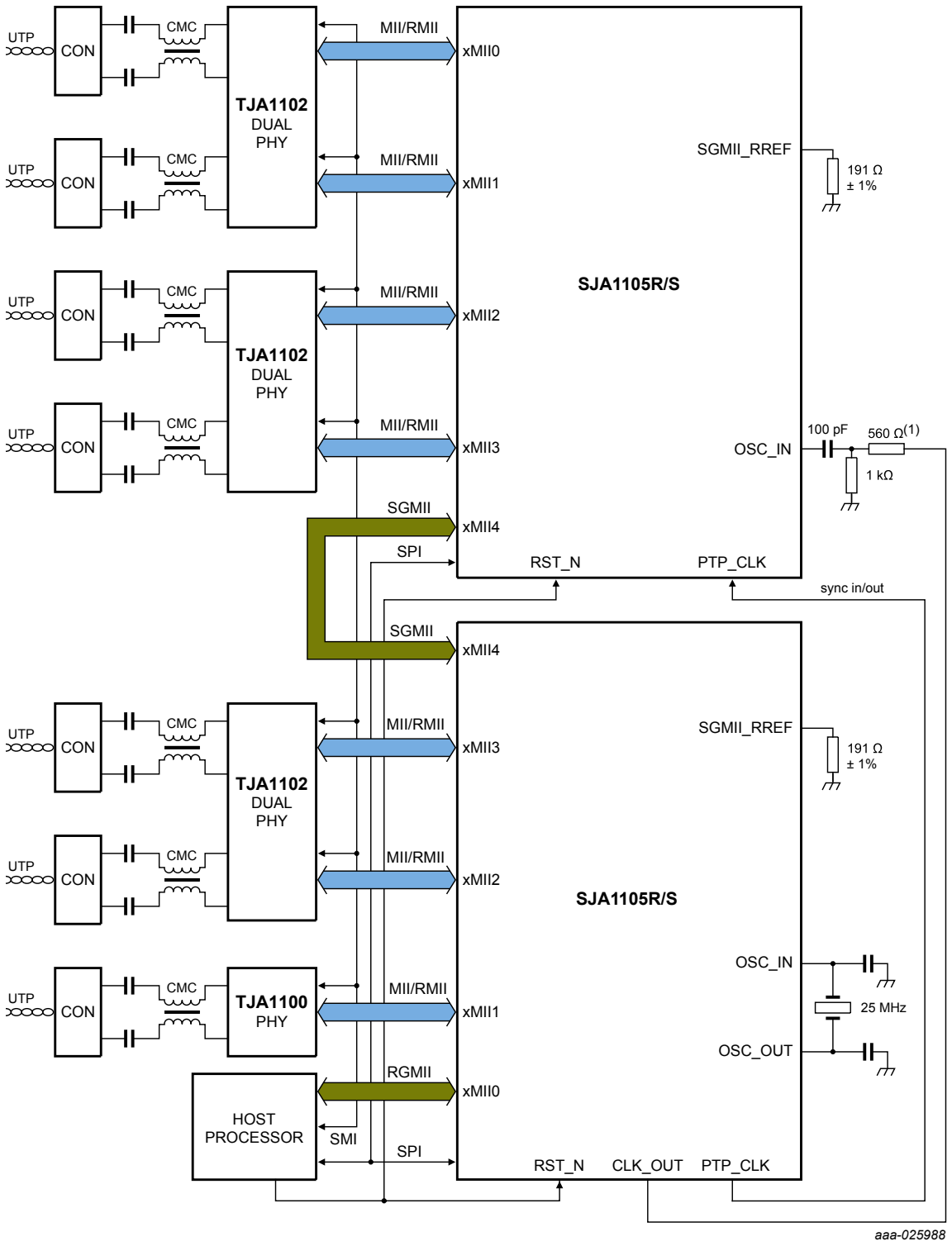
Figure 18. Typical SJA1105R/S application circuit

11.1 Cascading

SJA1105P/Q/R/S devices can be cascaded to increase port count. A typical cascaded switch use case using SGMII is shown in Figure 19. The SGMII interface connecting the cascaded switches must be AC coupled.

The same clock source should be used for all switches in the cascade. This can be realized by feeding the switches from a common clock buffer or by daisy-chaining the

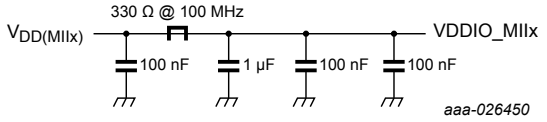
clock through the CLK_OUT pin to the OSC_IN pin. The CLK_OUT pin must be AC coupled to the OSC_IN pin through a divider network to limit the peak-to-peak voltage on the OSC_IN pin.



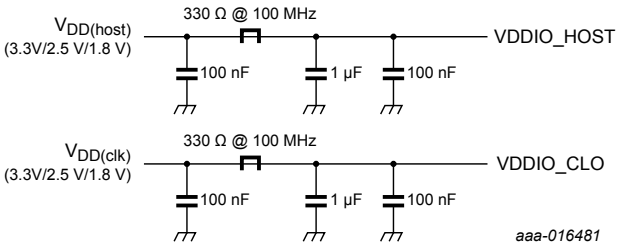
(1) This example (560 Ω / 1 kΩ) is only valid if 3.3 V is used for VDDIO_CLK.

Figure 19. Cascading SJA1105R/S devices

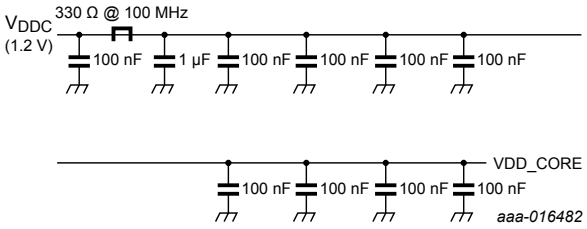
11.2 Power supply filtering



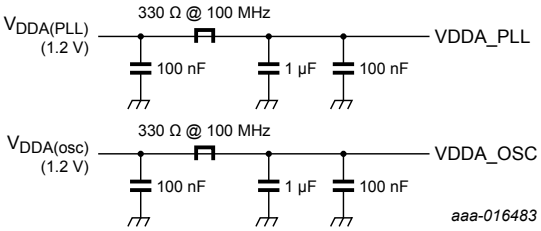
a. I/O pins



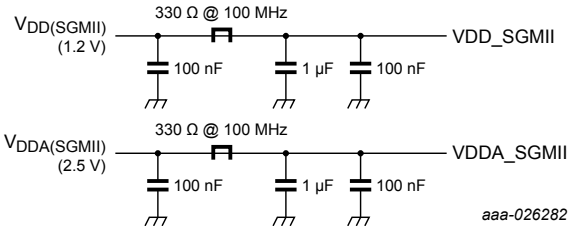
b. host interfacing and reference clock output



c. core



d. PLL and oscillator



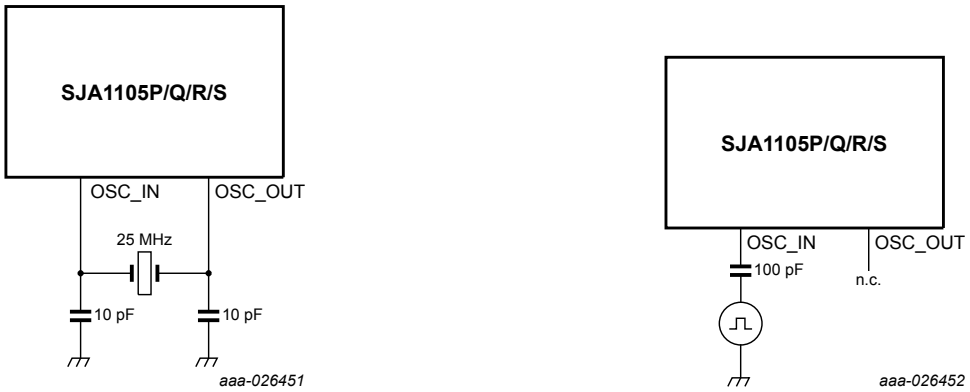
e. SGMII

Figure 20. Power supply filtering

11.3 Clocking

In Crystal oscillator mode, the SJA1105P/Q/R/S oscillator is used as a crystal oscillator with an external 25 MHz crystal and, typically, a 2 × 10 pF load. In Clock mode, the SJA1105P/Q/R/S oscillator is used as a clock input with an external clock connected to input terminal OSC_IN with OSC_OUT left open. Note that a digital clock signal must be AC coupled and limited to $V_{DDA(OSC)}$.

The SJA1105P/Q/R/S outputs a 25 MHz digital clock on the CLK_OUT pin. It can provide a clock signal to a PHY, another switch or a clock buffer for further distribution. The CLK_OUT signal is active immediately after oscillator startup, regardless of the state of the RST_N pin or any other configuration. The CLK_OUT pin can be disabled through software.



a. Crystal oscillator mode

b. Clock mode

Figure 21. Device clocking

11.4 Application hints

Further information on the application of the SJA1105P/Q/R/S can be found in NXP application hints AH1704 ‘SJA1105PQRS Application Hints'.

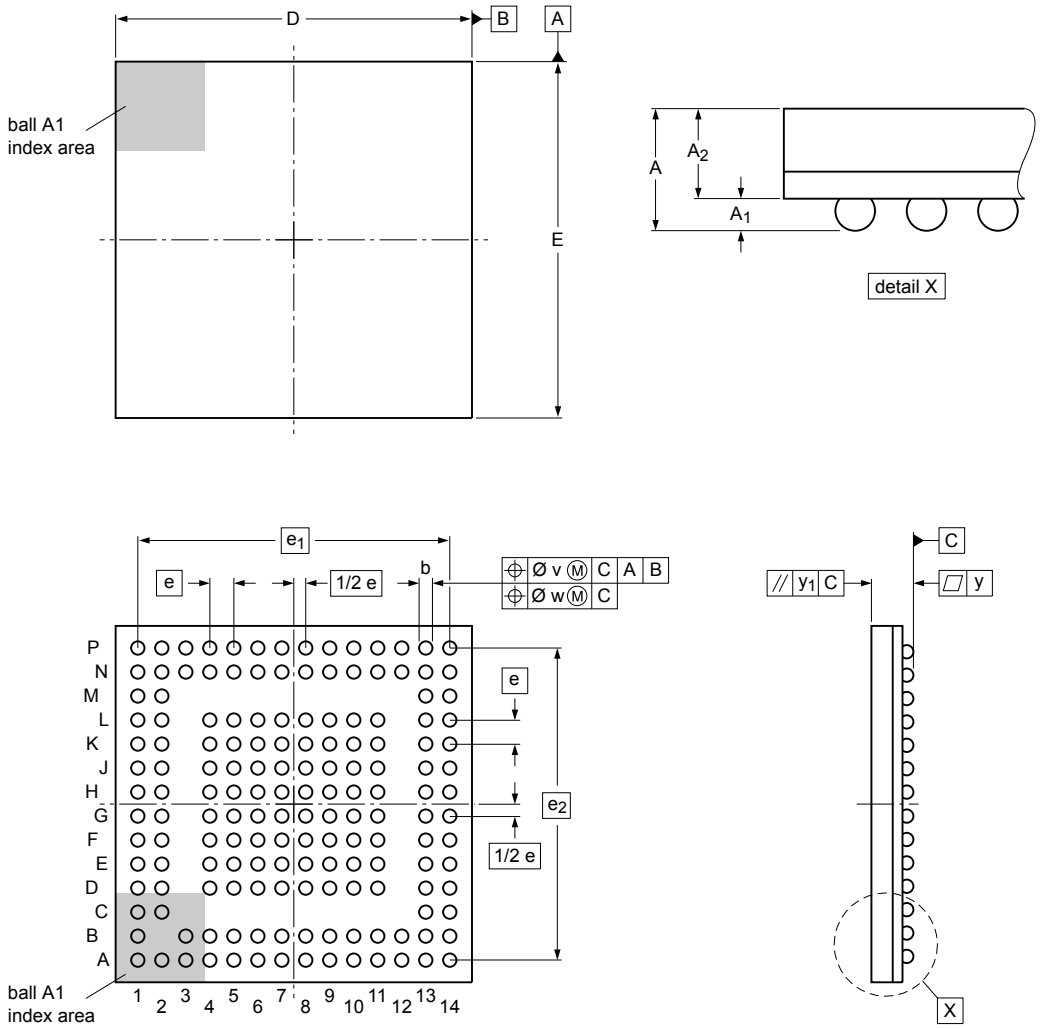
12 Test information

12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits, and is suitable for use in automotive applications.

13 Package outline

LFBGA159: plastic low profile fine-pitch ball grid array package; 159 balls **SOT1427-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
	max	1.50	0.40	1.10	0.50	12.1	12.1							
mm	nom	1.35	0.35	1.00	0.45	12.0	12.0	0.80	10.4	10.4	0.15	0.08	0.12	0.10
	min	1.25	0.30	0.95	0.40	11.9	11.9							

sot1427-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1427-1		MO-205				~~14-07-18~~ 14-07-26

Figure 22. Package outline SOT1427-1 (LFBGA159)

14 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in JESD625-A or equivalent standards.

15 Abbreviations

Table 13. Abbreviations

Abbreviation	Description
AVB	Audio Video Bridging
BSCAN	Boundary Scan
CMC	Common Mode Choke
CRC	Cyclic Redundancy Check
ECU	Electronic Control Unit
Gbit	Gigabit
IFG	InterFrame Gap
JTAG	Joint Test Action Group
LAN	Local Area Network
MAC	Medium Access Controller
Mbit	Megabit
MII	Media Independent Interface
OTP	One-Time Programmable
PHY	Physical Layer (of the interface)
PLL	Phase-Locked Loop
PRBS	Pseudo Random Binary Sequence
PTP	Precision Time Protocol
QoS	Quality of Service
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RSTP	Rapid Spanning Tree Protocol
SMI	Serial Management Interface
SGMII	Serial Gigabit Media Independent Interface
SOF	Start Of Frame
SPI	Serial Peripheral Interface
SR	Stream Reservation (class)
STP	Spanning Tree Protocol
TAP	Test Access Port
TCAM	Ternary Content Addressable Memory
TDL	Tuneable Delay Line

Abbreviation	Description
TSN	Time-Sensitive Networking
TTEthernet	Time-Triggered Ethernet
UTP	Unshielded Twisted Pair
VL	Virtual Link
VLAN	Virtual LAN

16 References

[1] **SJA1105** — SJA1105 5-port automotive Ethernet switch data sheet from NXP Semiconductors

[2] **TJA1100** — TJA1100 100BASE-T1 dual/single PHY for automotive Ethernet data sheet from NXP Semiconductors

[3] **TJA1102** — TJA1102 100BASE-T1 dual/single PHY for automotive Ethernet data sheet from NXP Semiconductors

[4] **MII** — IEEE Std. 802.3

[5] **RMII** — Reduced Media Independent Interface (RMII), March 20, 1998, RMII Consortium Copyright AMD Inc., Broadcom Corp., National Semiconductor Corp., and Texas Instruments Inc., 1997

[6] **RGMII v1.3** — Reduced Gigabit Media Independent Interface (RGMII), V1.3, 12 October 2000, V1.3, Broadcom Corporation, Hewlett Packard, Marvell

[7] **RGMII 2.0** — Reduced Gigabit Media Independent Interface (RGMII), V2.0, 4 January 2002, V2.0, Broadcom Corporation, Hewlett Packard, Marvell

[8] **SGMII** — Serial-GMII Specification, Cisco Systems, Revision 1.8, 2005

[9] **SPI** — SPI Block Guide, V03.06, 04 February 2003, Motorola Inc.

[10] **User Manual** — UM11040 SJA1105PQRS software user manuals available from NXP Semiconductors

17 Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SJA1105PQRS v.1	20171124	Product data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

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