Key Design Features

- Synthesizable, technology independent IP Core for FPGA, ASIC and SoC

- Supplied as human-readable VHDL (or Verilog) source code

- Test patterns generated as an industry standard 20-bit 4:2:2 SMPTE stream

- YCbCr 4:2:2 output pixels

- All 720p, 1080p and 1080i video formats supported (SMPTE 296M and SMPTE 274M)

- Colour-bar output with choice off 8 different patterns

- All signals synchronous with the pixel clock

- Compatible with a wide range of video encoder ICs

- Tiny implementation size makes the core suitable for even the smallest FPGAs and CPLDs

Applications

- Digital video testing and prototyping

- Default output displays and simple 'screen savers'

Generic Parameters

Generic name	Description	Type	Valid range
hd_mode	Output video mode	integer	0: 720p 1: 1080p 2: 1080i

Pin-out Description

| Pin name	I/O	Description	Active state
clk	in	Pixel clock (e.g. 148.5 MHz or 74.25 MHz depending on the required video stndard)	rising edge
reset	in	Asynchronous reset	low
tpg_type [2:0]	in	000 : bars 001 : blues 010 : reds 011 : greens 100 : yellows 101 : browns 110 : purples 111 : greys	data
video_ln [11:0]	out	Output video line number	data
video_y [9:0]	out	Y-channel video output	data
video_c [7:0]	out	C-channel video output	data
video_val	out	SMPTE output video stream valid	high

Block Diagram
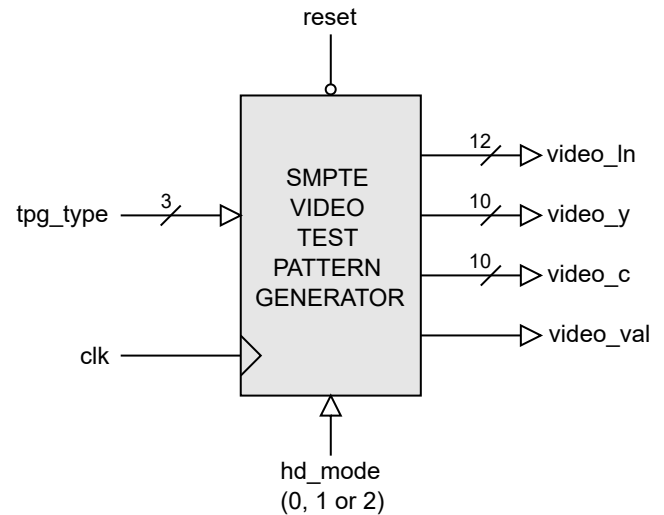
Figure 1: SMPTE Test pattern generator

General Description

The HD_SMPTE_TPG IP Core (Figure 1) is a versatile test pattern generator capable of producing a range of test patterns in 20-bit 4:2:2 format. The output stream format is compliant with the SMPTE standards 296M and 274M. The module is ideal for use in the prototyping stages of digital video systems or as a known good reference source for standard 720p, 1080p or 1080i video.

The video mode is controlled by the generic parameter *hd_mode* and the video test pattern can be set using the parameter *tpg_type*. In total there are 8 different test patterns to choose from.

The output video is a standard SMPTE 20-bit stream that is synchronous with the *clk* signal. The clock frequency should be set to the value that corresponds to the correct pixel clock frequency for the corresponding video mode. For instance, the clock frequency should be set to 74.25 MHz for 720p60, 1080p30 or 1080i60 modes. A clock frequency of 148.5 MHz should be chosen for 1080p60.

Test pattern type

By modifying the test pattern type, the colour and appearance of the test pattern may be controlled. Figure 2 on the following page gives a description of each pattern available[1].

The test pattern type may be programmed in real-time during normal operation. The images shown are for a single frame of a 720p60 video (SMPTE 296M). The video blanking regions are also shown. Note that the vertical blue lines are where the EAV and SAV codes are positioned in the video stream.

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1 Additional test patterns may be provided on request. Please contact Zipcores for more information.

Figure 2: Different test pattern types. An SMPTE 296M (720p) output video stream is shown as an example

Functional Timing

An example output waveform is shown in Figure 3 below. The 20-bit Y/C output data is valid on the rising clock-edge of *clk* when *video_val* is high.

The *video_val* signal is active high one clock cycle after system reset. The current active line number is provided by the *video_ln* signal which is a value from 0 to N. So for example, a 720p format stream has 750 lines in total (including blanking). This means that the video line number will run from 0 to 749.
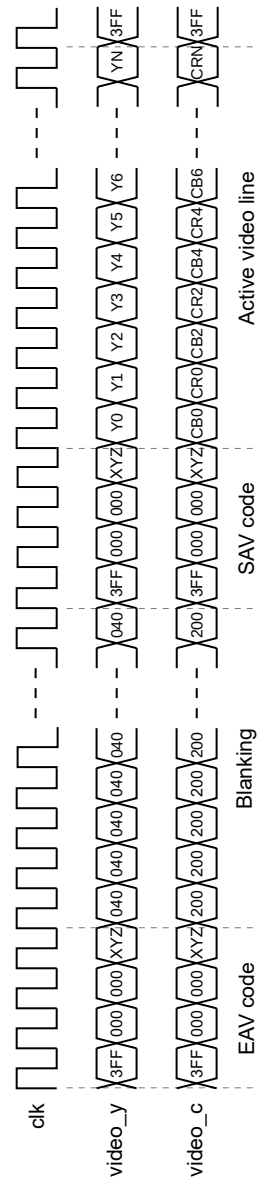

Figure 3: Typical SMPTE 296M/274M output stream

(Note: video_val and video_ln signals not shown)

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