Key Design Features

- Synthesizable, technology independent IP Core fro FPGA, ASIC and SoC

- Supplied as human readable VHDL (or Verilog) source code

- 16-bit signed output data samples

- 32-bit phase accumulator (tuning word)

- 32-bit phase shift feature

- Phase resolution of $2\pi / 2^{16}$

- Frequency resolution of $F_S / 2^{32}$ (F_S = sample frequency)

- Phase dithering option for improved SFDR

- ≈ 100 dB SNR and > 110 dB SFDR (with phase dithering enabled)

- Simultaneous SIN, COS, square and sawtooth outputs

- Optimized quarter-wave LUT for reduced area footprint

- Sample rates of 350 MHz+[1]

Applications

- Digital oscillators and phase-locked loops

- Digital modulation/demodulation

- Digital up/down converters and mixers

- Generation of quadrature (complex) signals

- Versatile waveform generation

Pin-out Description

| Pin name	I/O	Description	Active state
clk	in	Sample clock	rising edge
reset	in	Asynchronous reset	low
en	in	clock enable	high
phase_inc [31:0]	in	Phase increment as an unsigned 32-bit number	data
phase_shift [31:0]	in	Phase shift as an unsigned 32-bit number	data
sin_out [15:0]	out	Sine wave output (16-bit signed number)	data
cos_out [15:0]	out	Cosine wave output (16-bit signed number)	data
squ_out [15:0]	out	Square wave output (16-bit signed number)	data
saw_out [15:0]	out	Sawtooth wave output (16-bit signed number)	data

1   Xilinx® 7-series FPGAs used as a benchmark

Block Diagram
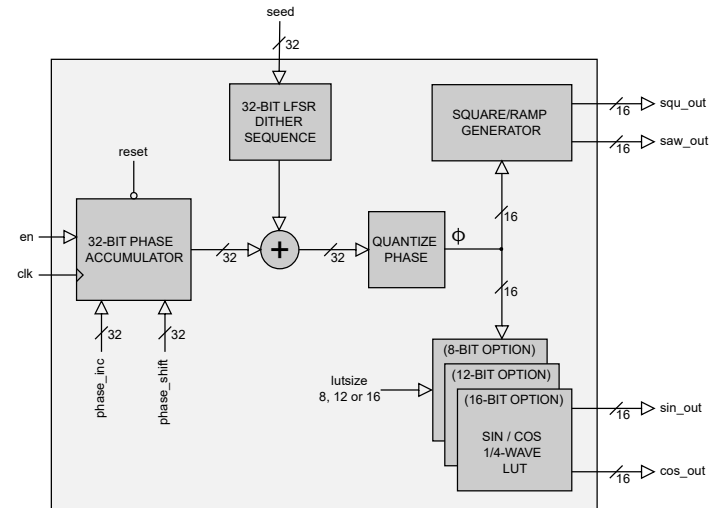
Figure 1: Direct Digital Synthesizer architecture

Generic Parameters

Generic name	Description	Type	Valid range
dithering	Enable phase dithering	boolean	TRUE/FALSE
lutsize	Use an 8,12 or 16-bit Look-up table (Effective size)	integer	8, 16 or 12
seed	Seed for random number generator	std_logic vector	$0 < seed < 2^{32}$

General Description

The DDS IP Core is a high-precision Direct Digital Synthesizer[2] used for the generation of periodic waveforms. On each rising-edge of the sample clock and when the clock-enable is high, the phase in the phase-accumulator is incremented by the value *phase_inc*. This phase is quantized to 16-bits and passed as an address to a look-up table which converts the phase into a waveform.

To save resources, the look-up table is implemented as a quarter sine wave (16384 x 15-bit samples). These samples are manipulated to generate 65536 x 16-bit samples over the range 0 to 2Pi. By setting the generic parameter *lutsize* to 12 or 8, the size of the LUT can be reduced further to (1024 x 11-bit) or (64 x 7-bit) if required. The general architecture of the DDS circuit is shown in Figure 1 above.

In addition to the quadrature outputs *sin_out* and *cos_out*, the DDS also provides square wave and sawtooth outputs: *squ_out* and *saw_out*. All output values are 16-bit signed numbers.

2   Also known as a Numerically Controlled Oscillator (NCO)

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Phase increment

The frequency of the DDS output waveform is controlled by the *phase_inc* signal on a clock-by-clock basis. A change in the phase increment during normal circuit operation will affect a change in the output waveform 5 sample clocks later. The phase increment may be calculated using the formula:

$$\Phi_{INC} = \left(F_{OUT} * 2^{32} \right) / F_S$$

Where F_{OUT} is the desired waveform output frequency and F_S is the sampling frequency. Note that an *integer* value of the phase increment must be used. As an example, consider a 100 MHz sample clock with a desired output frequency of 6.197 MHz. The phase increment would be calculated as $(6.197 * 2^{32}) / 100 = 266159123$.

The minimum and maximum frequencies DDS can generate are given by the following formulas:

$$F_{MIN} = F_S / 2^{32} \quad , \quad F_{MAX} = F_S / 2$$

As an example, a 100 MHz sample clock would allow a minimum DDS frequency of 0.0233 Hz. This is sometimes called the frequency resolution of the DDS. Conversely, the maximum frequency the DDS can generate is given by the Nyquist-Shannon sampling theorem (Fs / 2).

Phase shift

The relative phase of the DDS output waveform may be controlled by the *phase_shift* input. This input takes the form of a 32-bit unsigned value that is added to the phase accumulator. To implement a phase shift, then the *phase_shift* input should be asserted for 1 clock cycle. At all other times then the phase shift must be set to zero. The phase shift in degrees is calculated using the following formula:

$$\Phi_{SHIFT} = \Delta / 360 * 2^{32}$$

For example, to implement a phase shift of 45° in the output waveform then the *phase_shift* input would be calculated as $(45/360)*2^{32}$ or 0x20000000 in hex. This value of phase shift should be asserted for one clock cycle then reset to 0x00000000.

Phase dithering

The process of phase quantization introduces noise on the phase signal and it produces unwanted spurious spectral components in the DDS output signal (referred to as *spurs*). The difference between the carrier level and the maximum level of spurs is called the *Spurious Free Dynamic Range* (SFDR).

The DDS component alleviates this problem by adding a random number to the LSBs of the 32-bit phase accumulator before quantization. This has the effect of spreading the spurs throughout the available bandwidth while preventing spurs at the same harmonic frequencies reinforcing each other. With phase dithering enabled, an improvement of around 10 to 20 dB in SFDR may be achieved.

The random number used for phase dithering is generated using a *Linear Feedback Shift Register* (LFSR) of order 32. The LFSR is free running and generates a random bit every sample clock in accordance with the polynomial:

$$x^{32} + x^7 + x^5 + x^3 + x^2 + x^1 + x^0$$

The user may choose any number (other than zero) as an initial seed for the random number generator. Different seeds, in some cases, can change the SFDR by around +/- 1dB.

Functional Timing

Figure 2 shows the operation of the DDS immediately after reset. After reset goes high the DDS starts to generate the output waveforms 5 clock cycles later. Asserting the clock-enable low will stall the pipeline. Asserting clock-enable high once again will start waveform output at the next sample point in the waveform.
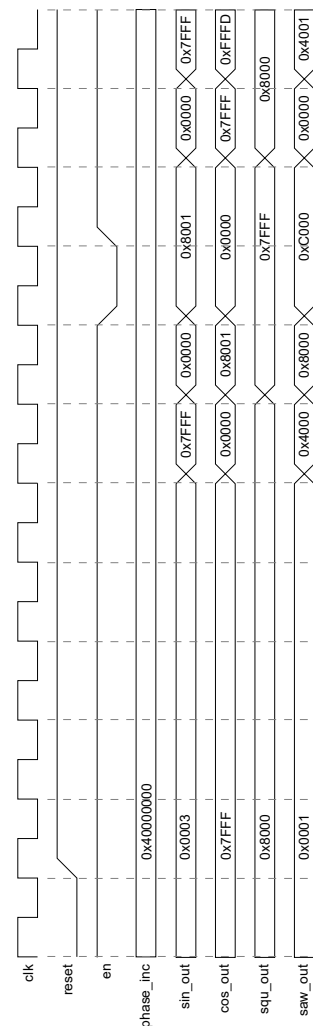

Figure 2: DDS operation after reset

Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	Description
sincos_lut16.vhd	SIN/COS look-up table (16-bit equivalent version)
sincos_lut12.vhd	SIN/COS look-up table (12-bit equivalent version)
sincos_lut8.vhd	SIN/COS look-up table (8-bit equivalent version)
dds.vhd	Top-level component
dds_bench.vhd	Top-level test bench

Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. sincos_lut16.vhd
2. sincos_lut12.vhd
3. sincos_lut8.vhd
4. dds.vhd
5. dds_bench.vhd

The VHDL testbench instantiates the DDS component and the user may modify the phase increment and generic parameters in order to generate the desired output waveform. The example provided generates a 2.73 MHz waveform with a 100 MHz sample clock.

The simulation must be run for at least 3 ms during which time the DDS will output the SIN, COS, square and sawtooth waveforms. Output samples are captured in the text file *dds_out.txt.* Figures 3 to 6 show plots of the resulting waveforms.
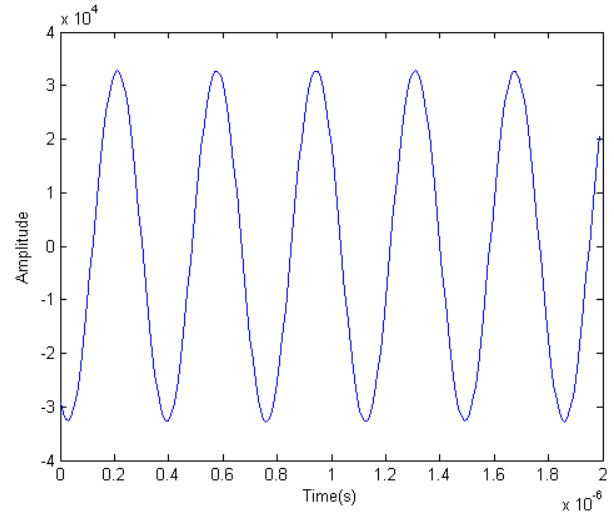

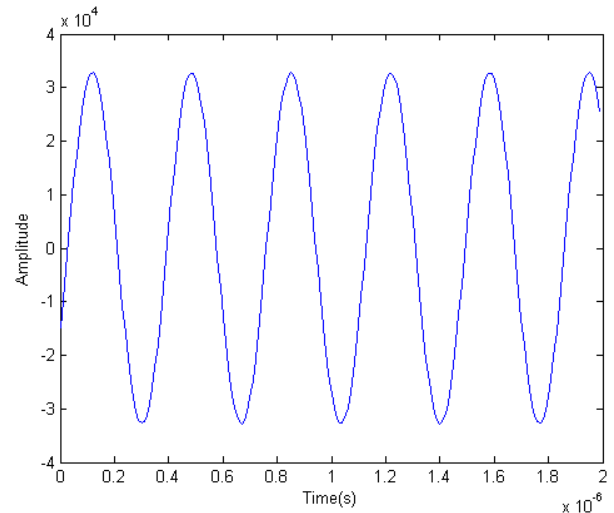*Figure 3: SIN waveform output (2.73 MHz)*
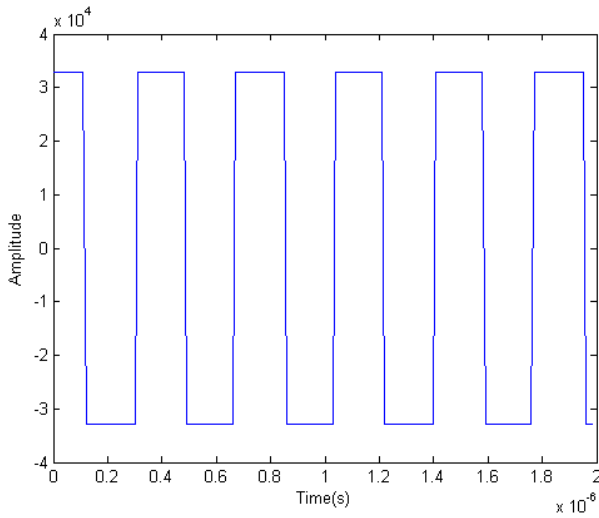

Figure 4: COS waveform output (2.73 MHz)

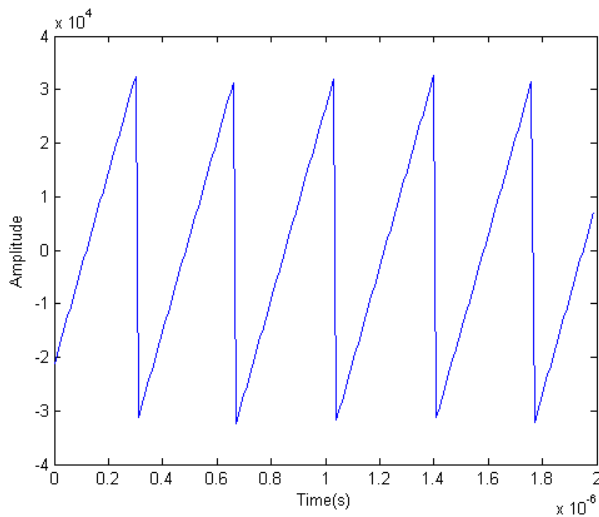*Figure 5: Square waveform output (2.73 MHz)*

Figure 6: Sawtooth waveform output (2.73 MHz)

Performance

The following plots demonstrate the effect of phase dithering on the output power spectra. The plots show the mean-squared power estimate of the SIN output samples for a 100MHz sample clock and a 2.73 MHz output waveform. The size of the LUT has been set to 16-bits.
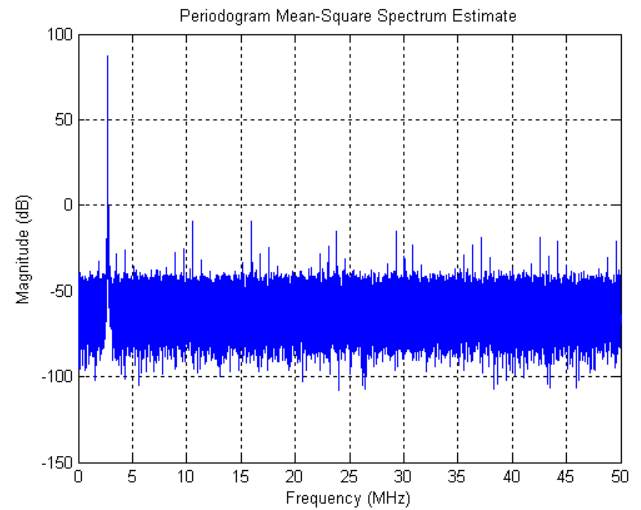

Figure 7: Single 2.73 MHz tone - dithering disabled

The SFDR for the non phase-dithered case (Figure 7) exhibits an SFDR of 96.3 dB with the largest magnitude spur of -9.1 dB at around 16 MHz.

Figure 8 shows the same 2.73 MHz tone with phase-dithering enabled. The SFDR is 114.9 dB with the largest magnitude spur of -27.7 dB at around 8 MHz. This is an improvement in SFDR of 18.6 dB.
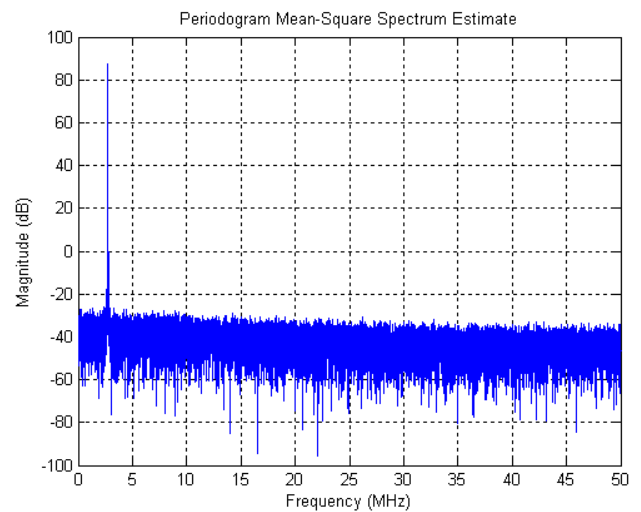

Figure 8: Single 2.73 MHz tone - dithering enabled

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