**ATAN2_XY**

12-bit 4-Quadrant Arctan Function

Rev. 1.2

## Key Design Features

- Synthesizable, technology independent VHDL IP Core
- Function φ = atan2 (y,x)
- Inputs as 12-bit signed numbers
- Output phase as a 19-bit signed
- Output range -π ≤ φ ≤ π
- Option for scaled output phase in range -1 ≤ φ ≤ 1
- Accurate to within 0.00008 radians
- High-speed fully pipelined architecture
- Small implementation size
- 7 clock-cycle latency

## Applications

- Fixed-point mathematics
- Precision phase measurements in digital communications and digital signal processing
- Digital Phase-locked Loops (PLLs)
- More accurate, smaller, lower latency and faster than a CORDIC solution of similar specification

## Pin-out Description

| Pin name | I/O | Description | Active state |
|---|---|---|---|
| clk | in | Synchronous clock | rising edge |
| en | in | Clock enable | high |
| x_in [11:0] | in | Input value | data |
| y_in [11:0] | in | Input value | data |
| phi_out [18:0] | out | Output phase angle in radians | data |

## Functional Specification

| Value | Type | Valid range |
|---|---|---|
| x_in [11:0] | 12-bit signed number | [-2048, 2047] |
| y_in [11:0] | 12-bit signed number | [-2048, 2047] |
| phi_out [18:0] | 19-bit signed fraction in [19 16] format | [-π, π]<br><br>Accurate to within 0.00008 radians |

## Block Diagram

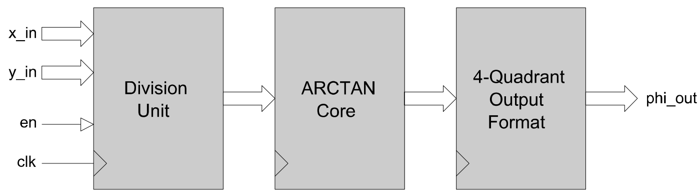


*Figure 1: 4-quadrant Arctan core architecture*

## General Description

ATAN2_XY (Figure 1) calculates the 4-quadrant inverse tangent in the range -π to π. It has a fully pipelined architecture and uses fixed-point mathematics throughout. Input values are accepted as 12-bit signed numbers in the range -2048 to 2047. The calculated output phase (in radians) is a 19-bit signed value with 1 sign bit, 2 integer bits and 16 fractional bits. As an example, the output phase angle 0x18000 would represent 1.5 radians and the value 0x68000 would represent the value -1.5 radians. Internally, the arctan core function uses a 2[nd] order polynomial of the form:

$$y = ax^2 + bx + c$$

The coefficients a, b and c dynamically change with respect to the input value in order to generate a more accurate approximation. The output result is accurate to within 0.00008 radians. Values are sampled on the rising clock-edge of *clk* when *en* is high. The function has a 7 clock-cycle latency in normal operation and 9 clock-cycles when the scaled phase output is selected.

### *Scaled phase output option*

By default, the output phase angle is computed in radians in the range -Pi to Pi. This is specified by setting the generic parameter *scale_output = false.* Alternatively, by setting the generic parameter: *scale_output = true*, the output phase angle is generated in the range -1 to 1. The two options are described graphically in Figure 2 below.

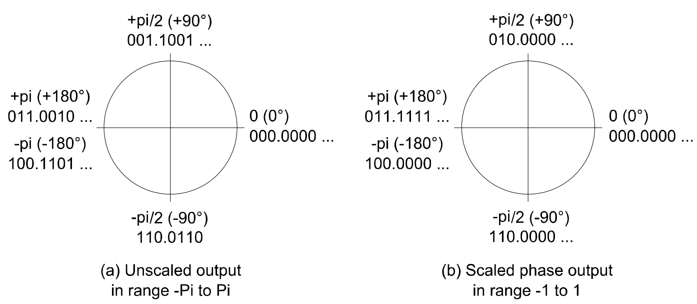


*Figure 2: Output phase angle options:*
*(a) scale_output = false, (b) scale_output = true*

## Functional Timing

Figure 3 demonstrates a series of computations of φ = atan2 (y,x). Samples are processed on the rising edge of *clk* when *en* is high. The function has a 7 cycle latency as shown by the timing between edges 'A' and 'B' in the waveform.

In the example, the first calculation is φ = atan2(0x02C,0x07E), the next calculation is φ = atan2(0xEB7, 0x98D). The results are respectively 0x05601 and 0x50E1B. Converting the numbers to decimals and decimal fractions the calculations are equivalent to:

$$\varphi = atan2\,(44{,}126) = 0.335953$$

and ..

$$\varphi = atan2\,(-329{,}-1651) = -2.944901$$

Note that the clock-enable is held low for one clock cycle during the second sample during which the whole pipeline is stalled.

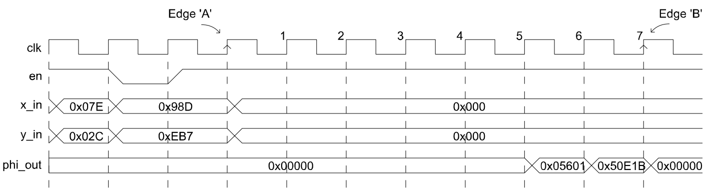


*Figure 3: Timing waveform for the atan2_xy function*

## Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

| ***Source file*** | ***Description*** |
|---|---|
| lut_reciprocal.vhd | Reciprocal unit |
| lut_divide.vhd | Division unit |
| atan2_scale.vhd | Phase scaling unit |
| atan2_x.vhd | Arctan core function |
| atan2_xy.vhd | Top-level block |
| atan2_xy_bench.vhd | Top-level test bench |

## Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. lut_reciprocal.vhd
2. lut_divide.vhd
3. atan2_scale.vhd
4. atan2_x.vhd
5. atan2_xy.vhd
6. atan2_xy_bench.vhd

The simulation must be run for at least 2 ms during which time a randomized 2 x 12-bit input stimulus will be generated at the input to the arctan core. The test terminates automatically.

The simulation generates two text files called *atan2_xy_in.txt* and *atan2_xy_out.txt*. These files contain the input and output samples captured during the course of the test and may be used to verify the correct operation of the core.

## Performance

Quadrature samples were generated in the range -π to π in order to check the accuracy and linearity of the phase output. Quadrature samples were generated according to the formulas:

$$x = G * \cos(\varphi)$$
$$y = G * \sin(\varphi)$$

Where φ is a phase angle in the range [-π, π] and G is a scale factor. The generated x, y samples were used as an input stimulus to the ATAN2_XY core and the output samples were captured during the simulation.

Figure 4 shows the resulting plot of (ideal) input phase vs. output phase in radians. The overall accuracy was measured at 0.00008 radians. This compares with a theoretical best case of 0.000015 radians for a 16-bit fractional output.

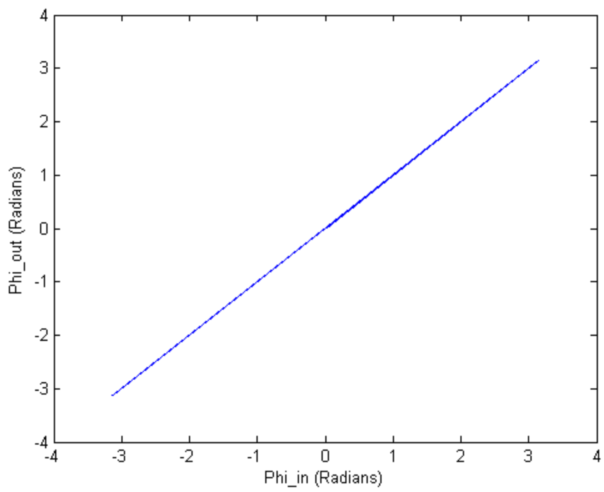


*Figure 4: Plot of Input phase vs. output phase showing good linear relationship*