

## Key Design Features

- Synthesizable, technology independent VHDL IP Core
- Test patterns generated as an industry standard 8-bit ITU-R BT.656 stream
- YCbCr 4:2:2 output pixels
- Both PAL and NTSC (720 x 576i and 720 x 480i) formats supported
- Choice of 6 different test pattern outputs
- All signals synchronous with the pixel clock
- Compatible with a wide range of video codec ICs
- Tiny implementation size makes the core suitable for even the smallest FPGAs and CPLDs

## Applications

- Digital video testing and prototyping
- Default output displays and simple 'screen savers'

## Generic Parameters

Generic name	Description	Type	Valid Range
tpg_mode	Output video mode	integer	0: PAL (576i) 1: NTSC (480i)
tpg_type	Test pattern type	integer	0 : colour bars 1 : colour checks 2 : hatch 3 : crosses 4 : blue screen 5 : alternating fields

## Pin-out Description

Pin name	I/O	Description	Active state
clk	in	Pixel clock (normally 27 MHz)	rising edge
reset	in	Asynchronous reset	low
video_out [7:0]	out	BT.656 output video (8-bit)	data
video_val	out	BT.656 output video valid	high

## Block Diagram

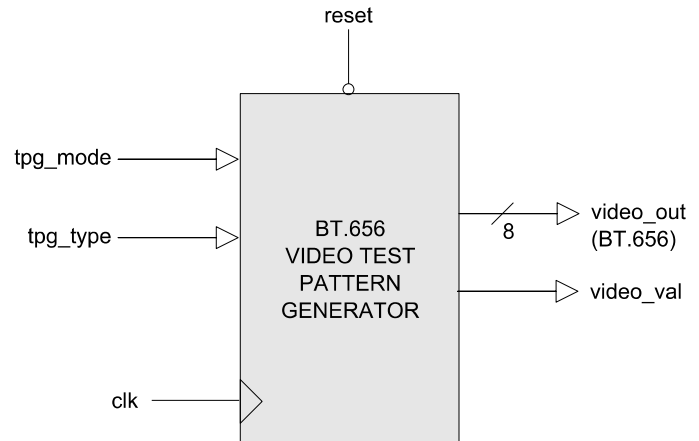


Figure 1: BT.656 Test pattern generator

## General Description

The BT656\_TPG module (Figure 1) is a versatile test pattern generator capable of producing a range of test patterns in 8-bit ITU-R BT.656 format. The module is ideal for use in the prototyping stages of digital video systems, or as a known good reference source for BT.656 video.

The video mode and output test pattern is controlled by a pair of generic parameters. The video output mode can be set using the parameter *tpg\_mode*. This gives the option of either 576i (PAL) or 480i (NTSC) output formats. The type of test pattern output is controlled by the *tpg\_type* parameter. In total there are a range of 6 different test patterns to choose from.

The output video is a standard BT.656 8-bit stream that is synchronous with the *clk* signal. The clock frequency is normally set to 27 MHz in order to comply with the BT.656 standard and the 16-bit pixel sample rate of 13.5 MHz.

### Test pattern mode and type

By modifying the test pattern type, the colour and appearance of the test pattern may be controlled. Figure 2 on the following page gives a description of each pattern available<sup>1</sup>.

The images show the consecutive odd and even fields and also include the video blanking regions. The vertical blue lines are where the EAV and SAV codes are positioned in the video stream.

<sup>1</sup> Original bitmap images for the output test patterns may be provided on request. Other custom test patterns can also be provided. Please contact Zipcores for more information.

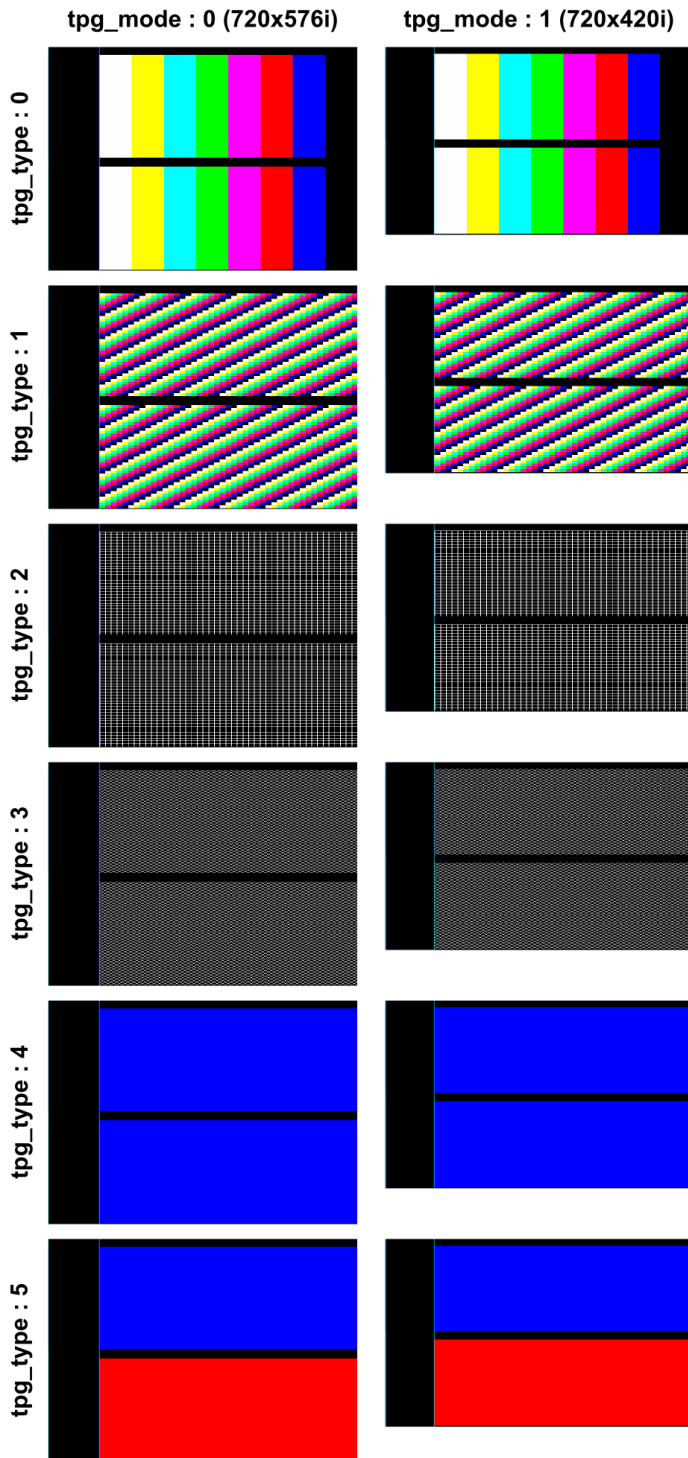


Figure 2: Video output test patterns for 576i and 480i video

### Functional Timing

An example output waveform is shown in Figure 3 below. The 8-bit output data is valid on the rising clock-edge of *clk* when *video\_val* is high.

The *video\_val* signal is active high with the first valid byte of the stream after a system reset.

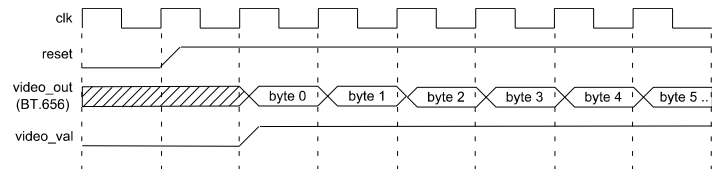


Figure 3: BT.656 output video timing

### Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief explanation of each file.

Source file	Description
bt_656_tpg_enc.vhd	Main BT.656 encoder module
bt_656_tpg_unpack.vhd	32-bit to 8-bit unpacker
bt_656_tpg.vhd	Top-level component
bt_656_tpg_bench.vhd	Top-level testbench

### Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. bt\_656\_tpg\_enc.vhd
2. bt\_656\_tpg\_unpack.vhd
3. bt\_656\_tpg.vhd
4. bt\_656\_tpg\_bench.vhd

The VHDL testbench instantiates the BT\_656\_TPG component with the video format set to 576i (PAL) and the output test pattern set to colour bars.

The simulation must be run for at least 20 ms during which time the outputs are captured to a text file called *bt\_656\_out.txt*. This file contains the captured BT.656 stream with each byte on a consecutive line.

### Synthesis and Implementation

The files required for synthesis and the design hierarchy is shown below:

- bt\_656\_tpg.vhd
  - bt\_656\_tpg\_enc.vhd
  - bt\_656\_tpg\_unpack.vhd