

### Key Design Features

- Synthesizable, technology independent VHDL Core
- Function  $y = \text{atan}(x)$
- Input range  $0 \leq x \leq 1$
- Output range  $0 \leq y \leq \pi/4$
- Based on a quadratic polynomial with dynamic coefficients
- Input values as 16-bit unsigned fractions
- Output values as 16-bit unsigned fractions in radians
- Accurate to within 0.00004 radians
- High-speed 250MHz+ operation<sup>1</sup>
- Fully pipelined architecture
- 3 clock-cycle latency

### Applications

- Fixed-point mathematics
- Phase measurements in digital communications
- Alternative to using a 64k x 16-bit LUT (128 kbytes)

### Pin-out Description

Pin name	I/O	Description	Active state
clk	in	Synchronous clock	rising edge
en	in	Clock enable	high
x_in [15:0]	in	Input value	data
y_out [15:0]	out	Output value in radians	data

### Functional Specification

Value	Type	Valid range
x_in [15:0]	16-bit unsigned fraction in [16 16] format	[0, 1]
y_out [15:0]	16-bit unsigned fraction in [16 16] format	[0, $\pi/4$ ]
		Accuracy to within 0.00004 radians

### Block Diagram

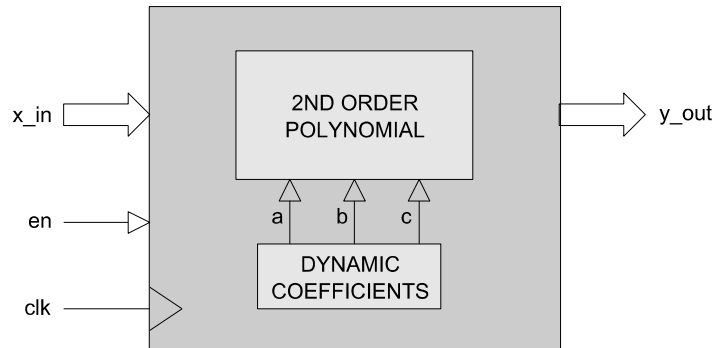


Figure 1: Atan\_x function architecture

### General Description

ATAN\_X (Figure 1) calculates the inverse tangent of a fraction. It has a fully pipelined architecture and uses fixed-point mathematics throughout. Input values are accepted as 16-bit unsigned fractions in the range 0 to 1. Output values are 16-bit unsigned fractions in the range 0 to  $\pi/4$ . Both input and output values are in [16 16] format with 0 integer bits and 16 fraction bits. As an example the input value 0x4000 would signify the fraction 0.5.

Internally, the function uses a 2<sup>nd</sup> order polynomial of the form:

$$y = ax^2 + bx + c$$

The coefficients a, b and c dynamically change with respect to the input value in order to generate a more accurate approximation. The output result is accurate to within 0.00004 radians.

Values are sampled on the rising clock-edge of *clk* when *en* is high. The function has a 3 clock-cycle latency.

### Functional Timing

Figure 2 demonstrates the computation of  $y = \text{atan}(x)$ , where  $x = 0xA673$  (0.6502 as a decimal fraction). The result, 0x9395 (0.5765 in decimal) has a latency of 3 clock cycles.

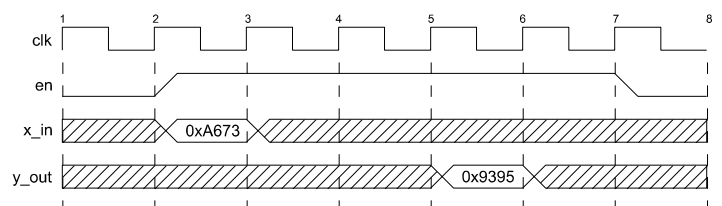


Figure 2: Calculation of  $y = \text{atan}(x)$

<sup>1</sup> Xilinx Virtex 6 FPGA used as a benchmark

## Source File Description

All source files are provided as text files coded in VHDL. The following table gives a brief description of each file.

Source file	Description
atan_x.vhd	Top-level block
atan_x_bench.vhd	Top-level test bench

## Functional Testing

An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is as follows:

1. atan\_x.vhd
2. atan\_x\_bench.vhd

The simulation must be run for at least 1 ms during which time a 16-bit input stimulus in the range 0 to 65535 will be generated. The test terminates automatically.

The simulation generates a text file called *atan\_x\_out.txt*. This file contains the output results captured during the test. The results of the test are shown graphically in Figure 3 below:

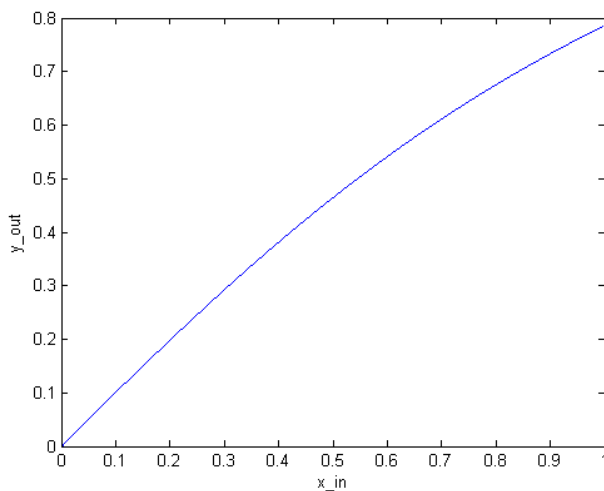


Figure 3: Plot of test results for atan\_x function

## Synthesis

The source file 'atan\_x.vhd' is the only file required for synthesis. There are no sub-modules in the design.

The VHDL core is designed to be technology independent. However, as a benchmark, synthesis results have been provided for the Xilinx® Virtex 6 and Spartan 6 FPGA devices. Synthesis results for other FPGAs and technologies can be provided on request.

Resource usage is specified after Place and Route.

### VIRTEX 6

Resource type	Quantity used
Slice register	41
Slice LUT	50
Block RAM	0
DSP48	3
Occupied slices	16
Clock frequency (approx)	270 MHz

### SPARTAN 6

Resource type	Quantity used
Register	41
Slice LUT	50
Block RAM	0
DSP48	3
Occupied slices	22
Clock frequency (approx)	200 MHz

## Revision History

Revision	Change description	Date
1.0	Initial revision	28/04/2008
1.1	Improved accuracy and updated synthesis results	07/04/2009
1.2	Improved accuracy further and updated synthesis results	30/04/2009
1.3	Updated synthesis results for Xilinx® 6 series FPGAs	06/06/2012