DATA SHEET

SKY13298-360LF: GaAs SP2T Switch for Ultra Wideband (UWB) 3–8 GHz

Features

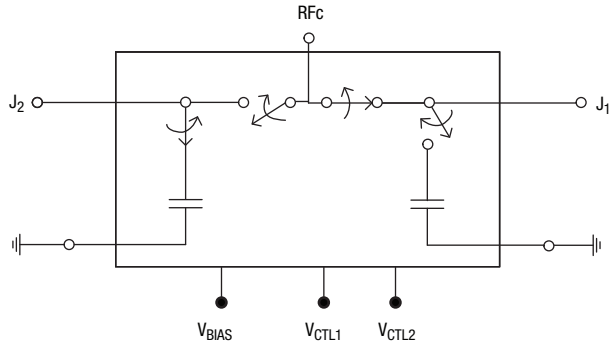
- Positive voltage control (0/1.8 V to 0/3.3 V)
- High isolation 25 dB for BG1, 25 dB for BG3
- Low loss 0.7 dB typical for BG1, 0.9 dB for BG3
- Lead (Pb)-free and RoHS-compliant

Description

The SKY13298-360LF is a pHEMT GaAs FET IC switch packaged in an 2 x 2 mm, 8-lead exposed pad plastic package for low-cost commercial applications. The use of the V_{BIAS} line enables the part to be used with low control bias voltages down to 1.8 V. This switch is ideal for Ultra Wide Band (UWB) applications covering BG1 and BG3. For 3.3 V control, the V_{BIAS} is not required and is left open circuit on the board.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

Functional Block Diagram



Electrical Specifications

V_{BIAS} = 1.8 V, V_{CTL} = 0 V/1.8 V, T = 25 °C, P_{INPUT} = 0 dBm, Z_O = 50 Ω, unless otherwise noted

Parameter	Frequency	Min.	Typ.	Max.	Unit
Insertion Loss	3.168–4.752 GHz		0.7	0.9	dB
	6.336–7.920 GHz		0.9	1.0	dB
Isolation	3.168–4.752 GHz	22	25		dB
	6.336–7.920 GHz	19	22		dB
Return loss (Insertion loss state)	3.168–4.752 GHz		25		dB
	6.336–7.920 GHz		12		dB

Operating Characteristics

V_{BIAS} = 1.8 V, V_{CTL} = 0 V/1.8 V, T = 25 °C, P_{INPUT} = 0 dBm, Z_O = 50 Ω, unless otherwise noted

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics						
Rise/fall time	10/90% or 90/10% RF			20		ns
On/off time	50% V_{CTL} to 90/10% RF			20		ns
Input power for 1 dB compression	V_{BIAS} = 1.8 V, V_{CTL} = 0 V/1.8 V	3.168–4.752 GHz		18		dBm
	V_{BIAS} = 1.8 V, V_{CTL} = 0 V/1.8 V	6.336–7.920 GHz		16		dBm
	V_{BIAS} = open circuit, V_{CTL} = 0 V/3.3 V	3.168–4.752 GHz		26		dBm
	V_{BIAS} = open circuit, V_{CTL} = 0 V/3.3 V	6.336–7.920 GHz		24		dBm
Intermodulation intercept point (IP3)	For two tone input power 5 dBm/tone 1 MHz spacing,					
	V_{BIAS} = 1.8 V, V_{CTL} = 0 V/1.8 V	3.168–4.752 GHz		39		dBm
		6.336–7.920 GHz		34		dBm
	V_{BIAS} = O/C, V_{CTL} = 0 V/3.3 V	3.168–4.752 GHz		47		
		6.336–7.920 GHz		42		
Control voltages	$V_{CTL\ LOW}$		0		0.2	V
	$V_{CTL\ HIGH}$ = V_{BIAS}		1.8		3.3	V
Supply voltage	V_{BIAS}		1.8		3.3	V
Supply currents	V_{BIAS} = 1.8 to 3.3 V			5		µA
	$V_{CTL\ LOW}$, $V_{CTL\ HIGH}$			5		µA

Truth Table

V_{BIAS}	V_{CTL1}	V_{CTL2}	RFc-J_1	RFc-J_2
1	1	0	Insertion loss	Isolation
1	0	1	Isolation	Insertion loss

"1"= 1.8 to 3.3 V.
"0"= 0 V.
For "1" > 3 V, V_{BIAS} is not necessary and may be left open ckt.
Any state other than described in the truth table will put the switch in an undefined state.

Absolute Maximum Ratings

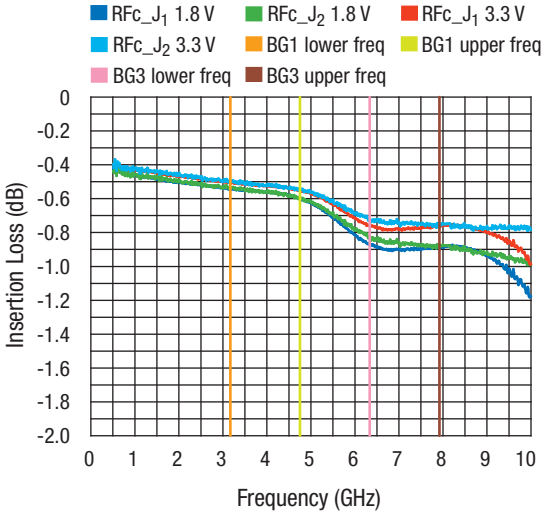
Characteristic	Value
V_{BIAS} voltage range	$1.8 \leq V_{BIAS} \leq 5$ V
RF input power @ 3 V	27 dBm
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +150 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

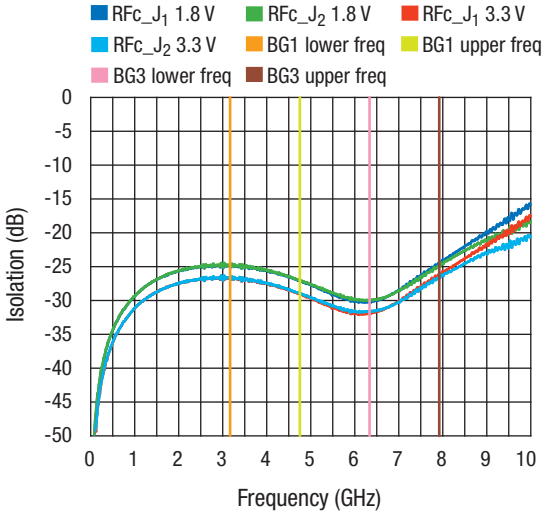
CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

Typical Performance Data

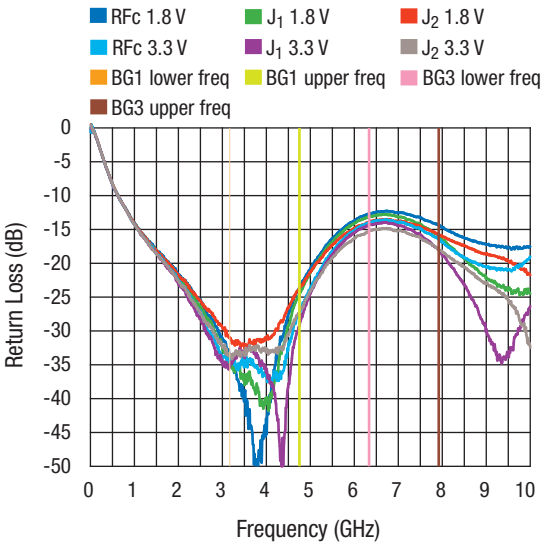
V_{BIAS} = 1.8 V, V_{CTL} = 0 V/1.8 V, and V_{BIAS} = Open Circuit, V_{CTL} = 0 V/3.3 V, T = 25 °C, P_{INPUT} = 0 dBm, Z_0 = 50 Ω, C_{BLK} = 15 pF, C_{BP} = 33 pF unless otherwise noted



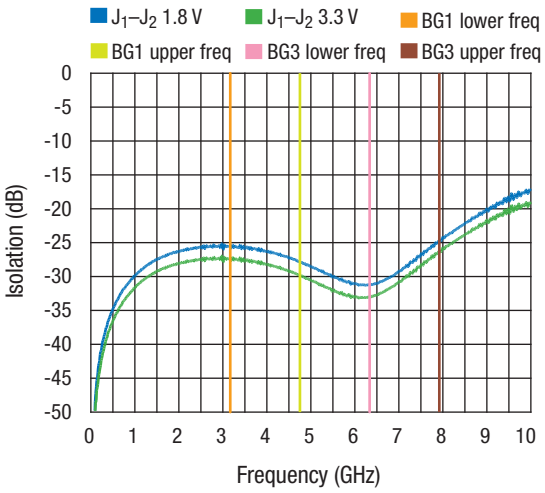
Typical Insertion Loss



Typical Isolation

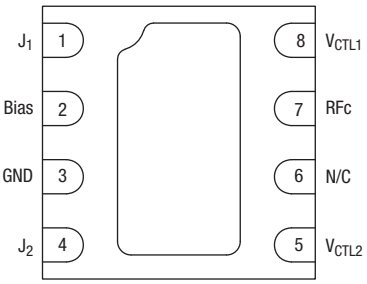


Return Loss (Ins. Loss state)



Typical J_1–J_2 Isolation

Pin Out (Top View)

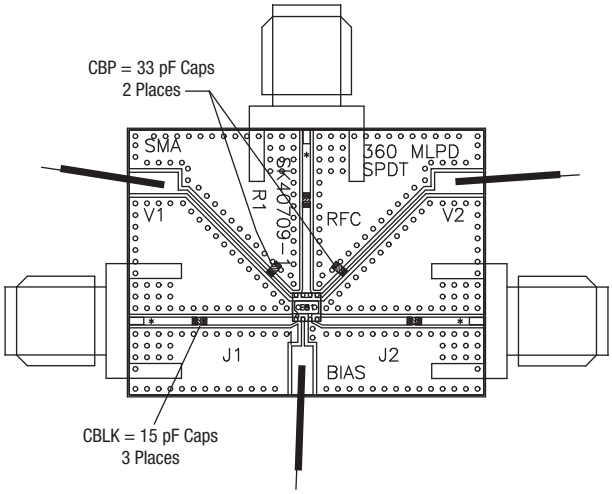


DC blocks are required on RFc, J_1, J_2.
C_{BLK} = 15 pF for UWB band operation.

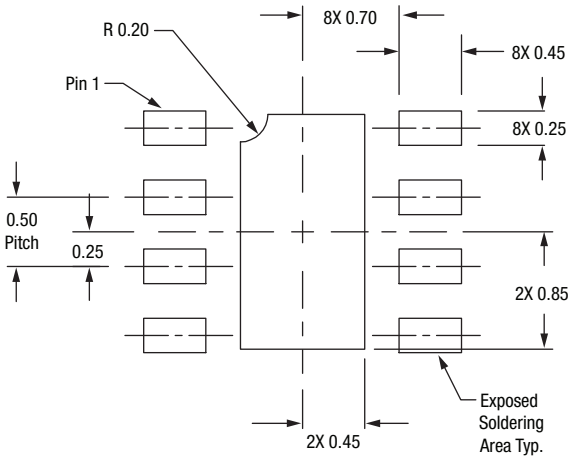
Pin Descriptions

Pin Number	Pin Name	Description
1	J_1	RF port
2	Bias	V_{BIAS}
3	Gnd	Gnd
4	J_2	RF port
5	V_{CTL2}	DC control voltage
6	N/C	No connect
7	RFc	RF common port
8	V_{CTL1}	DC control voltage
Exposed paddle	Paddle	Must be connected to RF ground

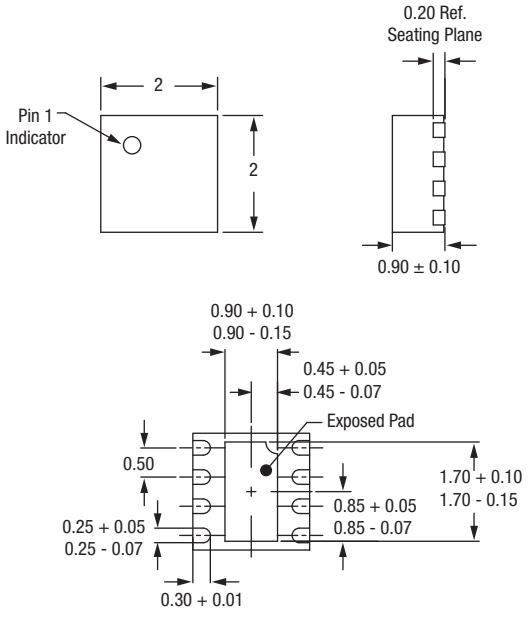
Evaluation Board



Suggested Land Pattern



QFN 8L 2 x 2 mm Package



Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.