DATA SHEET

SKY13473–569LF: 0.4 to 2.7 GHz SP10T LTE Transmit/Receive Switch with MIPI RFFE Interface

Applications

- 3G/4G multimode cellular tablets and handsets (LTE, UMTS, CDMA2000)
- Embedded data cards

Features

- Broadband frequency range: 0.4 to 2.7 GHz
- Low insertion loss
- High isolation and linearity
- Integrated, programmable MIPI interface
- Default USID = 1011
- Ten linear TRX ports with isolation greater than 20 dB @ 2.7 GHz
- Small QFN (20-pin, 2.4 x 2.4 x 0.75 mm) package (MSL1, 260 °C per JEDEC J-STD–020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Description

The SKY13473–569LF is a Single Pole, Ten Throw (SP10T) antenna switch with a Mobile Industry Processor Interface (MIPI) and is part of a two-switch family:

- SKY13473-569LF SP10T Antenna Switch with default USID = 1011 (this Data Sheet)
- SKY13473-12-569LF SP10T Antenna Switch with default USID = 1010 (Data Sheet #202983)

Using advanced switching technologies, the SKY13473–569LF maintains low insertion loss and high isolation for both transmit and receive switching paths. The high linearity performance and low insertion loss achieved by the SKY13473–569LF makes it an ideal choice for UMTS, CDMA2000, and LTE applications.

The switch also exhibits an excellent triple beat ratio and 2nd/3rd order Intermodulation Distortion (IMD) performance. Switching is controlled by an integrated MIPI interface. Depending on the logic applied to the decoder, the antenna pin is connected to one of 10 switched RF ports using a low insertion loss path, while the paths between the antenna pin and the other RF pins are in a high isolation state. No external DC blocking capacitors are required on the RF paths.

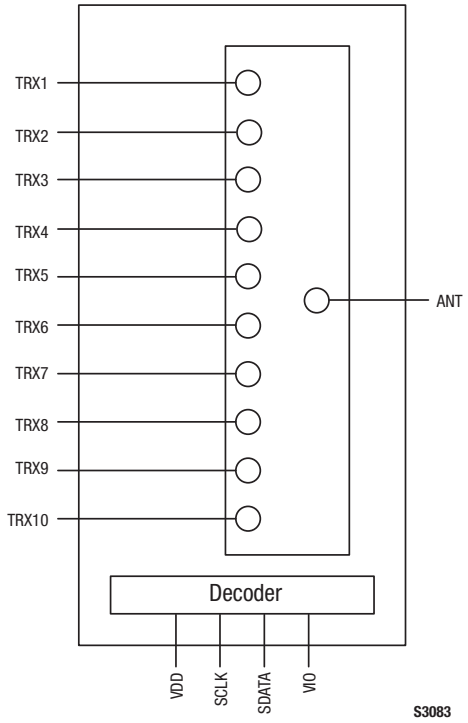


Figure 1. SKY13473–569LF Block Diagram

The SKY13473–569LF is manufactured in a compact, 2.4 x 2.4 x 0.75 mm, 20-pin surface mount Quad Flat No-Lead (QFN) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

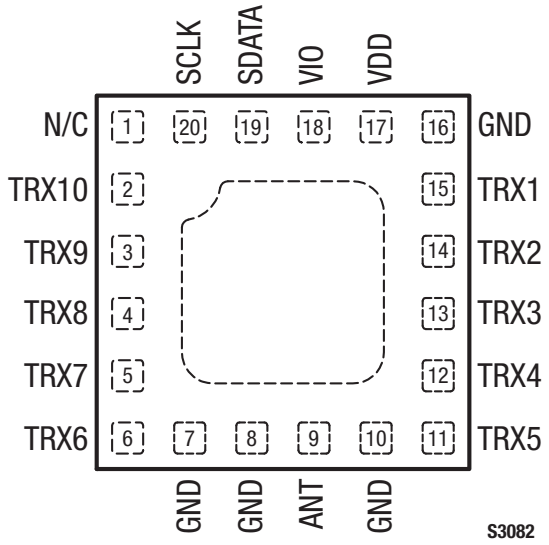


Figure 2. SKY13473–569LF Pinout – 20-Pin QFN (Top View)

Table 1. SKY13473–569LF Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	N/C	No connection. Can be grounded or left floating.	11	TRX5	Multi-band, multi-mode transmit/receive port #5. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.
2	TRX10	Multi-band, multi-mode transmit/receive port #10. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.	12	TRX4	Multi-band, multi-mode transmit/receive port #4. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.
3	TRX9	Multi-band, multi-mode transmit/receive port #9. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.	13	TRX3	Multi-band, multi-mode transmit/receive port #3. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.
4	TRX8	Multi-band, multi-mode transmit/receive port #8. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.	14	TRX2	Multi-band, multi-mode transmit/receive port #2. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.
5	TRX7	Multi-band, multi-mode transmit/receive port #7. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.	15	TRX1	Multi-band, multi-mode transmit/receive port #1. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.
6	TRX6	Multi-band, multi-mode transmit/receive port #6. This pin is either connected directly to or is disconnected from pin 9, depending on the control data applied to pin 19.	16	GND	Ground
7	GND	Ground	17	VDD	DC power supply
8	GND	Ground	18	VIO	MIPI decoder Interface/reference voltage
9	ANT	Antenna input/output	19	SDATA	Data input/output
10	GND	Ground	20	SCLK	Clock signal

Table 2. SKY13473–569LF Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Power supply	V_{DD}	2.5	5.0	V
Digital control signal	VIO		2	V
RF input power	P_{IN}		+33	dBm
Storage temperature	T_{STG}	–55	+150	°C
Operating temperature	T_{OP}	–40	+90	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13473–569LF are provided in Table 2. Electrical specifications are provided in Tables 3 through 6. Figure 3 provides the timing diagram for turn-on time and switching time.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 7 and 8, respectively.

Triple Beat Ratio (TBR) test conditions for bands 2 and 5 are listed in Table 9.

Figure 4 illustrates the test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA Band 1 linearity of the antenna switch. A +20 dBm Continuous Wave (CW) signal, f_{FUND}, is sequentially applied to the TRX1 through TRX10 ports, while a –15 dBm CW blocker signal, f_{BLK}, is applied to the ANT port.

The resulting 3rd Order Intermodulation Distortion (IMD3), f_{RX}, is measured over all phases of f_{FUND}. The SKY13473–569LF exhibits exceptional performance for all TRXx ports.

Table 10 describes the register content and programming read/write sequences. Refer to the *MIPI Alliance Specification for RF Front-End Control Interface (RFFE)*, v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.

Figures 5 and 6 provide the timing diagrams for register write commands and read commands, respectively.

Table 11 provides the Register_0 logic. Table 12 describes the register parameters and bit values.

Table 3. SKY13473–569LF General Electrical Specifications (Note 1)
(V_{DD} = 2.85 V, VIO = 1.8 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply voltage	V_{DD}		2.50	2.85	4.80	V
Supply current, active mode	I_{DD}			35	80	µA
Supply current, low power mode	I_{DD}			10		µA
Interface supply	VIO		1.65	1.80	1.95	V
Interface signal: High Low			 0.8 x VIO		 0.2 x VIO	 V V
Control current: High Low	I_{CTL}				 10 5	 µA µA
Turn-on time (Note 2)	t_{ON}	Measured from 50% of final V_{DD} supply voltage to 90% of RF power		20		µs
Switching time (Note 2)	t_{SW}	Measured from the rising edge of last clock signal to 90% RF power		2	5	µs

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: PIN = +27 dBm, TA = –40 to +90 °C. See Figure 3.

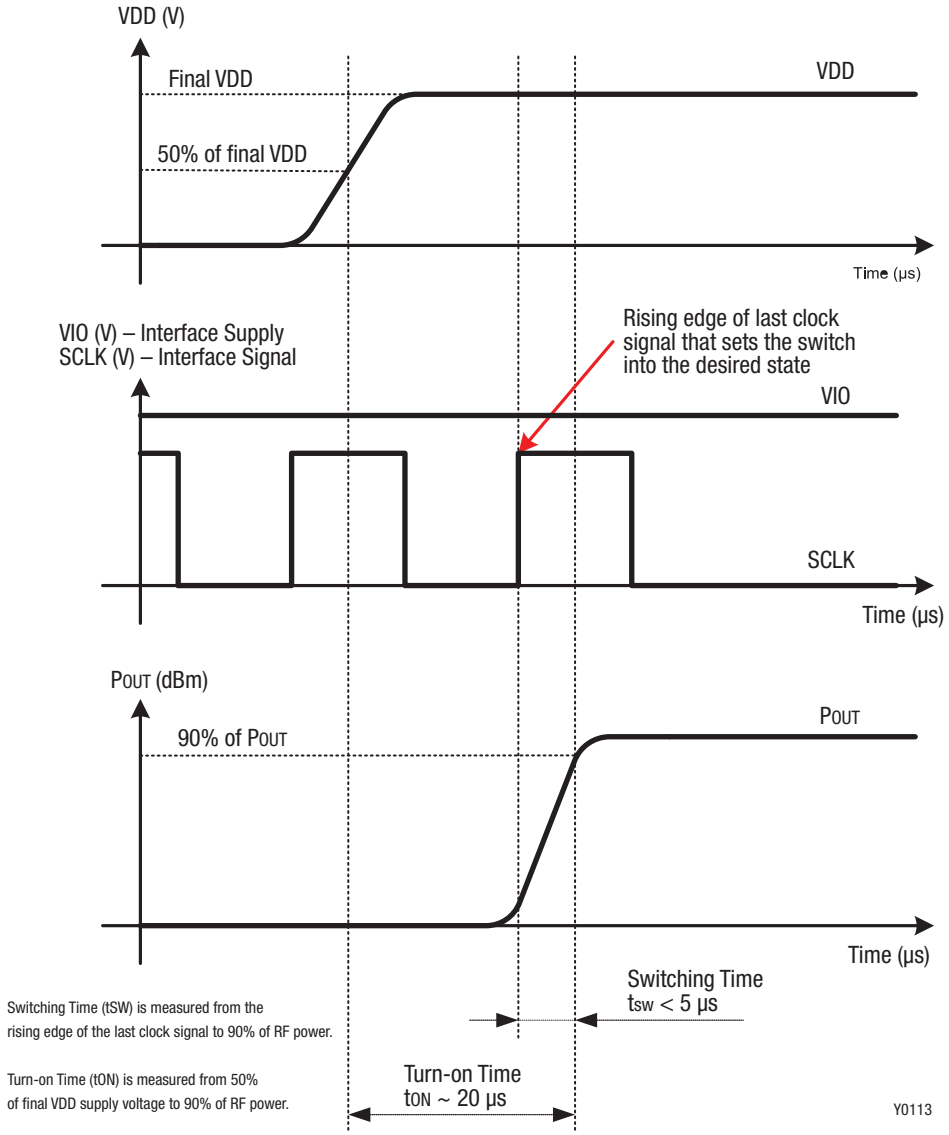


Figure 3. SKY13473-569LF Timing Diagram

Table 4. SKY13473–569LF RF Electrical Specifications (1 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Operating frequency	f		0.4		2.7	GHz
Insertion loss	IL	Up to 1.0 GHz Up to 2.0 GHz Up to 2.7 GHz		0.45 0.60 0.80	0.65 0.80 0.95	dB dB dB
Isolation (ANT port to any receive port) (see Table 5)	Iso	Up to 1.0 GHz Up to 2.0 GHz Up to 2.7 GHz	30 25 20	37 30 27		dB dB dB
Return loss	RL	All ports, up to 1.0 GHz All ports, up to 2.0 GHz All ports, up to 2.7 GHz	20 20	25 25 14		dB dB dB
Triple Beat Ratio	TBR	650 to 900 MHz 1710 to 2155 MHz (also see Table 9)	+81 +81	+93 +94		dBc dBc
2nd Order Intermodulation	IMD2	See Table 7		–110	–105	dBm
3rd Order Intermodulation	IMD3	See Table 8		–110	–105	dBm
Band 13 2nd harmonic	2fo	TRX1 to TRX10, P_{IN} = +25 dBm, fo = 782 MHz		–80	–78	dBm
Band 17 3rd harmonic	3fo	TRX1 to TRX10, P_{IN} = +25 dBm, fo = 707 MHz		–80	–78	dBm
Low band 2nd harmonic	2fo	TRX1 to TRX10, P_{IN} = +27 dBm, fo = 900 MHz		–80	–72	dBm
Low band 3rd harmonic	3fo	TRX1 to TRX10, P_{IN} = +27 dBm, fo = 900 MHz		–74	–66	dBm

Table 4. SKY13473–569LF RF Electrical Specifications (2 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
High band 2nd harmonic	2fo	TRX1 to TRX10, P_{IN} = +27 dBm, fo = 2690 MHz		–70	–62	dBm
High band 3rd harmonic	3fo	TRX1 to TRX10, P_{IN} = +27 dBm, fo = 2690 MHz		–68	–60	dBm

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 5. SKY13473–569LF RF Electrical Specifications: Isolation, ANT to TRX Ports (1 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Closed Path	Frequency (MHz)	Isolation (dB)									
		TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10
TRX1	915	–	–39	–43	–43	–38	–45	–49	–49	–52	–54
TRX1	1910	–	–31	–32	–36	–32	–39	–43	–41	–44	–46
TRX1	2690	–	–29	–28	–32	–28	–36	–39	–37	–40	–42
TRX2	915	–46	–	–48	–48	–39	–45	–49	–49	–52	–53
TRX2	1910	–35	–	–35	–37	–32	–39	–43	–41	–44	–46
TRX2	2690	–32	–	–30	–33	–28	–36	–39	–37	–40	–42
TRX3	915	–50	–44	–	–42	–41	–46	–49	–49	–52	–52
TRX3	1910	–38	–35	–	–34	–32	–40	–43	–42	–44	–45
TRX3	2690	–34	–32	–	–31	–28	–36	–39	–37	–40	–41
TRX4	915	–46	–47	–39	–	–46	–46	–49	–49	–51	–52
TRX4	1910	–37	–34	–31	–	–33	–40	–43	–42	–44	–45
TRX4	2690	–33	–29	–27	–	–29	–36	–39	–37	–39	–41
TRX5	915	–45	–45	–48	–43	–	–47	–50	–49	–52	–52
TRX5	1910	–37	–35	–35	–34	–	–40	–43	–42	–44	–45
TRX5	2690	–33	–31	–30	–32	–	–36	–39	–37	–39	–41
TRX6	915	–52	–51	–48	–47	–42	–	–43	–48	–44	–45
TRX6	1910	–45	–44	–40	–41	–36	–	–35	–35	–35	–37
TRX6	2690	–41	–40	–36	–37	–33	–	–32	–29	–30	–32
TRX7	915	–52	–51	–47	–47	–42	–46	–	–39	–46	–46
TRX7	1910	–45	–44	–40	–41	–36	–35	–	–31	–34	–37
TRX7	2690	–42	–40	–36	–37	–33	–31	–	–27	–29	–33
TRX8	915	–53	–51	–47	–46	–42	–43	–42	–	–43	–50
TRX8	1910	–45	–44	–40	–40	–36	–34	–34	–	–34	–38
TRX8	2690	–42	–40	–36	–37	–32	–30	–31	–	–31	–33

Table 5. SKY13473–569LF RF Electrical Specifications: Isolation, ANT to TRX Ports (2 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Closed Path	Frequency (MHz)	Isolation (dB)									
		TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10
TRX9	915	–53	–52	–47	–46	–41	–42	–50	–47	–	–43
TRX9	1910	–46	–44	–40	–40	–36	–34	–38	–34	–	–34
TRX9	2690	–42	–40	–36	–37	–32	–30	–34	–30	–	–31
TRX10	915	–54	–53	–47	–46	–41	–41	–45	–43	–38	–
TRX10	1910	–46	–45	–40	–40	–36	–34	–37	–32	–31	–
TRX10	2690	–42	–40	–36	–37	–32	–30	–33	–27	–28	–

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 6. SKY13473–569LF RF Electrical Specifications: Isolation, TRX to TRX Ports (1 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Closed Path	Frequency (MHz)	Isolation (dB)									
		TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10
TRX1	915	–	–31	–41	–43	–52	–57	–59	–57	–53	–53
TRX1	1910	–	–25	–34	–35	–39	–47	–48	–46	–44	–46
TRX1	2690	–	–21	–29	–32	–35	–44	–44	–41	–40	–42
TRX2	915	–33	–	–34	–39	–49	–57	–59	–57	–53	–54
TRX2	1910	–27	–	–28	–32	–38	–47	–48	–46	–45	–46
TRX2	2690	–24	–	–24	–29	–34	–44	–44	–41	–40	–42
TRX3	915	–39	–33	–	–32	–44	–58	–59	–57	–54	–55
TRX3	1910	–33	–27	–	–26	–35	–47	–48	–45	–45	–47
TRX3	2690	–29	–23	–	–22	–31	–43	–44	–41	–40	–43
TRX4	915	–42	–38	–31	–	–34	–58	–58	–56	–54	–55
TRX4	1910	–35	–32	–25	–	–27	–46	–47	–45	–45	–47
TRX4	2690	–31	–27	–21	–	–23	–42	–43	–40	–40	–43
TRX5	915	–43	–41	–37	–32	–	–58	–56	–55	–54	–55
TRX5	1910	–36	–34	–30	–26	–	–45	–47	–45	–45	–47
TRX5	2690	–32	–29	–26	–23	–	–41	–42	–40	–40	–43
TRX6	915	–55	–54	–58	–60	–51	–	–32	–37	–41	–43
TRX6	1910	–47	–45	–45	–47	–43	–	–26	–30	–34	–36
TRX6	2690	–43	–40	–40	–43	–40	–	–23	–26	–30	–32
TRX7	915	–55	–54	–58	–60	–50	–34	–	–31	–38	–41
TRX7	1910	–47	–45	–46	–48	–43	–27	–	–25	–32	–35
TRX7	2690	–43	–41	–41	–44	–40	–24	–	–21	–28	–31

Table 6. SKY13473–569LF RF Electrical Specifications: Isolation, TRX to TRX Ports (2 of 2) (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Closed Path	Frequency (MHz)	Isolation (dB)									
		TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10
TRX8	915	–55	–54	–59	–61	–49	–42	–32	–	–32	–39
TRX8	1910	–47	–45	–46	–48	–42	–35	–26	–	–26	–33
TRX8	2690	–43	–40	–41	–44	–40	–31	–22	–	–23	–29
TRX9	915	–54	–54	–59	–60	–49	–45	–39	–34	–	–32
TRX9	1910	–46	–45	–46	–48	–42	–37	–32	–28	–	–26
TRX9	2690	–42	–40	–41	–44	–41	–33	–28	–24	–	–23
TRX10	915	–53	–53	–59	–60	–49	–47	–41	–40	–30	–
TRX10	1910	–46	–44	–46	–48	–42	–38	–35	–33	–24	–
TRX10	2690	–42	–40	–42	–44	–41	–34	–31	–29	–21	–

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 7. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	–15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 8. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	–15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Table 9. Triple Beat Ratio Test Conditions

Band	Transmit Frequency 1 (MHz)	Transmit Power 1 (dBm)	Transmit Frequency 2 (MHz)	Transmit Power 2 (dBm)	Frequency Blocker @ ANT (MHz)	Power Blocker (dBm)	TBR Product Frequency (MHz)
2	1880.0	+21.5	1881.0	+21.5	1960.0	–30	1960.0 ± 1
5	835.5		836.5		881.5		881.5 ± 1

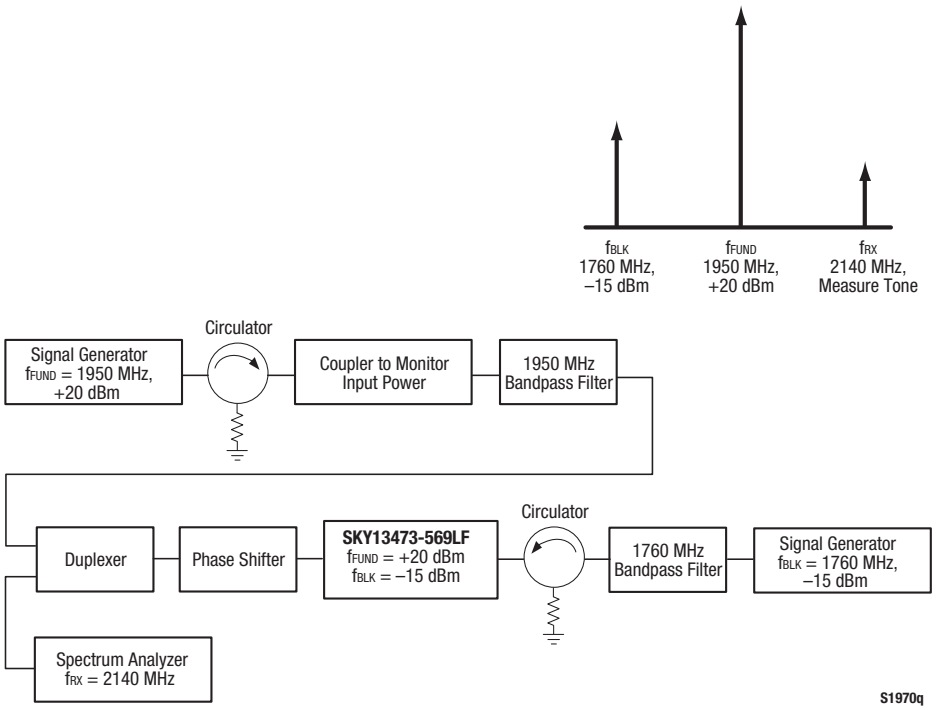


Figure 4. 3rd Order Intermodulation Test Setup

Table 10. Command Sequence Bit Definitions

Type	SSC	C11-C8	C7	C6-C5	C4	C3-C0	Parity Bits	BPC	Extended Operation					
									DA7(1)-DA0(1)	Parity Bits	BPC	DA7(n)-DA0(n)	Parity Bits	BPC
Reg0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data{3:0]	Y	Y	–	–	–	–	–	–
Reg Write	Y	SA[3:0]	0	10	Addr[4]	Addr[3:0]	Y	–	Data[7:0]	–	–	–	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Addr[3:0]	Y	Y	Data[7:0]	–	–	–	Y	Y

Legend:
SSC = Sequence start command
C = Command frame bits
DA = Data/address frame bits
BPC = Bus park cycle
BC = Byte count (# of consecutive addresses)

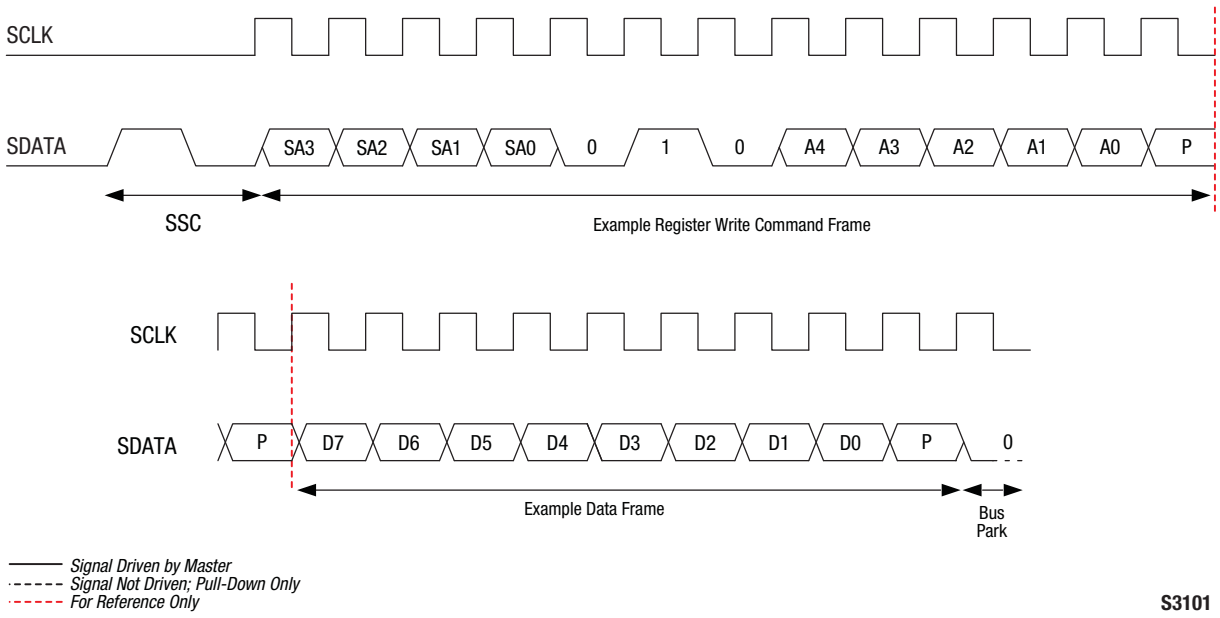


Figure 5. Register Write Command Timing Diagram

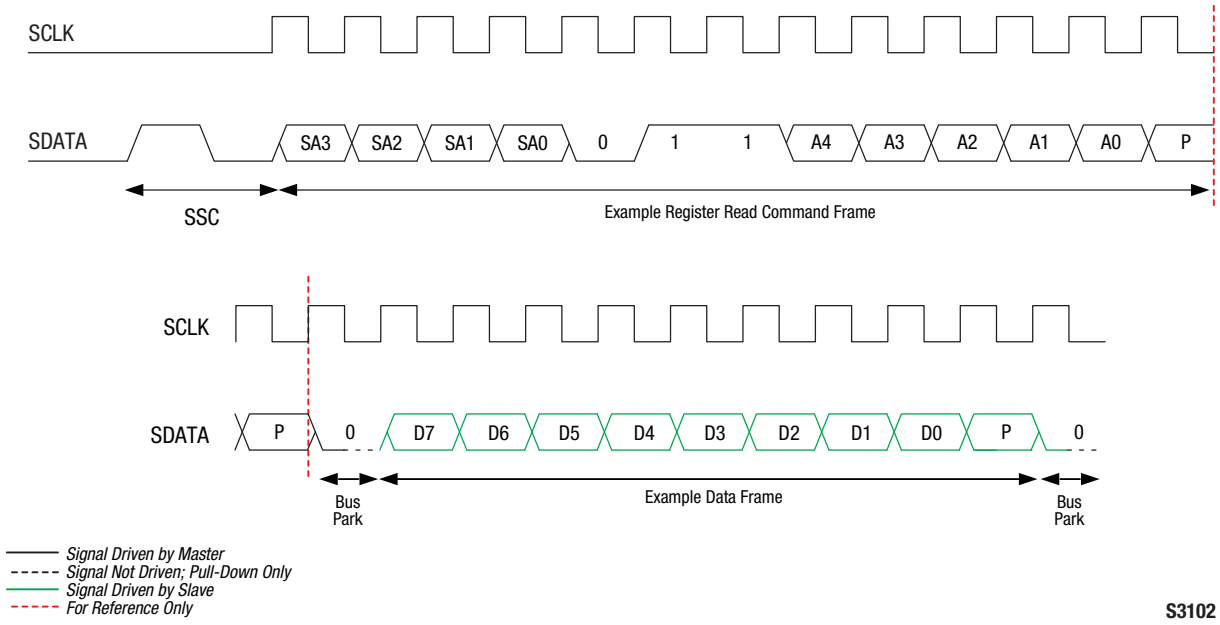


Figure 6. Register Read Command Timing Diagram

Table 11. Register_0 Truth Table

State	Mode	Register_0 Bits							
		D7	D6	D5	D4	D3	D2	D1	D0
1	Isolation (default)	x	0	0	0	0	0	0	0
2	TRX1	x	0	0	0	0	0	1	0
3	TRX2	x	0	0	0	1	0	1	0
4	TRX3	x	0	0	0	1	1	1	0
5	TRX4	x	0	0	0	1	0	1	1
6	TRX5	x	0	0	0	0	0	0	1
7	TRX6	x	0	0	0	1	0	0	1
8	TRX7	x	0	0	0	0	1	1	0
9	TRX8	x	0	0	0	0	1	0	0
10	TRX9	x	0	0	0	1	1	0	0
11	TRX10	x	0	0	0	1	0	0	0

Table 12. Register Description and Programming (1 of 2)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
Register_0	0000	MODE_CTRL	Bits[7:0]: Switch control. See Table 10 for logic	–
RFFE_STATUS	001A	SOFTWARE RESET	Bit[7]: Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register. 0 = Normal operation 1 = Software reset	0
		COMMAND_FRAME_PARITY_ERR	Bit[6]: Command sequence received with parity error – discard command.	0
		COMMAND_LENGTH_ERR	Bit[5]: Command length error.	0
		ADDRESS_FRAME_PARITY_ERR	Bit[4]: Address frame parity error =1.	0
		DATA_FRAME_PARITY_ERR	Bit[3]: Data frame with parity error.	0
		READ_UNUSED_REG	Bit[2]: Read command to an invalid address.	0
		WRITE_UNUSED_REG	Bit[1]: Write command to an invalid address.	0
		BID_GID_ERR	Bit[0]: Read command with a BROADCAST_ID (refer to the *MIPI Alliance Specification*) or GSID.	0
GROUP_SID	001B	Reserved	Bits[7:4]: Reserved	0000
		GSID	Bits[3:0]: Group slave ID	0000

Table 12. Register Description and Programming (2 of 2)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
PM_TRIG (Note 1)	001C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	00
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	0
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	0
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers.	0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers.	0
PRODUCT_ID	001D	PRODUCT_ID	Bits[7:0]: This is a read-only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	01000101
MANUFACTURER_ID	001E	MANUFACTURER_ID	Bits[7:0]: Read-only register	10100101
MAN_USID	001F	Reserved	Bits[7:6]: Reserved	00
		MANUFACTURER_ID	Bits[5:4]: Read-only register	01
		USID	Bits[3:0]: Programmable USID. A write to these bits programs the USID.	1011

Note 1: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively, as described in the MIPI RFFE Specification, this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Evaluation Board Description

The SKY13473–569LF Evaluation Board is used to test the performance of the SKY13473–569LF SP10T Switch. An Evaluation Board schematic diagram is provided in Figure 7. A recommended ESD protection circuit diagram is provided in Figure 8. An assembly drawing for the Evaluation Board is shown in Figure 9.

Package Dimensions

The PCB layout footprint for the SKY13473–569LF is provided in Figure 10. Typical case markings are shown in Figure 11. Package dimensions for the 20-pin QFN are shown in Figure 12, and tape and reel dimensions are provided in Figure 13.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13473–569LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

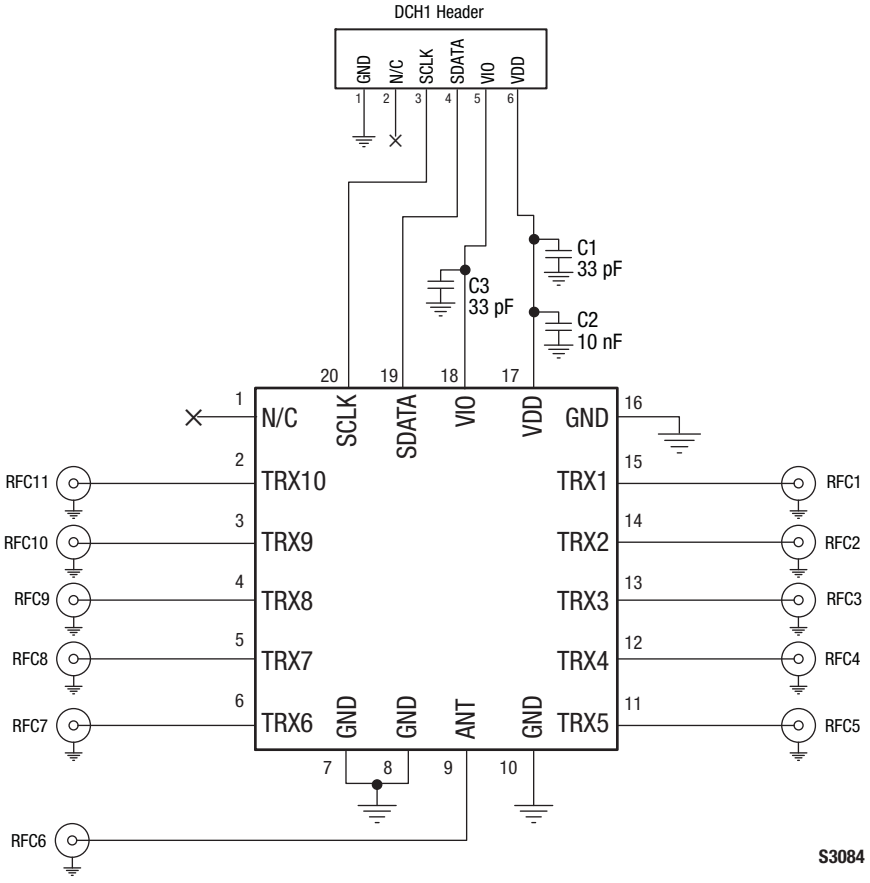


Figure 7. SKY13473–569LF Evaluation Board Schematic

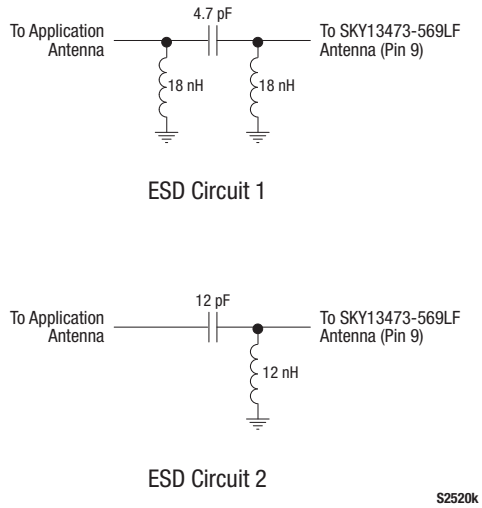


Figure 8. SKY13473–569LF Recommended ESD Protection Circuits

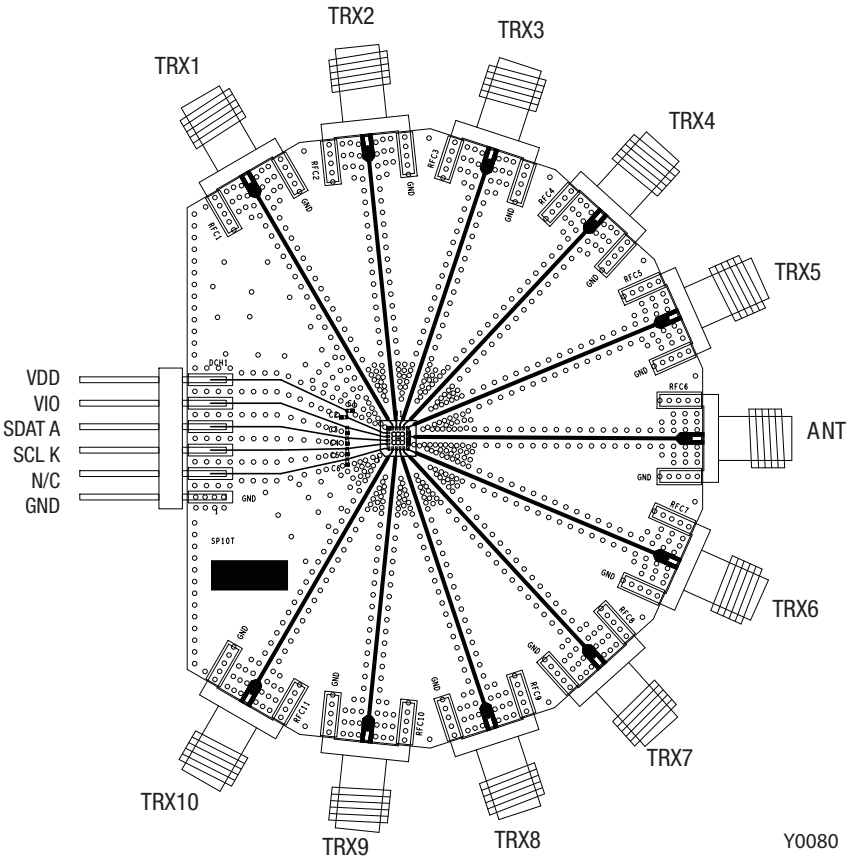
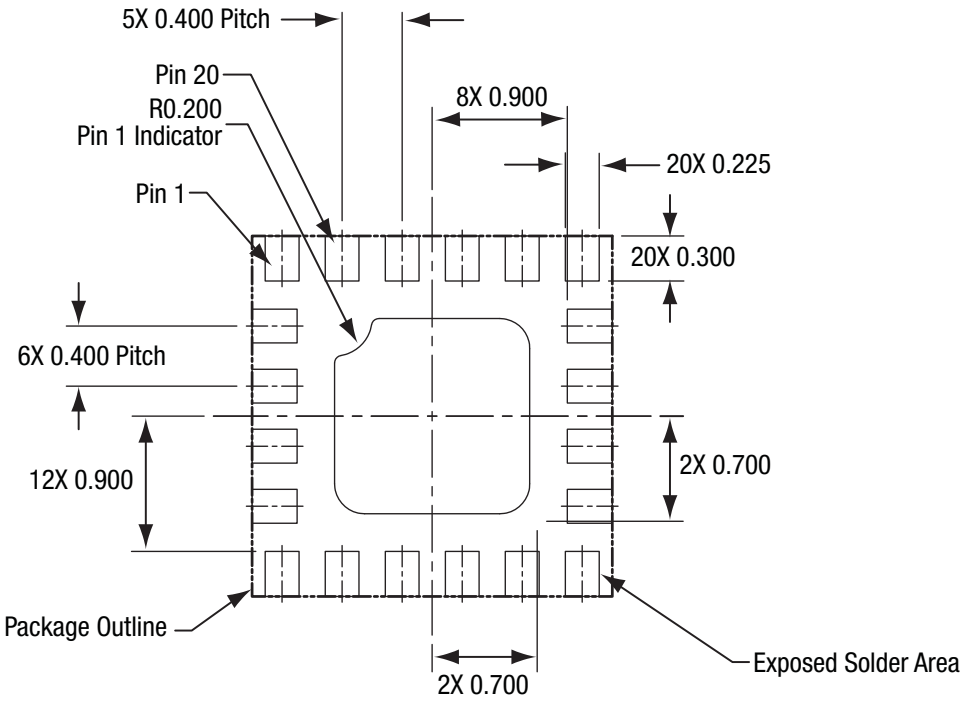


Figure 9. SKY13473–569LF Evaluation Board Assembly Diagram



All dimensions are in millimeters **S3292**

Figure 10. SKY13473–569LF PCB Layout Footprint (Top View)

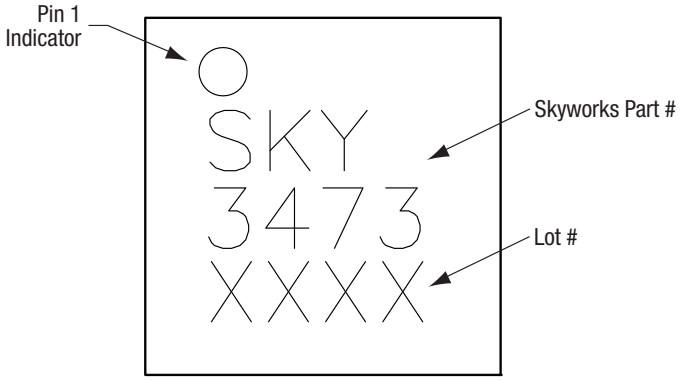
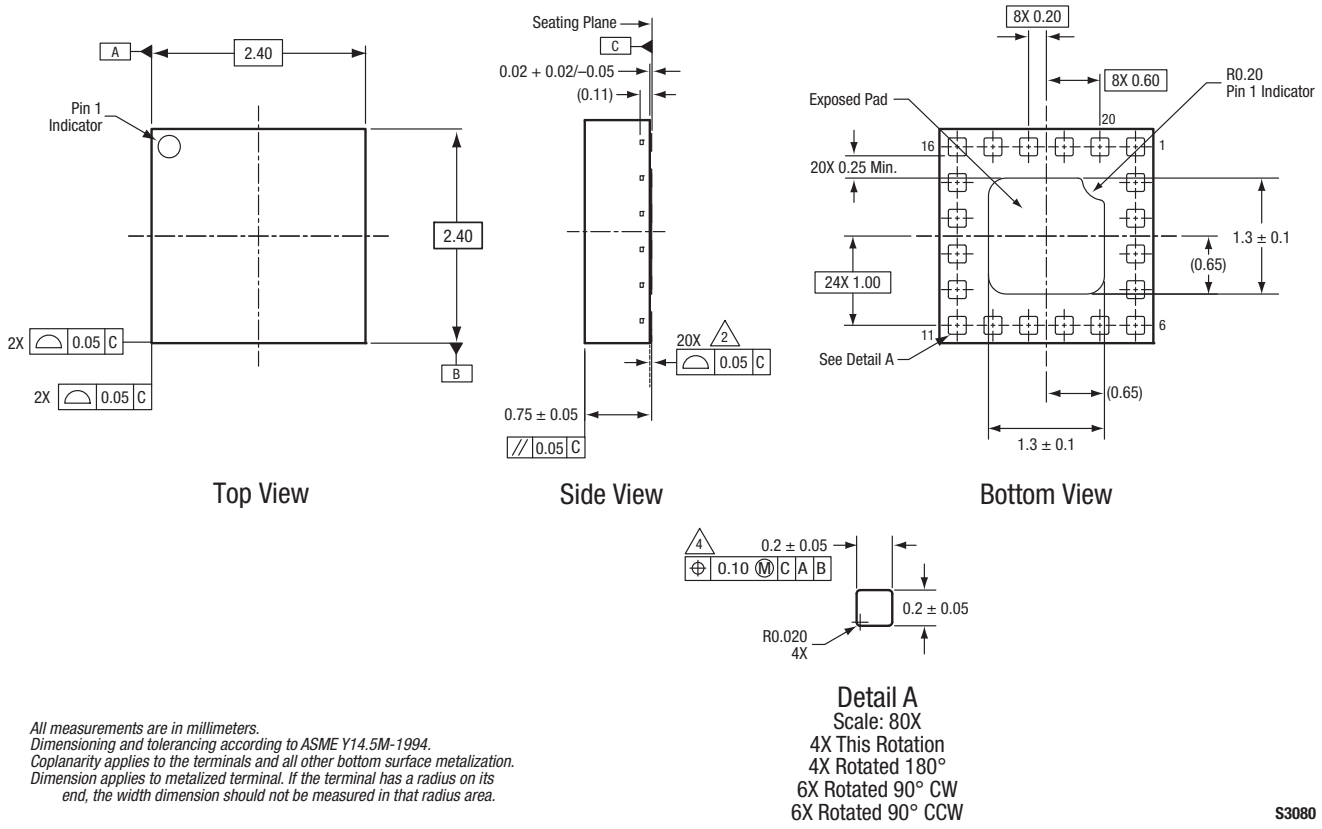
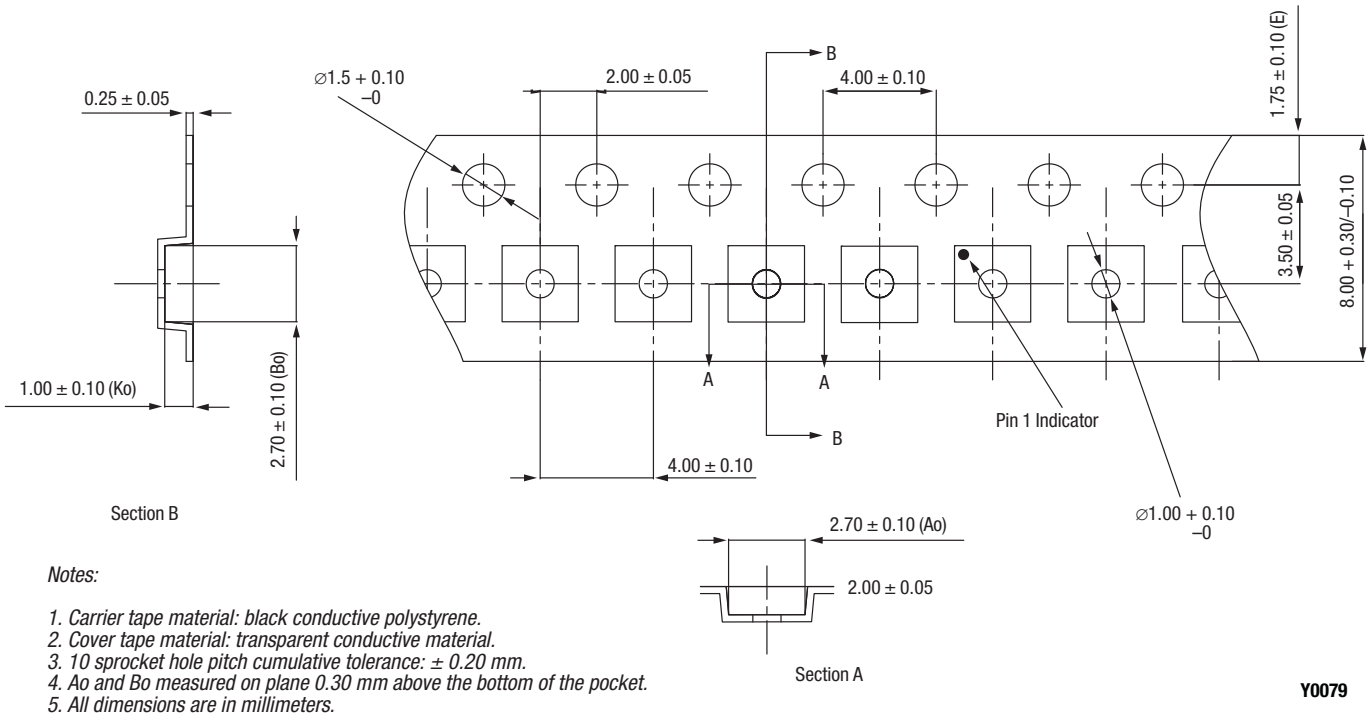


Figure 11. Typical Part Markings (Top View)



All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Coplanarity applies to the terminals and all other bottom surface metalization.
Dimension applies to metalized terminal. If the terminal has a radius on its end, the width dimension should not be measured in that radius area.

Figure 12. SKY13473–569LF 20-Pin QFN Package Dimensions



Notes:

1. Carrier tape material: black conductive polystyrene.
2. Cover tape material: transparent conductive material.
3. 10 sprocket hole pitch cumulative tolerance: ± 0.20 mm.
4. Ao and Bo measured on plane 0.30 mm above the bottom of the pocket.
5. All dimensions are in millimeters.

Figure 13. SKY13473–569LF Tape and Reel Dimensions