DATA SHEET

SKY65006-348LF-348LF: 2.4 to 2.5 GHz WLAN/ZigBee® Power Amplifier

Applications

- 2-stage InGaP power amplifier designed for 2.4 to 2.5 GHz ISM, IEEE 802.11b, 802.11g WLAN and ZigBee band applications

Features

- 2.4 to 2.5 GHz operation
- WLAN/ZigBee® applications
- Advanced GaAs HBT process
- Integrated output power detector and F2 filter
- Low voltage positive bias supply (3.3 V)
- Low quiescent current: 50 mA
- 27 dB small signal gain
- 802.11g linear power: +18 dBm (includes integrated filter loss)
- 802.11b mask-compliant power: +21 dBm (includes integrated filter loss)
- 802.15.4 mask-compliant power: +15.4 dBm (includes integrated filter loss)
- Low-cost 16-pin QFN (3 x 3 x 0.75 mm) plastic package
- Lead (Pb)-free, and RoHS-compliant

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

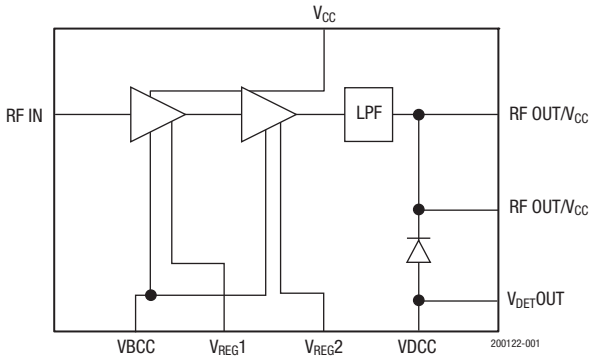


Figure 1. SKY65006-348LF Functional Block Diagram

Description

The SKY65006-348LF-348LF is a linear, high-gain two-stage power amplifier with integrated output power detector and second harmonic (F2) filter, designed for low voltage operations. This device is manufactured on an advanced Gallium Arsenide (GaAs), Heterojunction Bipolar Transistor (HBT) process. The device is designed for power amplifier applications in WLAN, ZigBee, and spread spectrum systems from 2.4 to 2.5 GHz. The amplifier is packaged in a QFN-16, 3 x 3 x 0.75 mm package.

The Skyworks SKY65006-348LF is a high-performance 2-stage InGaP power amplifier designed for 2.4 to 2.5 GHz ISM, IEEE 802.11b, 802.11g WLAN and ZigBee band applications. The SKY65006-348LF is a high-efficiency linear amplifier designed for single 3.3 V supply operation, requiring no input and output matching components for 50 Ω operation. This device also includes an internal power detector and integrated harmonic filter for reduced PC board component count. The integrated low pass filter is also highly effective in reducing harmonics at their source by localizing harmonic rejection to a tiny portion of the PA chip. This significantly reduces the risk of radiation from a high order filter design external to the amplifier. Filtering of harmonics in this way can eliminate the need for an external shield over the PA, and reduces overall cost.

A functional block diagram is provided in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

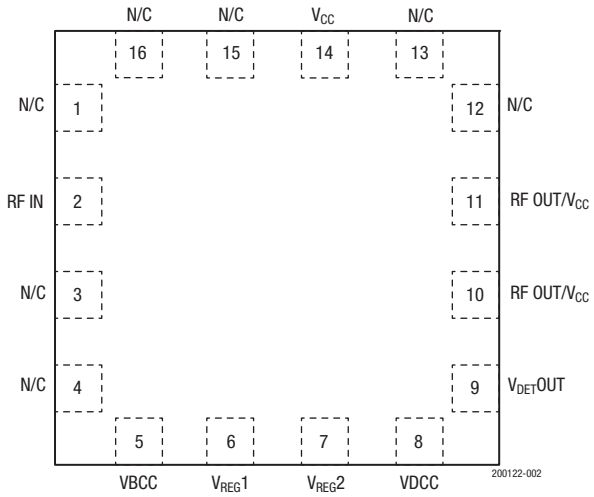


Figure 2. SKY65006-348LF Pinout

Table 1. SKY65006-348LF Signal Descriptions[1]

Pin	Name	Description
1, 3, 4, 12, 13, 15, 16	N/C	No connect
2	RF IN	RF input
5	VBCC	DC control voltage input that sets bias to the first and second amplifier stages.
6	$V_{REG}1$	DC control voltage input to regulate the current to the first amplifier stages.
7	$V_{REG}2$	DC control voltage input to regulate the current to the second amplifier stage.
8	VDCC	Reference voltage input to power detector.
9	V_{DET}	Power detector output voltage.
10, 11	RF OUT/V_{CC}	RF outputs and supply voltage inputs to second amplifier stage. These pins must be connected directly together for current sharing.
14	V_{CC}	DC supply voltage input to the first amplifier stage.
Center	GND	Equipotential point. Connect package backside center paddle to the printed circuit board common via the lowest possible impedance.

Electrical and Mechanical Specifications

The absolute maximum ratings for the SKY65006-348LF are provided in Table 2, and the general RF transmit electrical specifications are shown in Table 3. Electrical specifications are provided in Table 4.

Table 5 shows the DC voltage control information.

Typical performance characteristics of the SKY65006-348LF are illustrated in Figures 3 through 38.

Table 2. SKY65006-348LF Absolute Maximum Ratings
(T_A = +25 °C, Unless Otherwise Noted) [1]

Parameter	Symbol	Value	Units
Supply voltage	VCC	5	V
Supply current	I_{CC}	500	mA
Regulator supply voltage	(V_{REG}1 and V_{REG}2)	<V_{CC}	V
Operating temperature	T_C	-40 to +85	°C
Storage temperature range	T_{ST}	-55 to +125	°C
RF input power	P_{IN}	+10	dBm
Junction temperature	T_J	150	°C

[1] Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

***ESD HANDLING**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 3. RF Transmit Electrical Specifications
T_C = 25 °C, V_{CC} = 3.3 V, V_{REG} = 3 V, V_{DCC} = 3 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency range	f		2400		2500	MHz
Gain	$\|S_{21}\|$	Small signal	26	27		dB
Gain variation over frequency	$\|\Delta S_{21}\|$	Small signal		0.2		dB
Input return loss	$\|S_{11}\|$	Small signal		27		dB
Output return loss	$\|S_{22}\|$	Small signal		6.5		dB
Output $P_{1\ dB}$	$P_{1\ dB}$	CW	23	24		dBm
2nd harmonic	F_2	CW at $P_{1\ dB}$		-35		dBm
3rd harmonic	F_3	CW at $P_{1\ dB}$		-49		dBm
Detector voltage	V_{DET}	P_{OUT} = 10 dBm, 802.11g modulation		0.4		V
Noise figure	NF	Small signal		6.2	7	dB
PAE @ $P_{1\ dB}$	PAE	CW at $P_{1\ dB}$	26	29		%
Quiescent current	I_{CQ}	(No RF signal)		53		mA
Reference current	I_{REF}	(No RF signal)		6		mA
I_{CC} @ $P_{1\ dB}$	I_{CC}	at $P_{1\ dB}$		265		mA

Table 4. SKY65006-348LF Electrical Characteristics[1]
(V_{CC} = 3.3 V, T_C = 25 °C, V_{REG} = 3 V, V_{DCC} = 3 V Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
802.11g, OFDM Modulation, 54 Mbps						
Linear power at 2.442 GHz	P_{OUT}	54 Mbps at 3.5% EVM		17		dBm
Current consumption	I_{CC}	54 Mbps at linear power		130		mA
Detector voltage	V_{DET}	54 Mbps at linear power		1		V
802.11b, CCK Modulation, 11 Mbps[2]						
Compliant power at 2.442 GHz	P_{OUT}	11 Mbps		21.5		dBm
Current consumption	I_{CC}	11 Mbps at compliant power		190		mA
Detector voltage	V_{DET}	11 Mbps at compliant power		1.4		V
802.15.4, ZigBee O-QPSK Modulation, 250 Kb/s						
Frequency	f	Best OIP3 match		1960		MHz
Small signal gain	S21	P_{IN} = –15 dBm	10.5	12		dB

1 Performance is guaranteed only under the conditions listed in this table.

2 802.11b data is taken with a raised cosine filter and an alpha factor of 0.7.

Table 5. DC Voltage Control Table

Mode	V_{CC}	V_{REG}[1]	VBCC	VdCC
RF IN-RF OUT	3.3 V	3.0 V	3.3 V	3.0 V

1. Voltage applied at evaluation board DC pins.

Typical Performance Data

(V_{CC} = V_{BCC} = 3.3 V, V_{REF} = V_{DCC} = 3 V, ZO = 50 Ω, TC = 25 °C, Frequency = 2.442 GHz Unless Otherwise Noted)

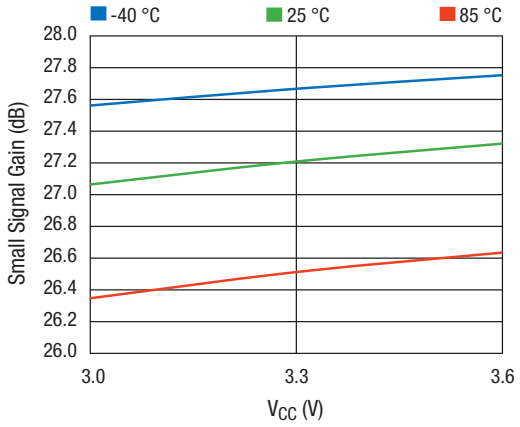


Figure 3. Small Signal Gain vs Vcc Across Temperature

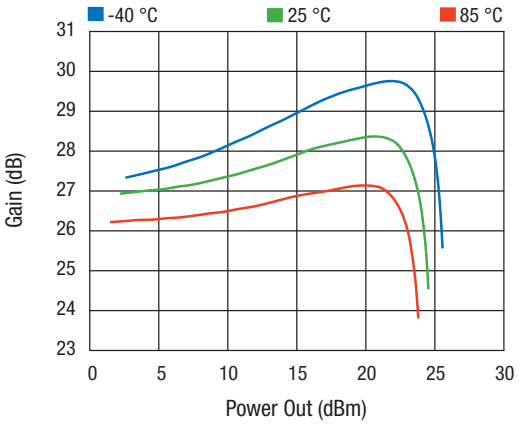


Figure 4. Gain vs Power Out Across Temperature

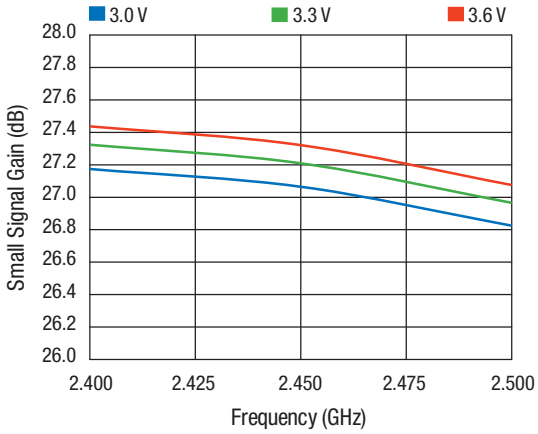


Figure 5. Small Signal Gain vs Frequency across Vcc

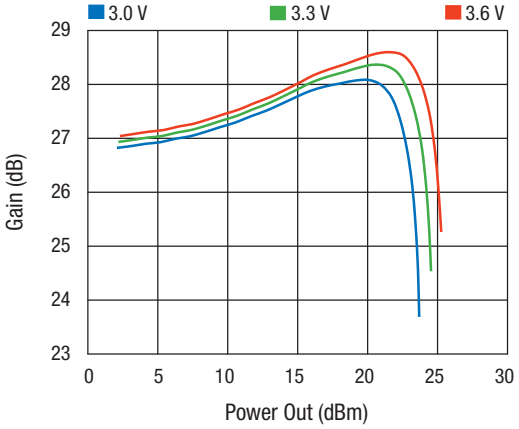


Figure 6. Gain vs Power Out Across Vcc

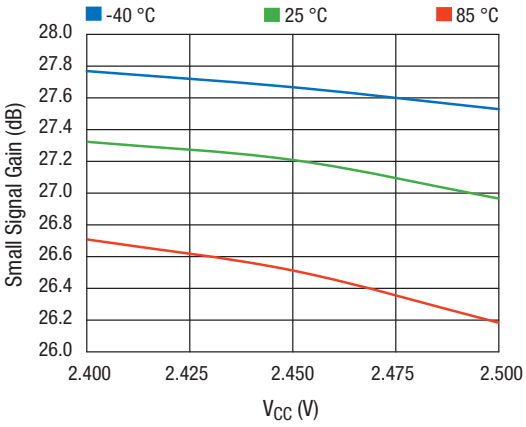


Figure 7. Small Signal Gain vs Frequency Across Temperature

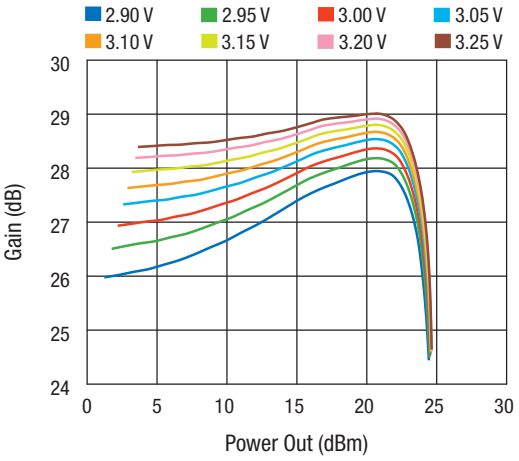


Figure 8. Gain vs Power Out Across V_{REG}

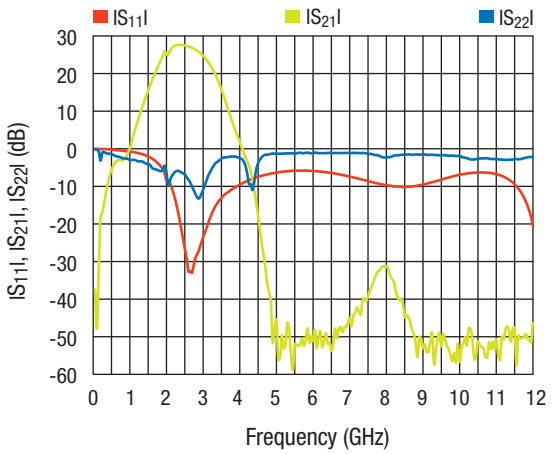


Figure 9. S-Parameters vs Frequency

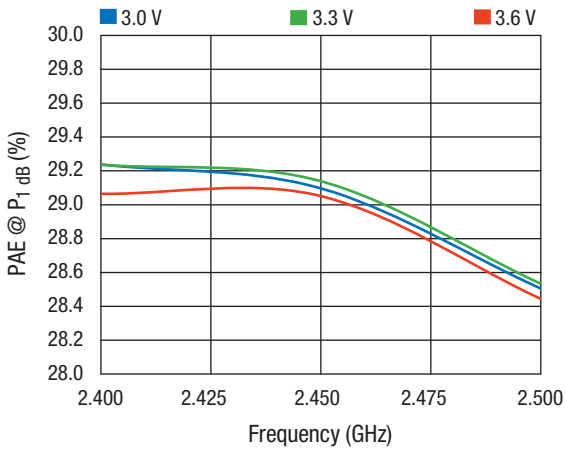


Figure 10. PAE @ P1dB vs Frequency Across Vcc

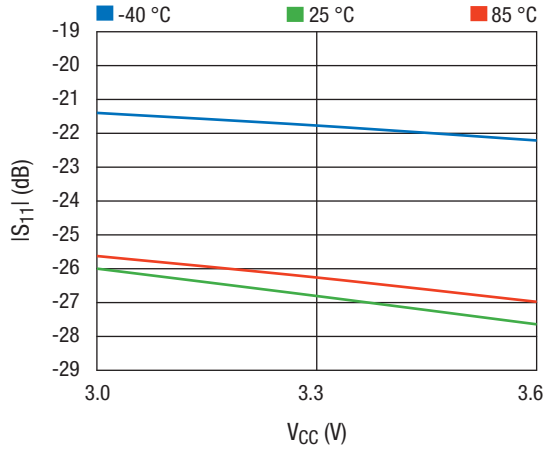


Figure 11. |S11| vs. Vcc Across Temperature

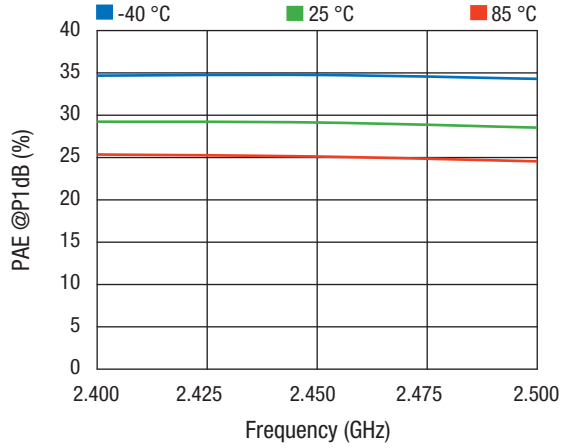


Figure 12. PAE @ P1dB vs Frequency Across Temperature

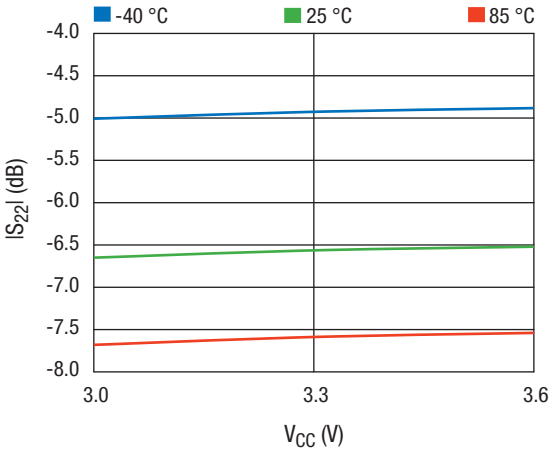


Figure 13. |S22| vs. Vcc Across Temperature

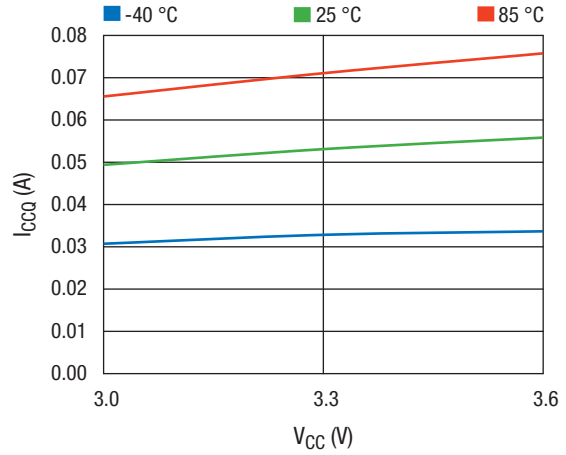


Figure 14. Iccq vs. Vcc Across Temperature

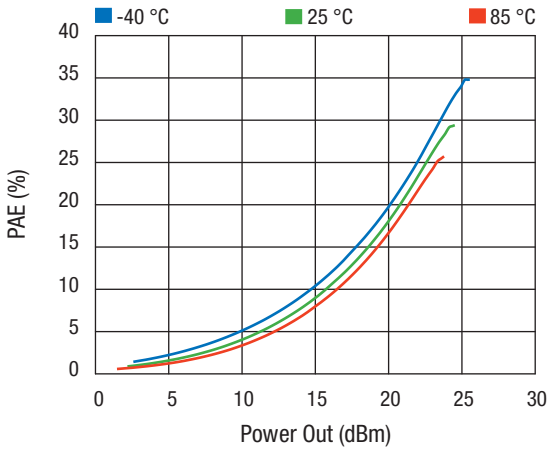


Figure 15. PAE @ P1dB vs Power Out Across Temperature

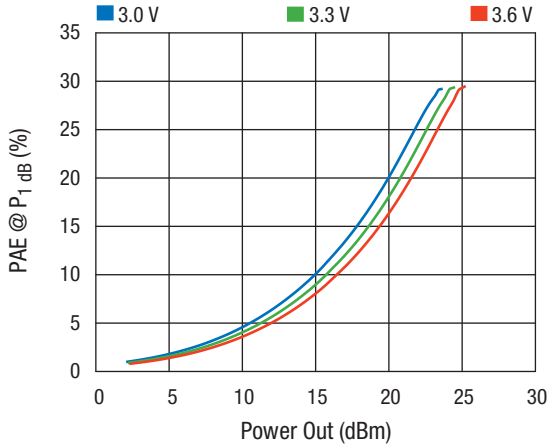


Figure 16. PAE @ P1dB vs Power Out Across Vcc

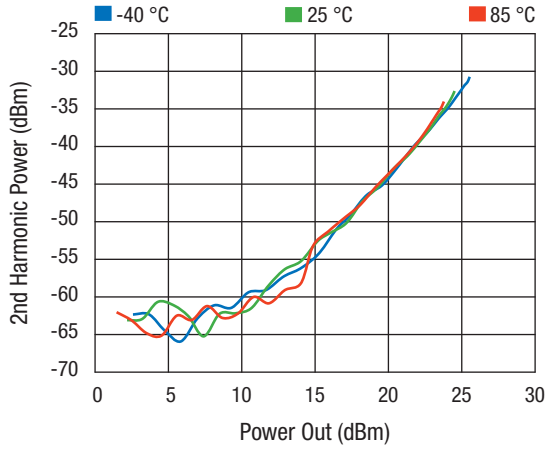


Figure 17. 2nd Harmonic vs. Power Out Across Temperature

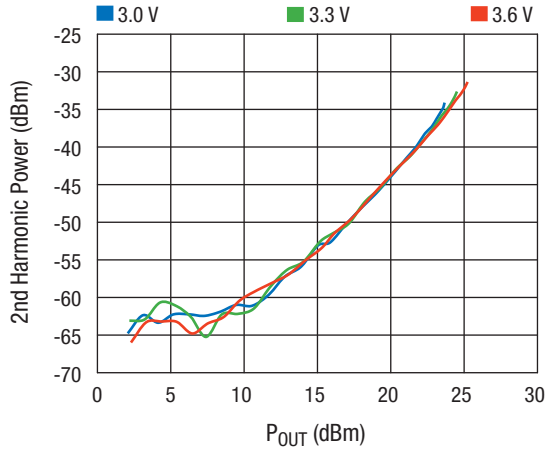


Figure 18. 2nd Harmonic vs. Power Out Across Vcc

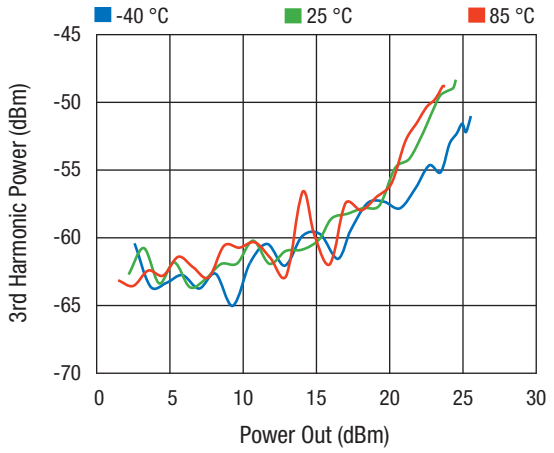


Figure 19. 3rd Harmonic vs. Power Out Across Temperature

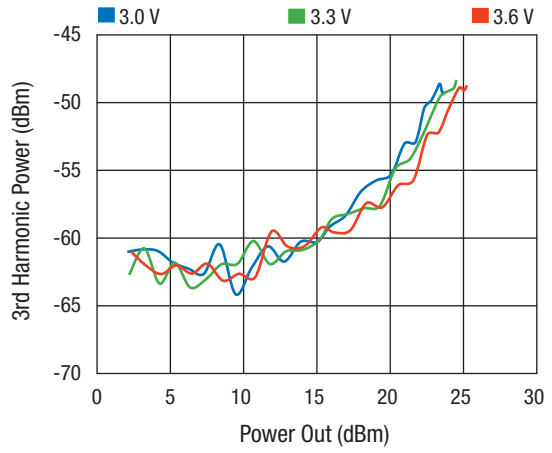


Figure 20. 3rd Harmonic vs. Power Out Across Vcc

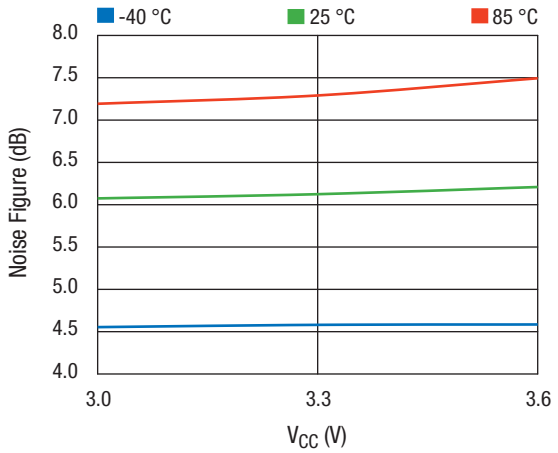


Figure 21. Noise Figure vs. Vcc Across Temperature

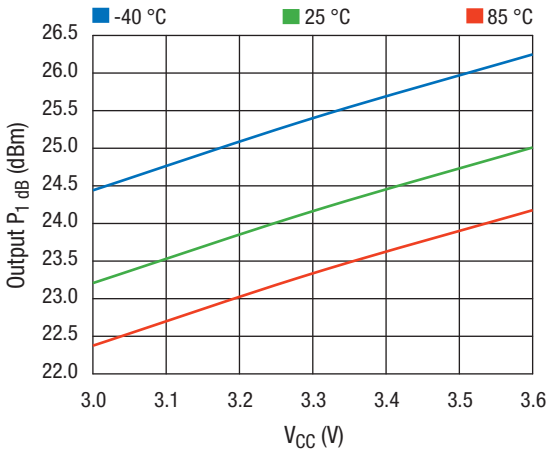


Figure 22. Output P1dB vs. Vcc Across Temperature

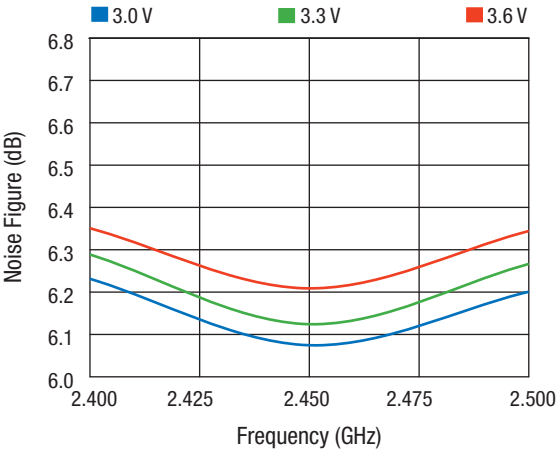


Figure 23. Noise Figure vs. Frequency Across Vcc

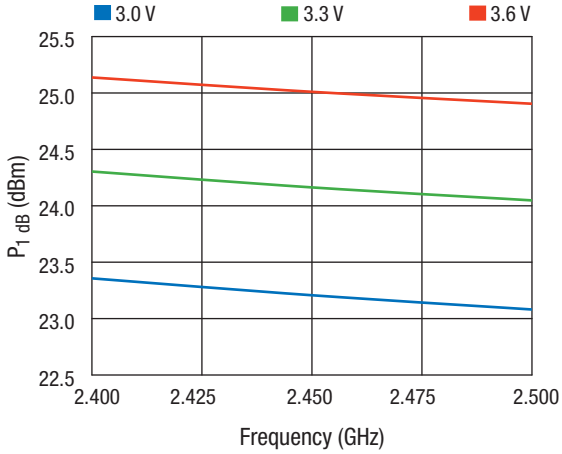


Figure 24. Output P1dB vs Frequency Across Vcc

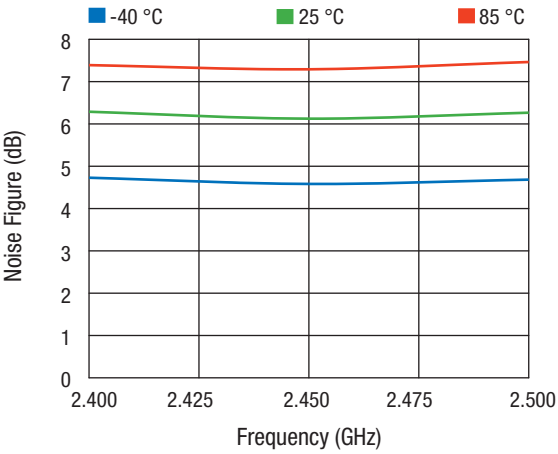


Figure 25. Noise Figure vs Frequency Across Temperature

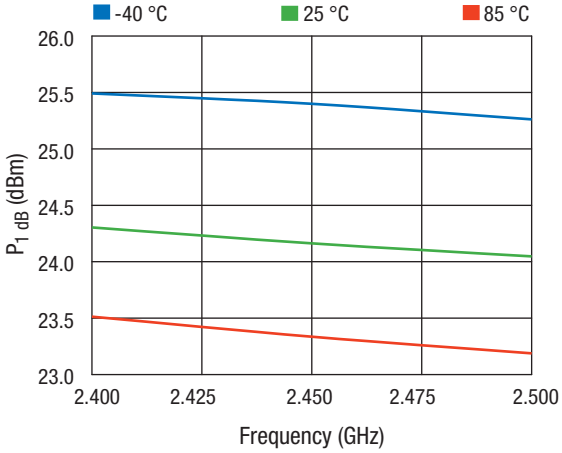


Figure 26. Output P1dB vs Frequency Across Temperature

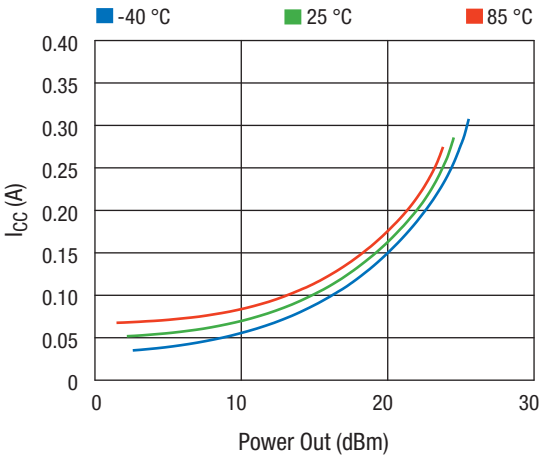


Figure 27. Icc vs Power Out Across Temperature

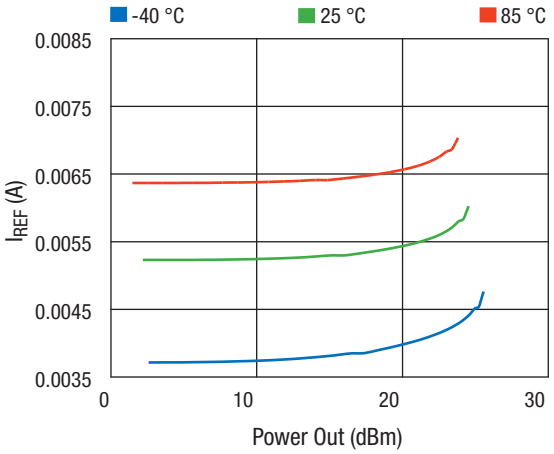


Figure 28. IREF vs Power Out Across Temperature

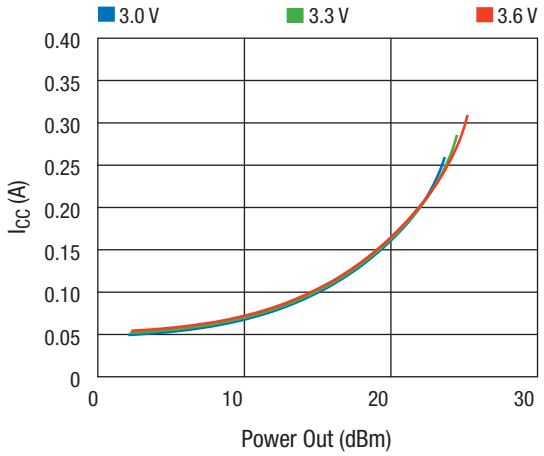


Figure 29. Icc vs Power Out Across Vcc

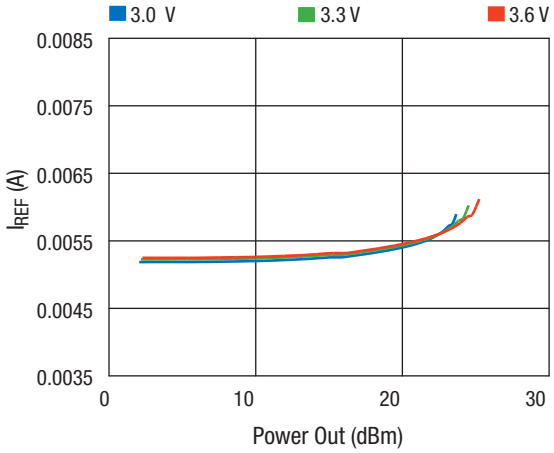


Figure 30. IREF vs Power Out Across Vcc

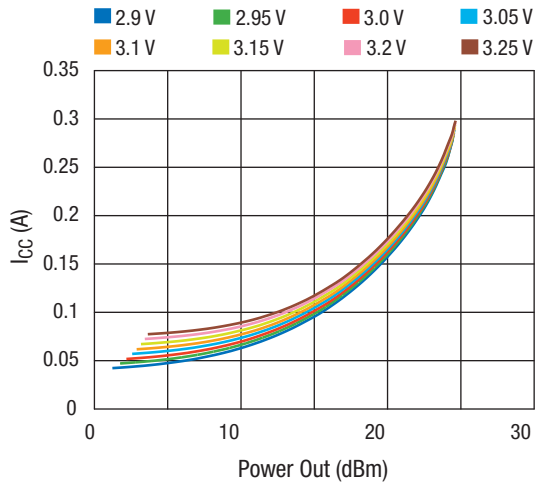


Figure 31. Icc vs Power Out Across VREG

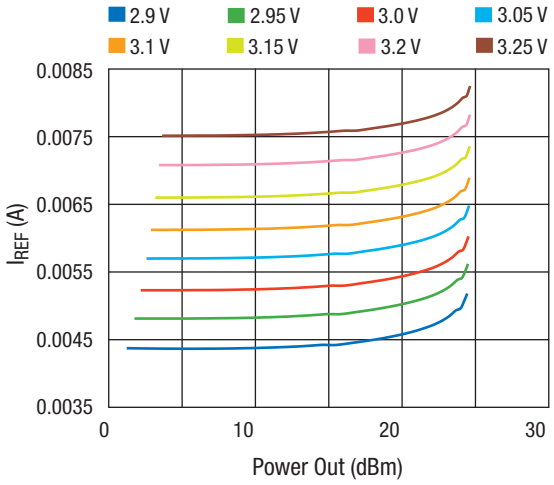


Figure 32. IREF vs Power Out Across VREG

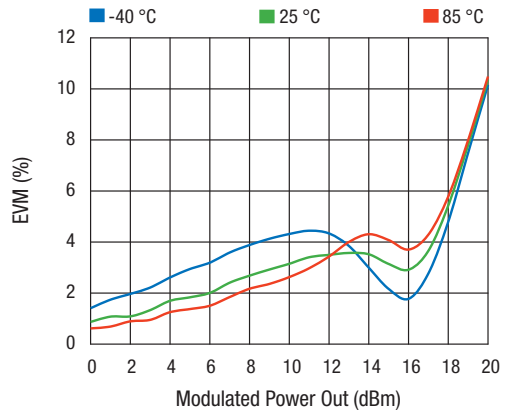


Figure 33. EVM vs Modulated Power Out Across Temperature 802.11g, 54 Mbps, 64 QAM

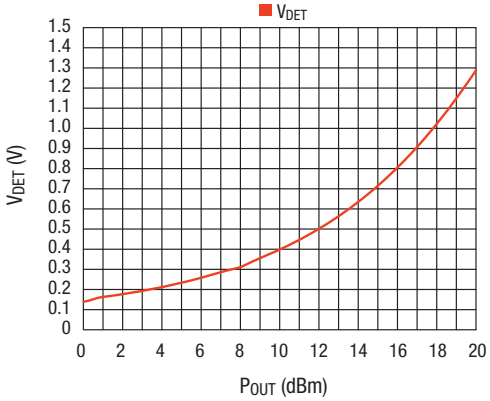


Figure 34. Detector Voltage vs Power Out 802.11g , 54 Mbps, 64 QAM

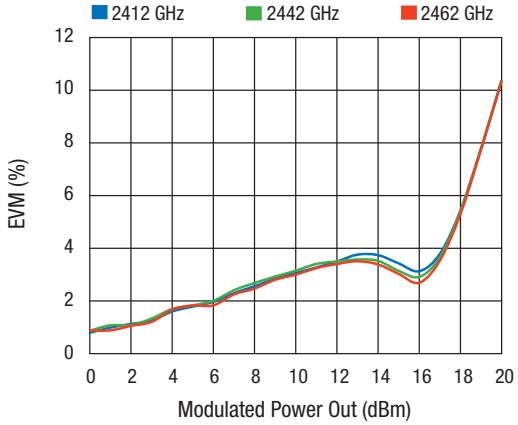


Figure 35. EVM vs Modulated Power Out Across Frequency 802.11g, 54 Mbps, 64 QAM

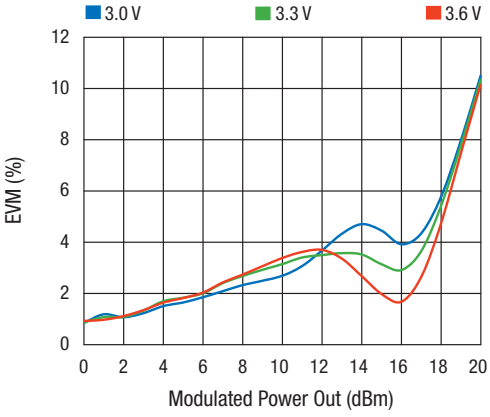


Figure 36. EVM vs Modulated Power Out Across Vcc 802.11g, 54 Mbps, 64 QAM

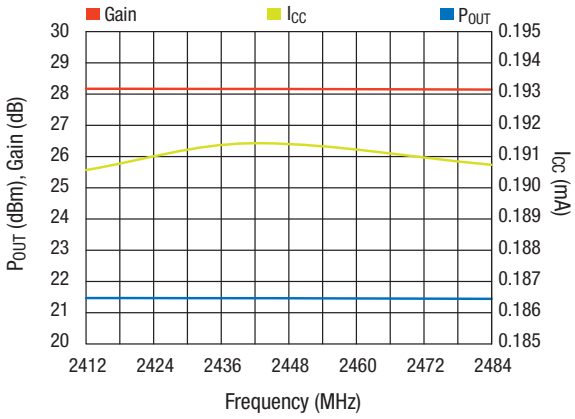
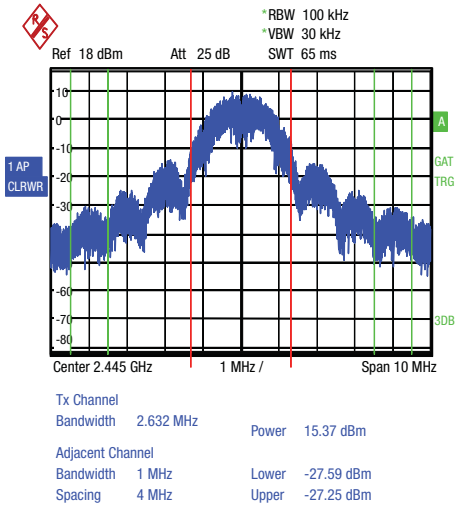


Figure 37. POUT, Gain, and Icc vs Frequency 802.11b, CCK, 11 Mbps



Channel Absolute Power Spectral Density at Mask Limit (absolute limit of -30 dBm with |f-fc| > 3.5 MHz with 100 MHz resolution bandwidth).

Figure 38. ZigBee® 802.15.4, Spectral Mask, O-QPSK, 250 Kb/s F = 2.445 GHz, Channel Power = 15.4 dBm

EVB Test Board Biasing Procedure

1. Connect the RF input and output ports as labeled on the engineering Evaluation Board.
2. Set the input power level from a CW signal generator to approximately -25 dBm.
3. Apply ground connection from DC voltage supply to all GND pins before applying any voltage.
4. Adjust the power supply to 3.3 V and set the current limit to 400 mA. Apply voltage to the pin labeled V_{CC} and note that there is no current draw from the supply. Be sure to apply the voltage to V_{CC} before applying any other voltages to the test board.
5. Adjust a second power supply output to 3.0 V and set the current limit to 30 mA. Apply voltage to the pin labeled V_{REG} and VDCC. Note that the current draw for V_{REG} is approximately 10 mA.
6. Observe that the current on the V_{CC} supply is in the range of the quiescent current specification. The SKY65006 should be approximately 50 mA.
7. Observe that the small signal gain is within the range specified. The SKY65006 should be in the range of 27 dB. This should verify the proper working conditions for this device, and further testing can proceed.
8. To observe the detector voltage output, connect a voltmeter or oscilloscope to the V_{DET} pin on the evaluation test board. Set the signal source to CW mode and increase power until the output voltage begins to increase. The nominal offset voltage with low or no signal inputs should be approximately 50 to 200 mV and should increase monotonically to approximately 700 to 1000 mV, when driven at an output level of approximately +18 dBm. The evaluation circuit contains an external 51 kΩ resistor and an equivalent capacitance of 10 pF to ground.
9. Bias the unit off by first removing the V_{REG} power supply and finally remove the connection to the V_{CC} power supply.

Application Information

The Skyworks SKY65006-348LF-11 is a high-performance 2-stage InGaP power amplifier designed for 2.4 to 2.5 GHz ISM, IEEE802.11b, 802.11g WLAN and ZigBee band applications. The SKY65006-348LF is a high-efficiency linear amplifier designed for single 3.3 V supply operation, requiring no input and output matching components for 50 Ω operation. This device also includes an internal power detector and integrated harmonic filter for reduced PC board component count. The integrated low pass filter is also highly effective in reducing harmonics at their source by localizing harmonic rejection to a tiny portion of the PA chip. This significantly reduces the risk of radiation from a high order filter design external to the amplifier. Filtering of harmonics in this way may eliminate the need for an external shield over the PA, and reduces overall cost. If additional suppression of harmonics is required, an external low pass filter can be added to the output of the amplifier. Optional shunt inductor, L3, is included on the applications board at the input of the amplifier to improve the return loss. The typical performance data shown includes these optional components.

The SKY65006-348LF requires a nominal V_{CC} supply voltage of 3.3 V and a positive control voltage $V_{REG}1,2$ providing bias for the first and second stage amplifiers. Nominal control voltage, V_{REG}, is 2.5 to 2.6 V resulting from the stack of two emitter-base junctions of about 1.3 V each for typical GaAs HBT device. To ensure proper reference currents into $V_{REG}1,2$, for normal operation of the RF stages, drop-in resistors could be used between $V_{REG}1,2$ and a V_{REG} supply. Bias control would then be set in the range of 2.7 to 3.5 V allowing added flexibility for both the control voltage value and desired RF stage currents. If additional output power is required, V_{CC} can also be increased 4.0 V. Biasing of each stage consists of an external resistor of 180 Ω (R_1) and 240 Ω (R_2) for the recommended typical bias currents of 15 mA and 35 mA for stage 1 and 2, respectively. In most applications, one end of each of the bias resistors is tied to the V_{REG} supply, so both amplifier stages are biased with a single common voltage. Capacitor C_5, 1.8 pF, bypasses the V_{REG} stage 1 control bias pin and is used to improve RF rejection of the bias control lines.

Although there is no need for external matching when operating in a 50 Ω system, an input and output 6 pF decoupling capacitor is shown on the evaluation circuit. This capacitor is only mandatory on the RF output side of the device. The RF input is DC isolated and could be connected to driver circuits directly without the need for additional blocking capacitors. Capacitors of 5.6 pF were chosen because their self-resonant frequency would not add any unwanted disturbances in the 50 Ω transmission line path.

The SKY65006-348LF is unconditionally stable at any frequency and voltage setting as long as it is grounded correctly. It is extremely important to pay special attention to the RF grounding pad under the device.

Ground pad vias and solder mask patterns are designed to ensure minimum parasitic inductance to the underlying ground and at each RF bypassing component. To ensure reliable soldering of the device paddle, it is highly recommended that filled vias with a minimal reliable diameter and filling the entire pattern be used. The filled-via technique would remove the possibility of solder migration down via holes, which can cause a large increase in inductance and possible instabilities.

Each amplifier stage is biased through a series choke and shunt capacitor combination which is completely integrated on chip to provide maximum RF isolation and harmonic radiation immunity. To avoid interferences from the low-frequency gain of the amplifier and to ensure stability at low out-of-band frequencies, the stage 1 amplifier is biased through inductor L_1. It is also shunted by a large value capacitance to ensure proper low-frequency bypassing of the amplifier. To avoid a shunting effect on the 50 Ω line, a high-impedance, self-resonating choke L_2 (in the range of 22 to 33 nH depending on vendor and size) and a large value bypass capacitor are used for biasing the output stage. Capacitor C_6, 4.7 µF, on the V_{CC} line should be placed as close as possible to the biasing network supplying stage 2 or the output stage of the amplifier. Applications with the DC bias being generated strictly from a battery as the voltage source may not require this capacitor, or as large a value as specified in the applications circuit. However, in that case, a smaller ceramic capacitor of at least 0.1 µF should be used and also placed as close as possible to the biasing network supplying stage 2.

Capacitor C_9 affects amplifier turn-on time. Reduce the value of C_9 to decrease turn-on time as long as bias stability is not compromised.

Note: Normal operation requires that V_{CC} including VBCC be applied before the application of the V_{REG} voltages biasing stage 1 and 2 bias currents. If V_{CC} and VBCC are not applied prior to the application of the V_{REG} biasing, voltage damage could occur from excessive base current draw through the collector junction of the bias transistor. The SKY65006-348LF also includes an on-board, compensated power detector providing a single-ended output voltage for measuring power over a wide dynamic range. The detector load and settling time constant are set external to the device. Nominal detector load is 51 kΩ and 5 pF, yielding a settling time of approximately 500 ns. Note that there is an internal 5 pF on-chip capacitance, so the net capacitance value is approximately 10 pF. Lower resistor values may be used if necessary with the net impact being a lower output detector voltage over its useful dynamic range. For proper detector operation, a reference voltage must be applied to the V_{DET} line. Any voltage between 2 and 4 V is acceptable for the reference voltage, but it is recommended to supply V_{DET} from the V_{REG} power supply. The benefit is that the approximate 2 mA of current that the reference circuit consumes will not be wasted with the PA in the "Off" state. There is also the option of not biasing the detector reference if the current consumption is of prime importance, but the detector will then act as a normal unbiased detector, and sensitivity and accuracy will be degraded.

The evaluation circuit board is constructed as a four-layer FR4 stack with an overall thickness of 0.062 inch (1.57 mm). Top layer dielectric is 0.01-inch thick with 50 Ω transmission line widths of 0.0195 inch. The printed circuit board is constructed using a symmetrical 0.01-inch stack on the top and bottom layers and with a 0.032-inch thick pre-preg core. All components are 0402 in size with the exception of the 4.7 µF and 10 µF tantalum capacitors. Please note the 10 µF capacitors are installed to provide low frequency filtering for lab testing. Actual values, if necessary, will be dependent upon layout and circuit environment. All ground vias used are 0.012 inch in diameter and placed as close to the ground ends of bypassing components as possible. Four vias are used under the device to create a low inductance path to ground. If a smaller diameter is to be used, or if the substrate thickness is greater than 0.01 inch, additional vias must be placed under the device to reduce the potential risk of parasitic oscillation.

Evaluation Board Description

The Skyworks SKY65006-348LF Evaluation Board is used to test the performance of the SKY65006-348LF PA . The Evaluation Board application schematic diagram is shown in Figure 39. The Evaluation Board Bill of Materials (BOM) is shown in Table 6.

An assembly drawing for the Evaluation Board is shown in Figure 40, and the layer detail is provided in Figure 41.

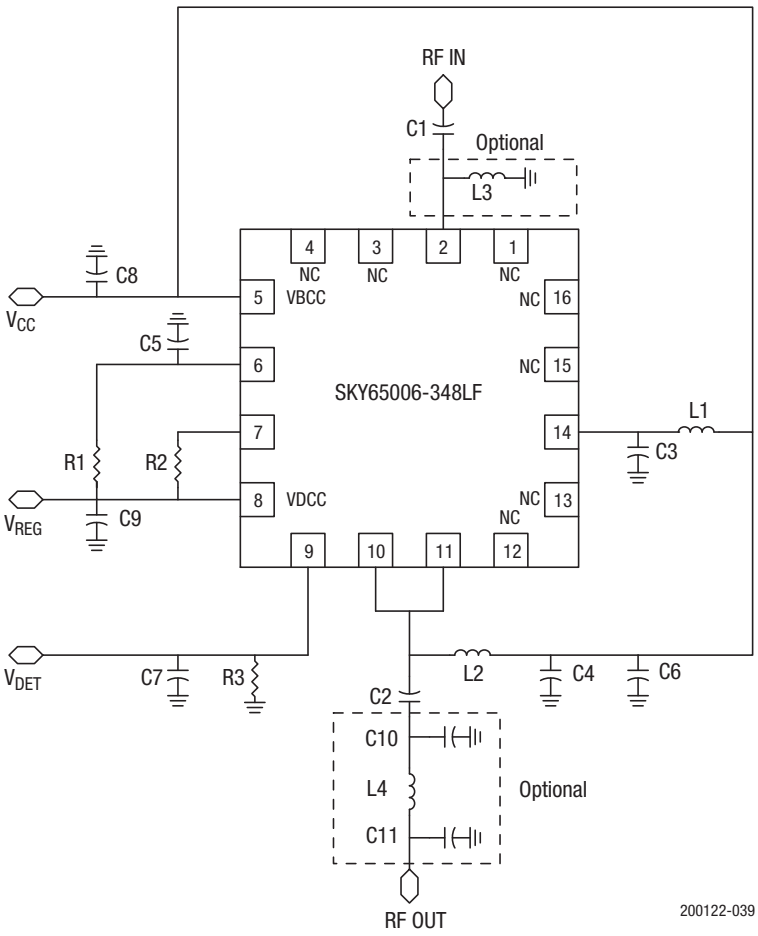


Figure 39. SKY65006-348LF Evaluation Board Application Schematic

Table 6. Evaluation Board Bill of Materials (BOM)

Component	Size	Value	Units	Manufacturer	Mfr Part Number
C_1	0402	5.6	pF	Murata	GRM1555C1H5R6CZ01E
C_2	0402	5.6	pF	Murata	GRM1555C1H5R6CZ01E
C_3	0402	10K	pF	Murata	GRM155R71E103KA01
C_4	0402	10K	pF	Murata	GRM155R71E103KA01
C_5	0402	1.8	pF	Murata	GRM1555C1H1R8CZ01D
C_6	0603	4.7	µF	Panasonic	ECST1AZ475R
C_7	0402	4.7	pF	Murata	GRM1555C1H4R7CZ01E
C_8	1206	10	µF	AVX	TAJA106M006R
C_9	1206	10	µF	AVX	TAJA106M006R
C_{10}	0402	1	pF	Murata	GRM1555C1H1R0CZ01E
C_{11}	0402	1	pF	Murata	GRM1555C1H1R0CZ01E
L_1	0402	22	nH	TDK	MLK1005S22NJT000
L_2	0402	22	nH	TDK	MLK1005S22NJT000
L_3	0402	2.2	nH	TDK	MLK1005S2N2ST000
L_4	0402	2.2	nH	TDK	MLK1005S2N2ST000
R_1	0402	180	Ω	Panasonic	ERJ2GEJ181X
R_2	0402	240	Ω	Panasonic	ERJ2GEJ241X
R_3	0402	51	kΩ	Panasonic	ERJ2GEJ513X
PCB				Metro circuits	EN18-D730

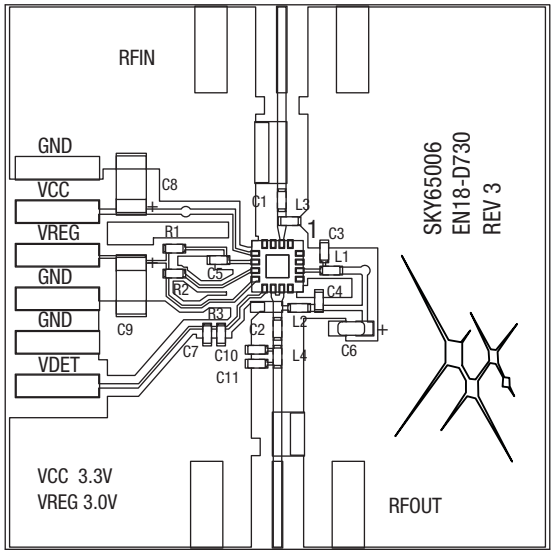
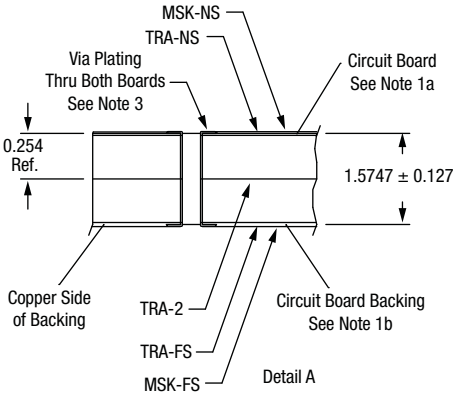


Figure 40. SKY65006-348LF Evaluation Board Assembly Drawing



Notes:
Units = mm.
1. Material:
1a. Circuit board: FR4, 0.254 mm thick, 1 oz finished copper TRA-NS layer, 1/2 oz finished copper TRA-2 layer.
1b. Circuit board backing: FR4 prepreg, 1 oz copper one side.
1c. Laminate the unmetalized side of backing to bottom of circuit board for a total thickness of 1.5747 ± 0.127 mm. (See Detail A)
2. Plating: 200 microinches of nickel, and 50–100 microinches of soft gold.
3. Via plating: Cu plate 0.001 to 0.0015 thru both boards.
4. RF lines marked with * to be finished width of 0.50 mm measured at bottom of trace (trace to board interface).
All line width tolerances ± 0.025 mm.
All rubout tolerances ± 0.025 mm.
5. Silk-screen reference designators approximately as shown.
6. Separate boards with router.

200122-041

Figure 41. Evaluation Board Layer Detail

Package Dimensions

The PCB layout footprint for the SKY65006-348LF is shown in Figure 42. Typical part markings are shown in Figure 43. Package dimensions are shown in Figure 44.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY65006-348LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

Tape and Reel Information

Refer to the *Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation* Application Note.

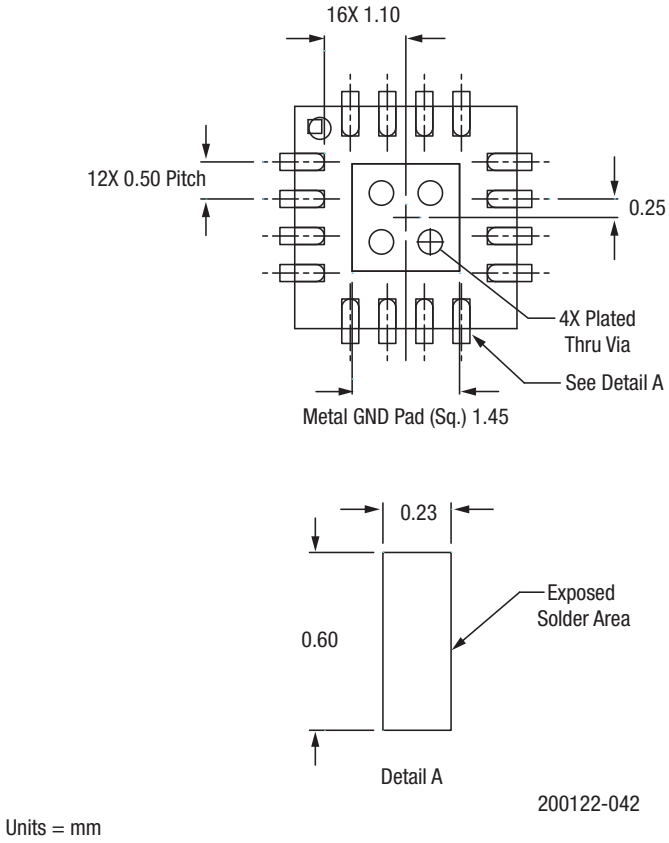


Figure 42. SKY65006-348LF Board Layout Footprint

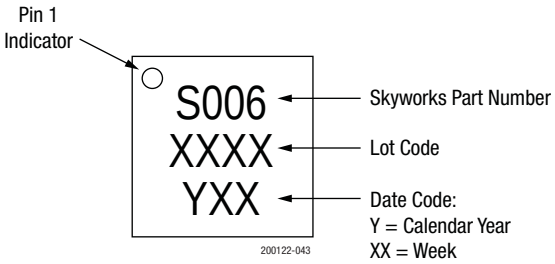


Figure 43. Typical Package Marking

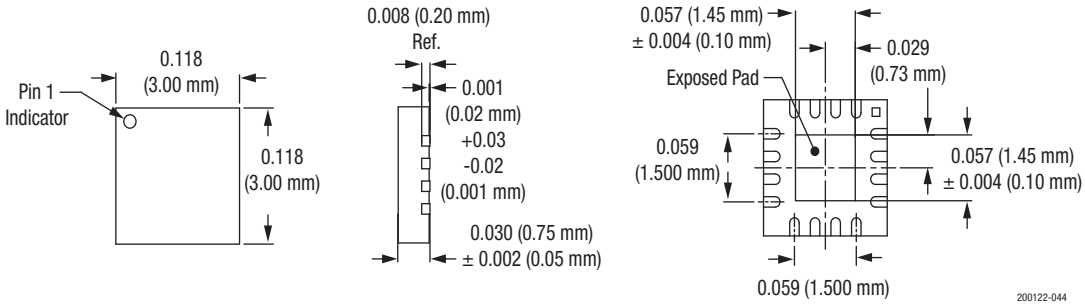


Figure 44. SKY65006-348LF Package Dimensions