DATA SHEET

SKY66313-11: 3400 to 3600 MHz Wide Instantaneous Bandwidth High-Efficiency Power Amplifier

Applications

- FDD and TDD 4G LTE and 5G systems
- Supports 3GPP Bands n78, B22, and B42
- Driver amplifier for micro-base and macro-base stations
- Enterprise small cell and massive MIMO

Features

- Wide instantaneous signal bandwidth: 100 MHz
- High-efficiency: PAE = 15% @ +23 dBm
- High linearity: +23 dBm with < -50 dBc ACLR with pre-distortion (5x20 MHz LTE, 8.5 dB PAR signal)
- High gain: 37 dB
- Excellent input and output return loss: to 50 Ω system
- Integrated active bias: performance compensated over temp
- Integrated enable On/Off function: PAEN = 1.5 to 2.5 V
- Single supply voltage: 5.0 V
- Pin-to-pin compatible PA family supporting major 3GPP bands
- Compact (16-pin, 5 × 5 × 1.3 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

Description

The SKY66313-11 is a highly efficient, wide instantaneous bandwidth, fully input/output matched power amplifier (PA) with high gain and linearity. The compact 5 × 5 mm PA is designed for FDD and TDD 4G LTE and 5G systems operating from 3400 to 3600 MHz. The active biasing circuitry is integrated to compensate PA performance over temperature, voltage, and process variation.

The SKY66313-11 is part of a high-efficiency, pin-to-pin compatible PA family supporting major 3GPP bands.

A block diagram of the SKY66313-11 is shown in Figure 1. The device package and pinout for the 16-pin device are shown in Figure 2. Table 1 lists the pin-to-pin compatible parts in the PA family. Signal pin assignments and functional pin descriptions are described in Table 2.

Table 1. Pin-to-Pin Compatible PA Family

Part Number	Frequency (MHz)	3GPP Band
SKY66312-11	2300 to 2400	Bands 30 and 40
SKY66317-11	2490 to 2700	Bands 7, 38, and 41
SKY66313-11	3400 to 3600	Band n78
SKY66315-11	4400 to 5000	Band n79

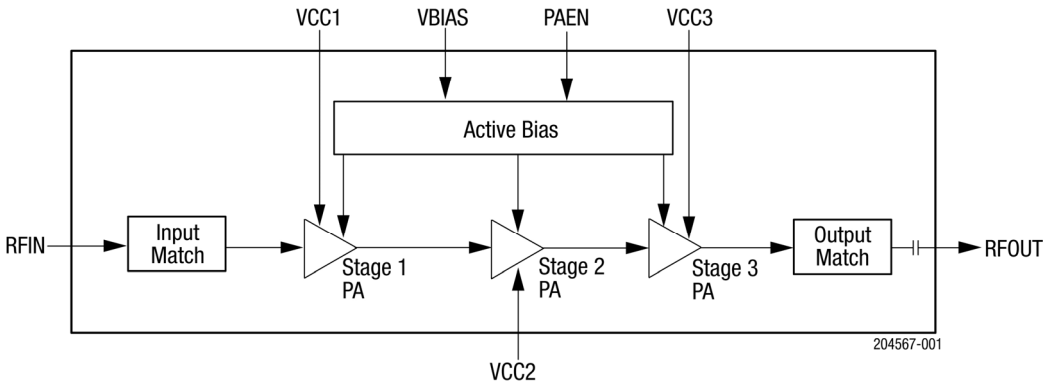


Figure 1. SKY66313-11 Block Diagram

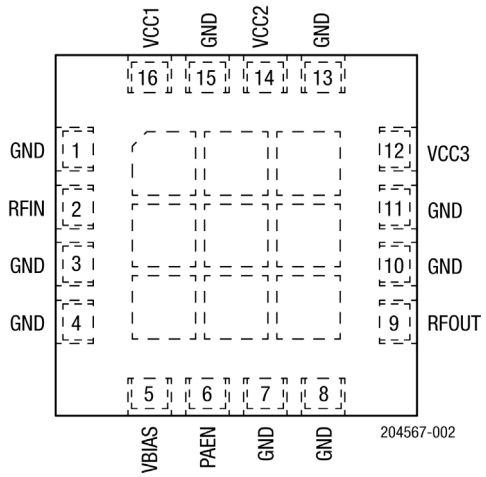


Figure 2. SKY66313-11 Pinout
(Top View)

Table 2. SKY66313-11 Signal Descriptions[1]

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	RFOUT	RF output port
2	RFIN	RF input port	10	GND	Ground
3	GND	Ground	11	GND	Ground
4	GND	Ground	12	VCC3	Stage 3 collector voltage
5	VBIAS	Bias voltage	13	GND	Ground
6	PAEN	PA enable	14	VCC2	Stage 2 collector voltage
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	VCC1	Stage 1 collector voltage

[1] The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

Technical Description

The matching circuits are contained within the device. An on-chip active bias circuit is included within the device for both input and output stages, which provides excellent gain tracking over temperature and voltage variations.

The SKY66313-11 is internally matched for maximum output power and efficiency. The input and output stages are independently supplied using the VCC1, VCC2, and VCC3 supply lines (pins 16, 14, and 12, respectively). The DC control voltage that sets the bias is supplied by the VCBIAS signal (pin 5).

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY66313-11 are provided in Table 3. Recommended operating conditions are specified in Table 4, and electrical specifications are provided in Table 5.

Typical performance characteristics are shown in Figures 3 through 33.

Table 3. SKY66313-11 Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Maximum	Units
RF input power (CW)	P_{IN}		+10	dBm
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V_{CC}		5.5	V
PA enable	V_{EN}		2.8	V
Operating temperature	T_C	-40	+110	°C
Storage temperature	T_{ST}	-55	+125	°C
Junction temperature	T_J		+150	°C
Power dissipation (T_{CASE} = 100 °C):				
P_{OUT} = +23 dBm	P_{DISS_23dBm}		1.3	W
P_{OUT} = +27 dBm	P_{DISS_27dBm}		2.0	W
Device thermal resistance (T_{CASE} = 100 °C):				
P_{OUT} = +23 dBm	$R_{TH23dBm}$		16.5	°C/W
P_{OUT} = +27 dBm	$R_{TH27dBm}$		14.5	°C/W

1 Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***ESD HANDLING**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 4. SKY66313-11 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V_{CC1}, V_{CC2}, V_{CC3}, V_{BIAS}	4.75	5	5.25	V
PA enable:	PAEN				
ON		1.5	2.0	2.5	V
OFF			0	0.5	V
PA enable current	I_{ENABLE}		1	12	µA
Operating frequency	f	3400		3600	MHz
Operating temperature	T_C	-40	+25	+110	°C

Table 5. SKY66313-11 Electrical Specifications[1]
(V_{CC1} = V_{CC2} = V_{CC3} = V_{BIAS} = 5 V, PAEN = 2.0 V, f = 3500 MHz, T_C = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	f		3400		3600	MHz
Small signal gain	|S21|	P_{IN} = -30 dBm	36			dB
Gain @ +23 dBm	|S21|@+23dBm	P_{OUT} = +23 dBm	34.5	37		dB
Input return loss	|S11|	P_{IN} = -20 dBm	10	14		dB
Output return loss	|S22|	P_{IN} = -20 dBm	11	16		dB
Reverse isolation[2]	|S12|	P_{IN} = -30 dBm		50		dB
ACLR @ +23 dBm	ACLR	P_{OUT} = +23 dBm (5x20 MHz LTE, 8.5 dB PAR signal)		-30	-28	dBc
Output power at 1dB gain compression[2]	P1dB	CW, reference to small signal gain (P_{IN} = -30 dBm)		+33		dBm
Output power at 3 dB gain compression[2]	P3dB	CW, reference to small signal gain (P_{IN} = -30 dBm)	+33	+34.5		dBm
2nd harmonic	2fo	CW, P_{OUT} = +23 dBm		-31	-24	dBc
3rd harmonic[2]	3fo	CW, P_{OUT} = +23 dBm		-65		dBc
Power-added efficiency	PAE	CW, P_{OUT} = +23 dBm	12.5	15		%
Quiescent current	I_{CCQ}	No RF signal		115	135	mA
Turn-on time[3]	t_{ON}			<1		uS

1 Performance is guaranteed only under the conditions listed in this table.

2 Not tested in production. Verified by design.

3 RF turn-on time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power achieves 90% of the average steady-state “on” level.

RF turn-off time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power decreases to 10% of the average steady-state “on” level.

Typical Performance Characteristics

(Vcc1 = Vcc2 = Vcc3 = VBIAS = 5 V, PAEN = 2.0 V, f = 3500 MHz, Tc = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted)

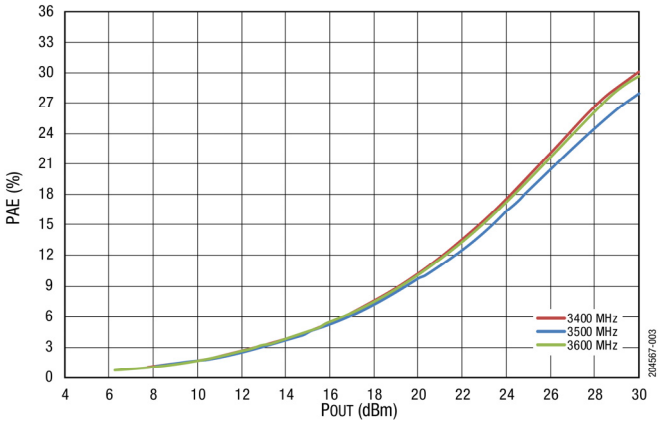


Figure 3. PAE vs Output Power (CW) Across Frequency

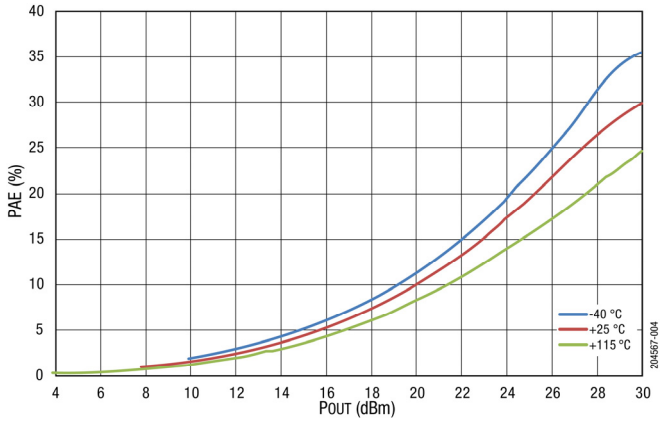


Figure 4. PAE vs Output Power Across Temperature

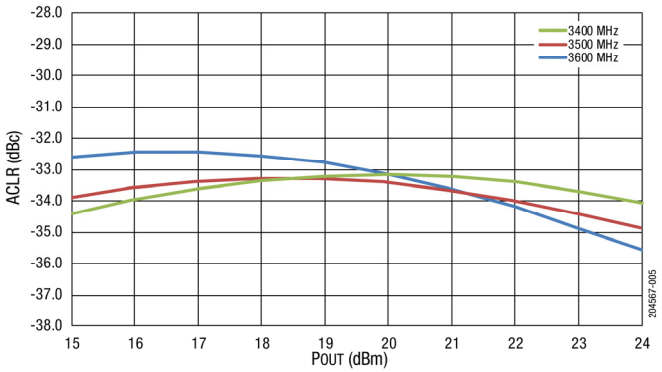


Figure 5. ACLR-1C vs POUT Across Frequency @ 5 V 25 °C

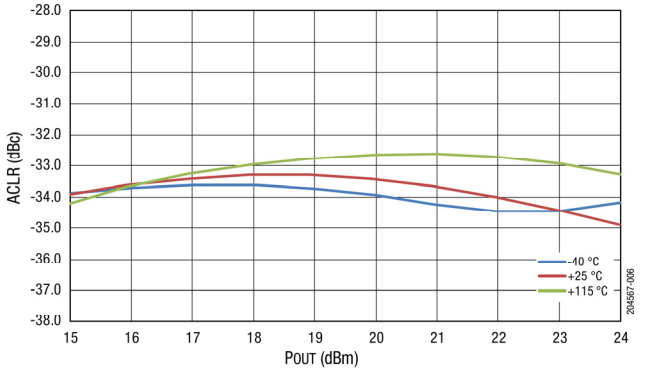


Figure 6. ACLR-1C vs POUT Across Temperature @ 3500 MHz, 5 V

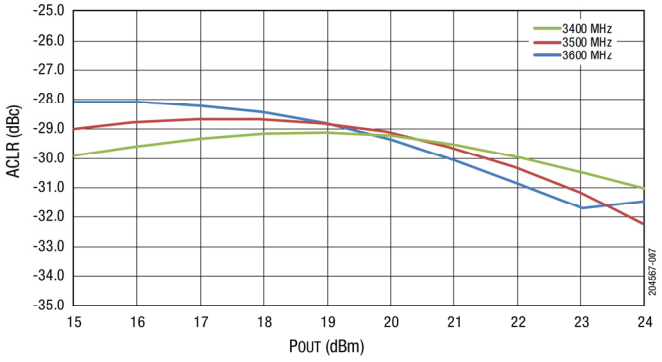


Figure 7. ACLR-5C vs POUT Across Frequency @ 5 V 25 °C

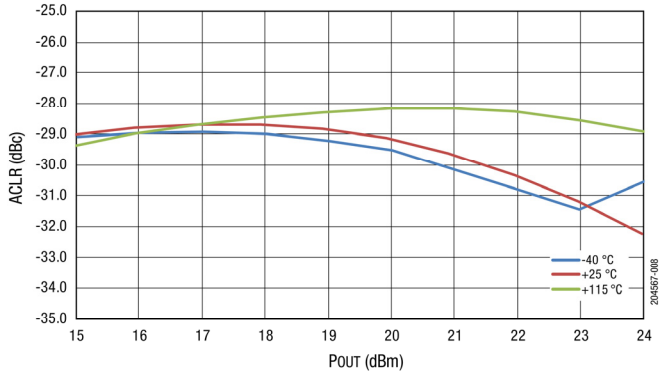


Figure 8. ACLR-5C vs POUT Across Temperature @ 3500 MHz, 5 V

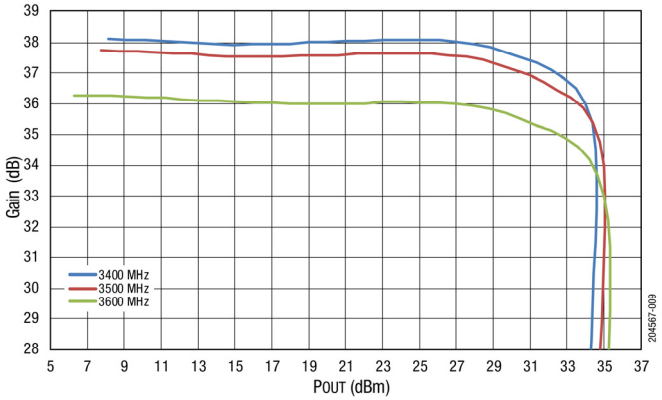


Figure 9. Gain vs POUT Across Frequency @ 5 V 25 °C

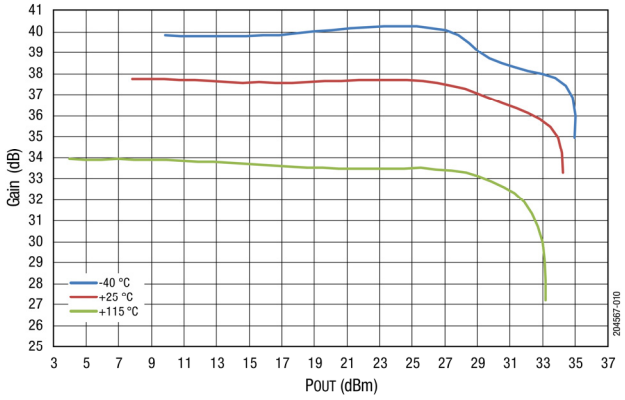


Figure 10. Gain vs POUT Across Temperature @ 3500 MHz, 5 V

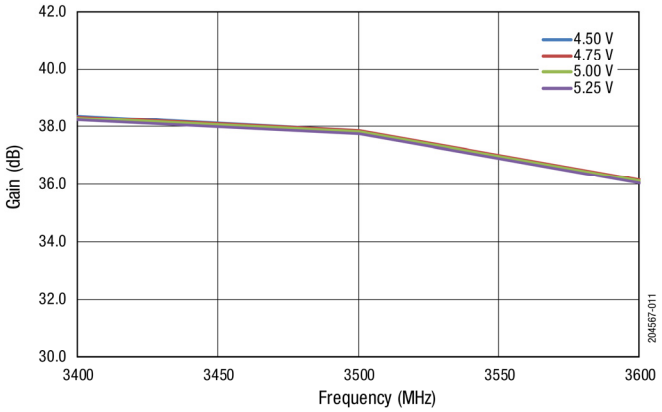


Figure 11. Gain @ +23 dBm vs Frequency Across VCC

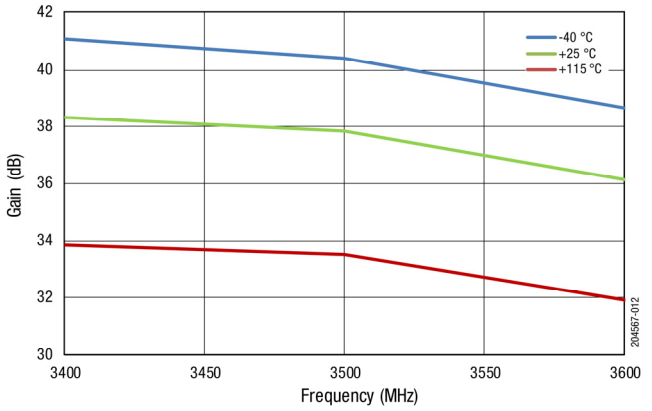


Figure 12. Gain @ +23 dBm vs Frequency Across Temperature

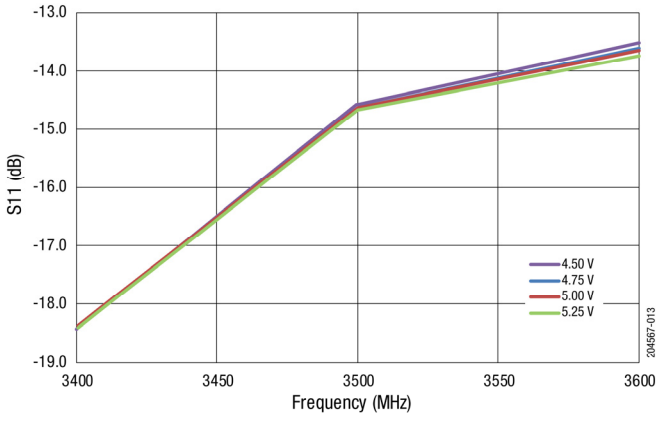


Figure 13. S11 vs Frequency Across VCC

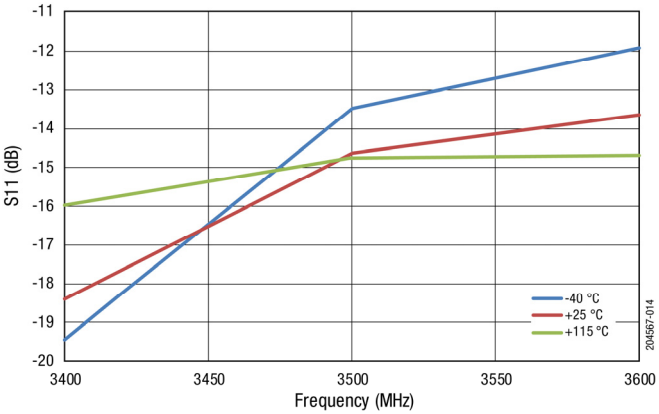


Figure 14. S11 vs Frequency Across Temperature

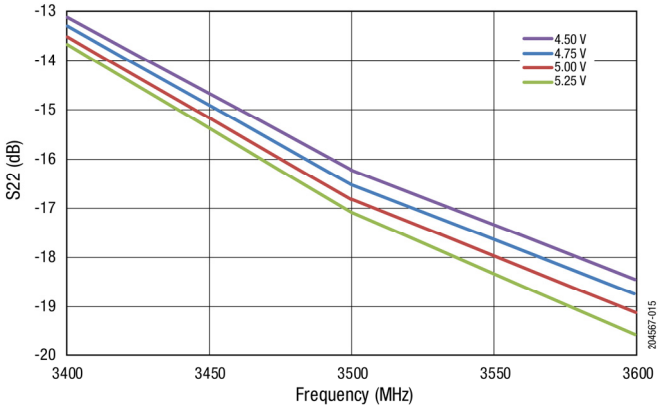


Figure 15. S22 vs Frequency Across Vcc

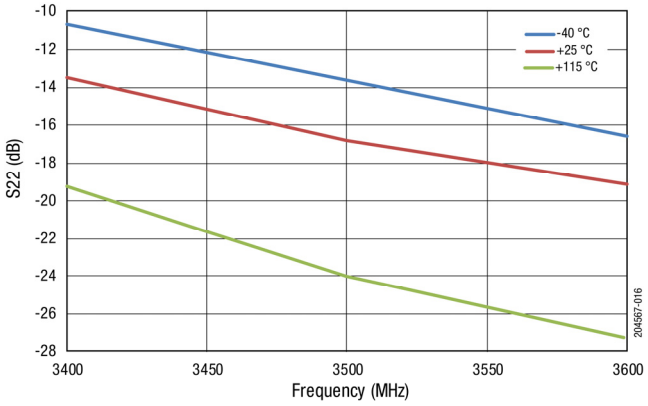


Figure 16. S22 vs Frequency Across Temperature

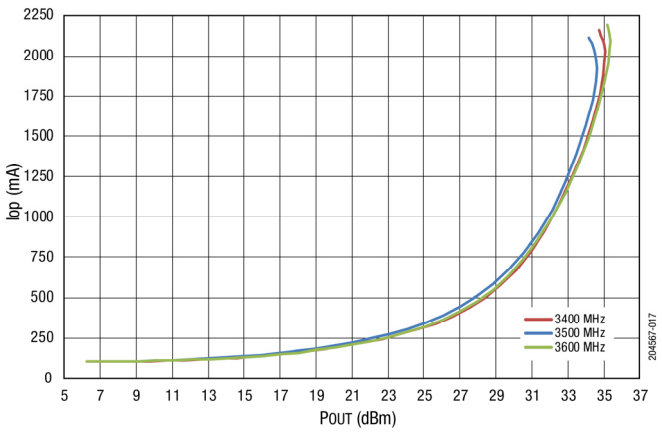


Figure 17. Iop vs POUT Across Frequency @ 5 V, 25 °C

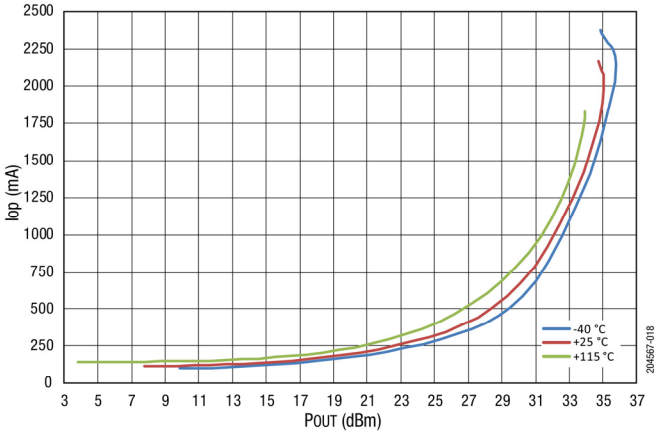


Figure 18. Iop vs POUT Across Temperature @ 3500 MHz, 5V

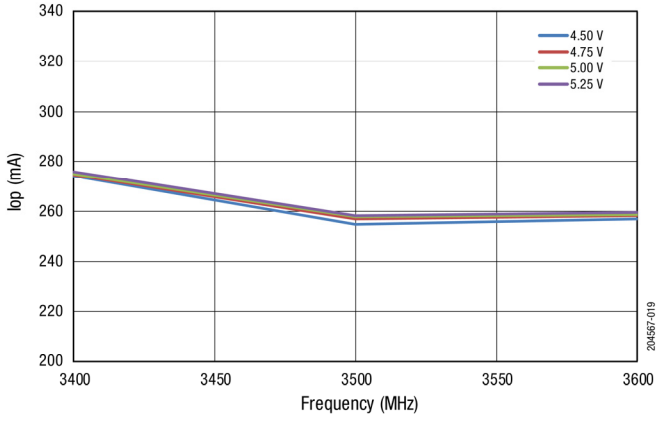


Figure 19. Iop @ +23 dBm vs Frequency Across Vcc

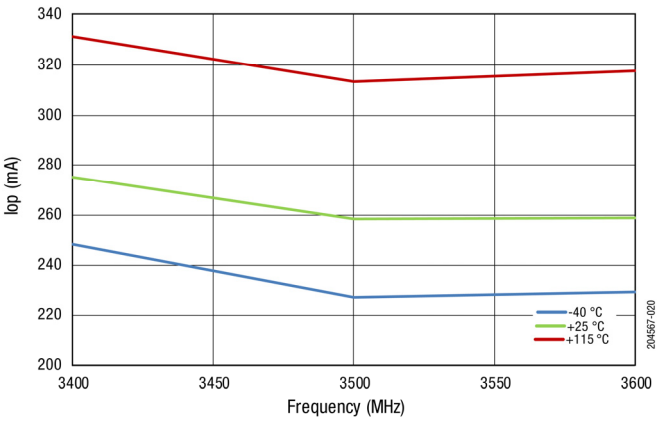


Figure 20. Iop @ +23 dBm vs Frequency Across Temperature

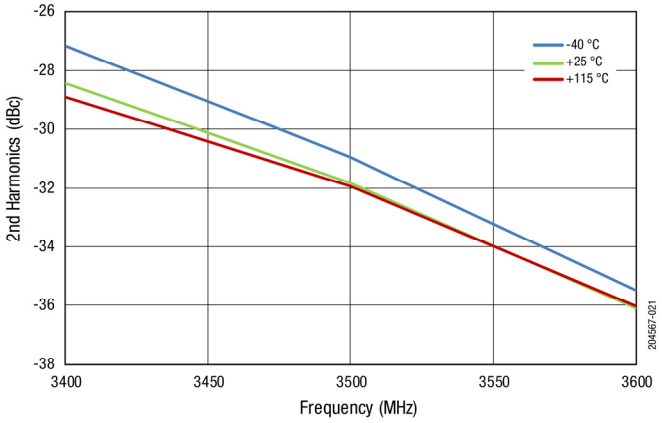


Figure 21. 2nd Harmonics @+23 dBm vs Frequency Across Temperature

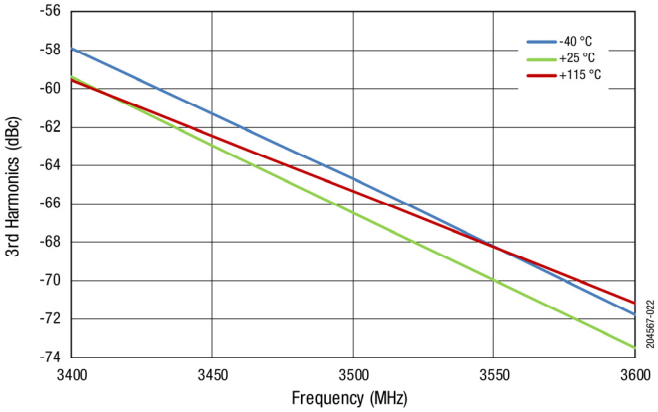


Figure 22. 3rd Harmonics @+23 dBm vs Frequency Across Temperature

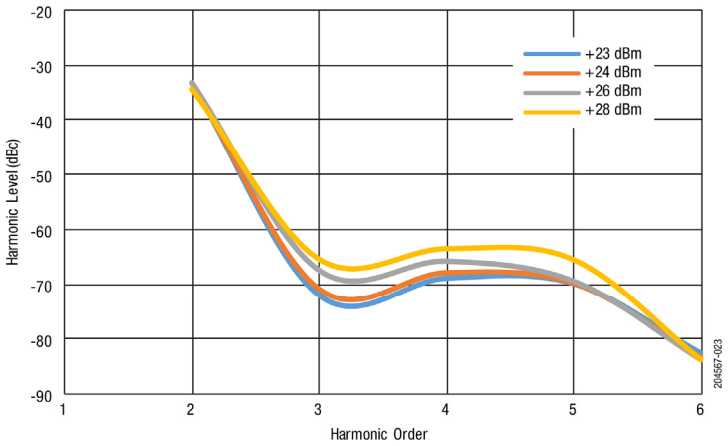


Figure 23. Harmonics Level vs Harmonic Order over Output Power (CW)

Table 6. SKY66313-11 Electrical Specifications[1]
(VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 3600 to 3800 MHz, TC = +25C, Input/Output Load = 50 Ω, Unless Otherwise Noted)

Parameter	Test Condition	Min	Typ	Max	Units
S21	P_{IN} = -30 dBm	34.5	36.0		dB
Gain @ 23dBm	P_{OUT} = +23 dBm	34.5	36.0		dB
S11	P_{IN} = -20 dBm		-15.0	-10.0	dB
S22	P_{IN} = -20 dBm		-15.0	-12.0	dB
S12	P_{IN} = -20 dBm		-50.0		dB
ACLR @ 23dBm (100 MHz)	5x20MHz LTE; 8.5 dB PAR		-29.0	-27.0	dBc
OP1dB	CW, Referenced to S21	32.0	33.0		dBm
OP3dB	CW, Referenced to S21	34.0	34.7		dBm
2Fo	CW, P_{OUT} = +23 dBm		-35.8	-33.0	dBc
3Fo	CW, P_{OUT} = +23 dBm		-80.4	-60.0	dBc
PAE @ 23dBm	CW, P_{OUT} = +23 dBm	13.0	14.0		%

[1] Verified by characterization

Typical Performance Specifications
(Vcc1 = Vcc2 = Vcc3 = VBIAS = 5 V, PAEN = 2.0 V, f = 3600 MHz to 3800 MHz, Tc = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted

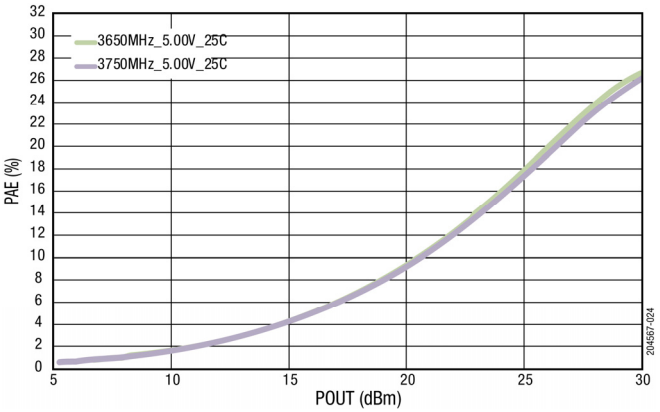


Figure 24. PAE vs Output Power (CW) over Frequency

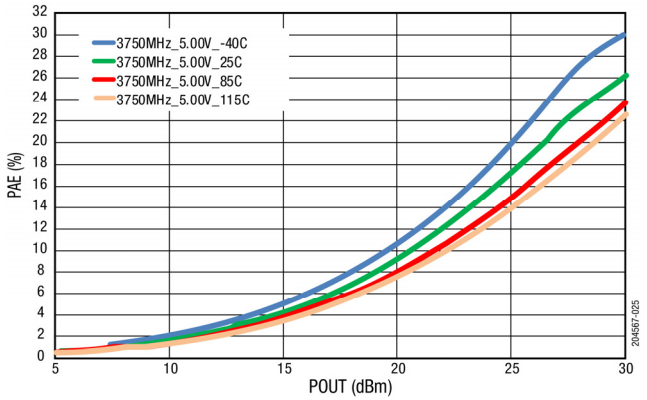


Figure 25. PAE vs POUT @ B43 (CW)

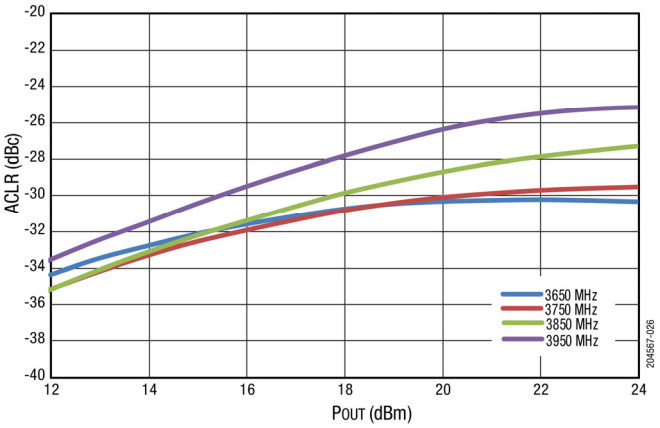


Figure 26. ACLR vs Output Power (CW) over Frequency (5x20 MHz LTE)

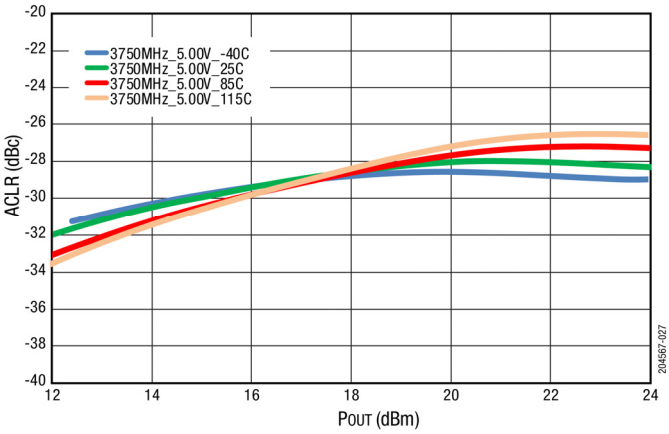


Figure 27. ACLR vs POUT @ B43 (100 MHz LTE, PAR = 8.5 dB)

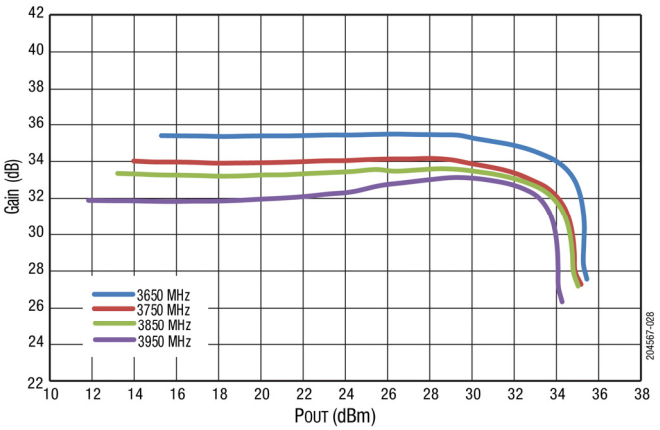


Figure 28. Gain vs Output Power (CW) over Frequency

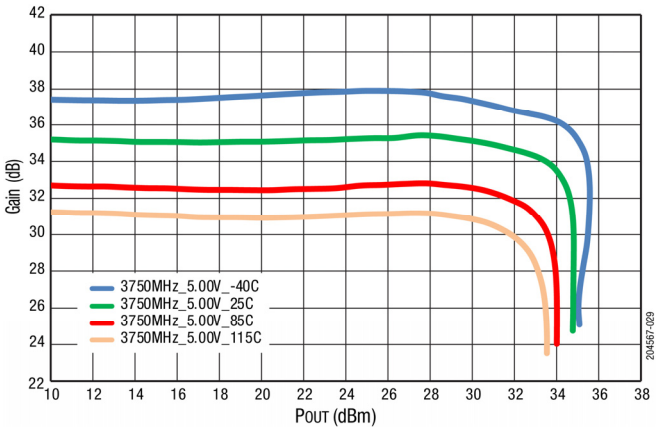


Figure 29. Gain vs Output Power (CW) over Temperature

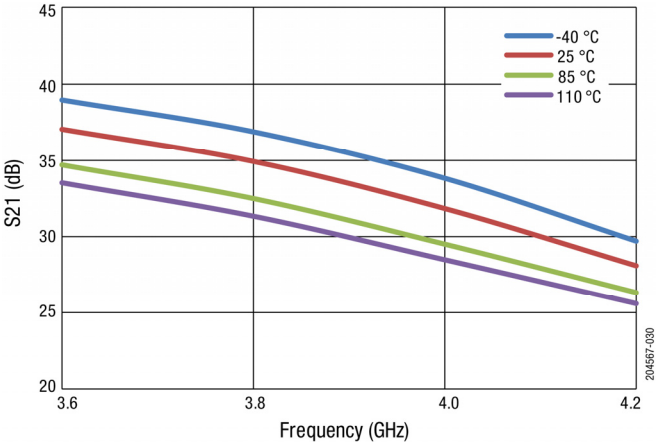


Figure 30. Small Signal Gain vs Frequency over Temperature

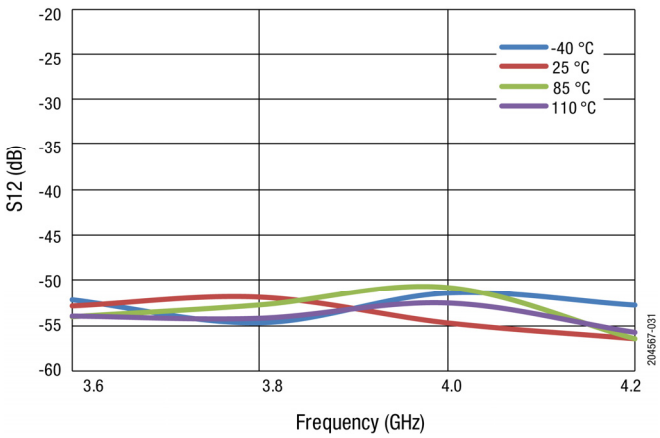


Figure 31. Reverse Isolation vs Frequency over Temperature

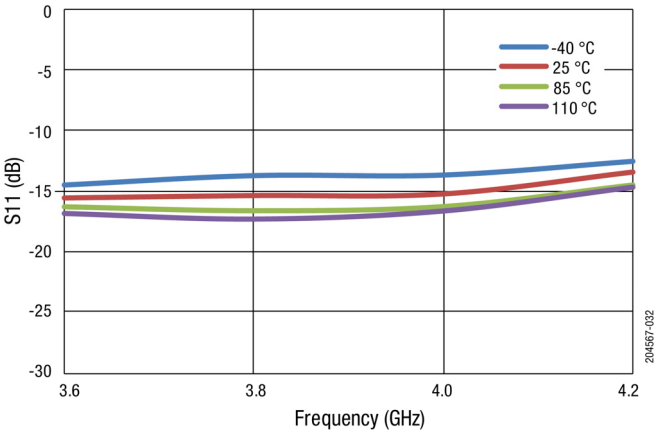


Figure 32. Input Return Loss vs Frequency over Temperature

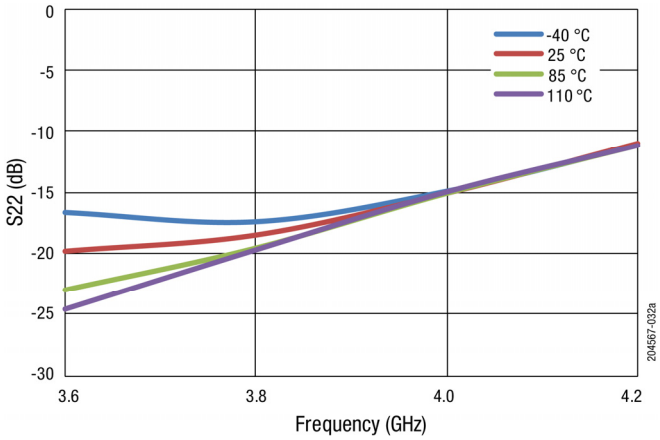


Figure 33. Output Return Loss vs Frequency over Temperature

Evaluation Board Description

The SKY66313-11 Evaluation Board is used to test the performance of the SKY66313-11 PA. An application schematic is provided in Figure 34. Table 7 provides the Bill of Materials (BOM) list for Evaluation Board components.

An assembly drawing for the Evaluation Board is shown in Figure 35. Board layer details are shown in Figure 36. Layer detail physical characteristics are noted in Figure 37.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SKY66313-11 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Because the circuit board acts as the heat sink, it must shunt as much heat as possible from the device.

  Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

NOTE: *A poor connection between the ground pad and ground increases junction temperature (T_J), which reduces the life of the device.*

Evaluation Board Test Procedure

Turn-On Sequence

1. Connect 50 Ω Test Equipment or Load to the input and output RF ports of the Evaluation Board.
2. Connect the DC ground.
3. Connect all VCCs and VBIAS lines to a +5 V supply. Connect PAEN to a 2.0 V supply.
4. Without applying RF, turn on the 5 V supply, then turn on the 2 V PAEN.
5. Apply RF signal data at -30 dBm and observe that the gain of the device is approximately 36 dB. Begin measurements.

Turn-Off Sequence

1. Turn off the RF input to the device.
2. Turn off PAEN (set to 0 V).
3. Turn off all VCCs and VBIAS.

NOTE: *It is important to adjust the VCC voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.*

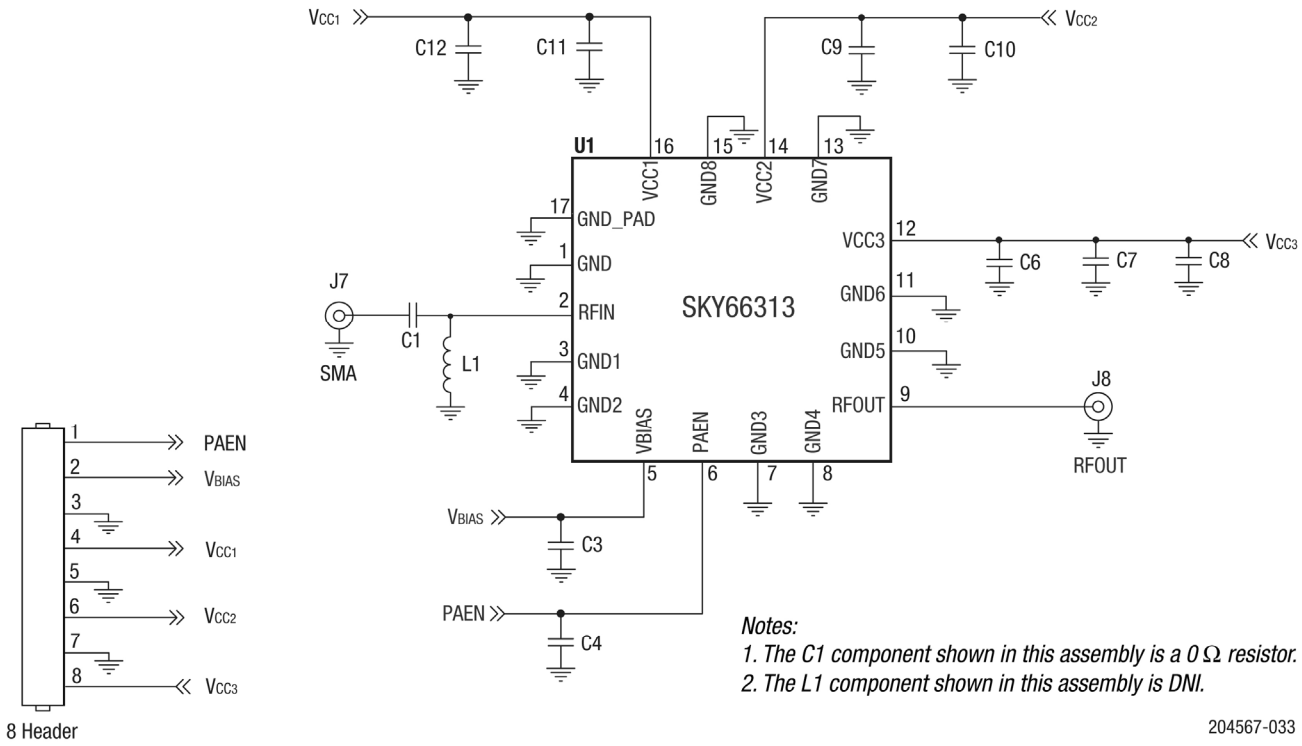
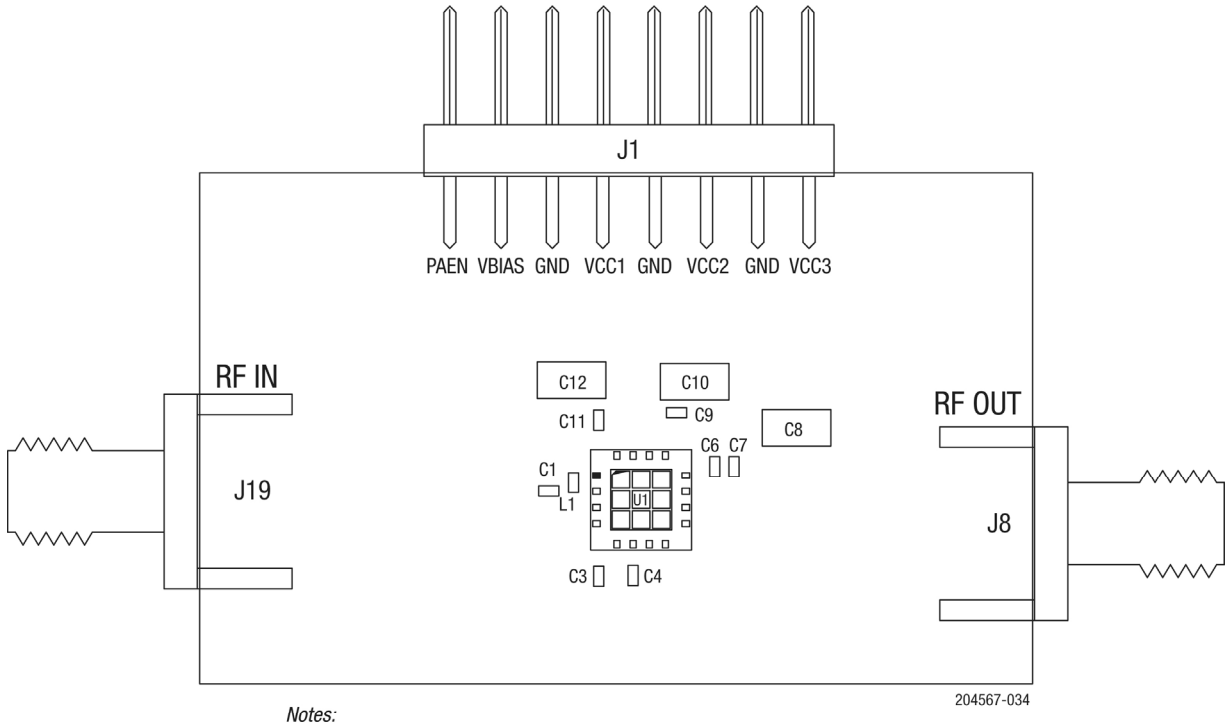


Figure 34. SKY66313-11 Application Schematic

Table. 7. SKY66313-11 Evaluation Board Bill of Materials (BOM)

Component	Description	Size
C1	Resistor, 0 Ω, 0.063 W	0402
C3, C6	Ceramic capacitor, 1 uF, ±10%, 16 V	0402
C4, C7	Ceramic capacitor, 3300 pF, X7R, ±10%, 50 V	0402
C8, C10, C12	Ceramic capacitor, 10 uF, X7R, ±10%, 16 V	1206
C9	Ceramic capacitor, 0.47 uF	0402
C11	Ceramic capacitor, 0.1 uF	0402
L1	DNI	
TW21-D690-XXXX	Evaluation Board	



Notes:

1. *Evaluation Board Gerber files are available on request.*
2. *The C1 component shown in this assembly is a 0 Ω resistor.*
3. *The L1 component shown in this assembly is DNI.*

Figure 35. Evaluation Board Assembly Drawing

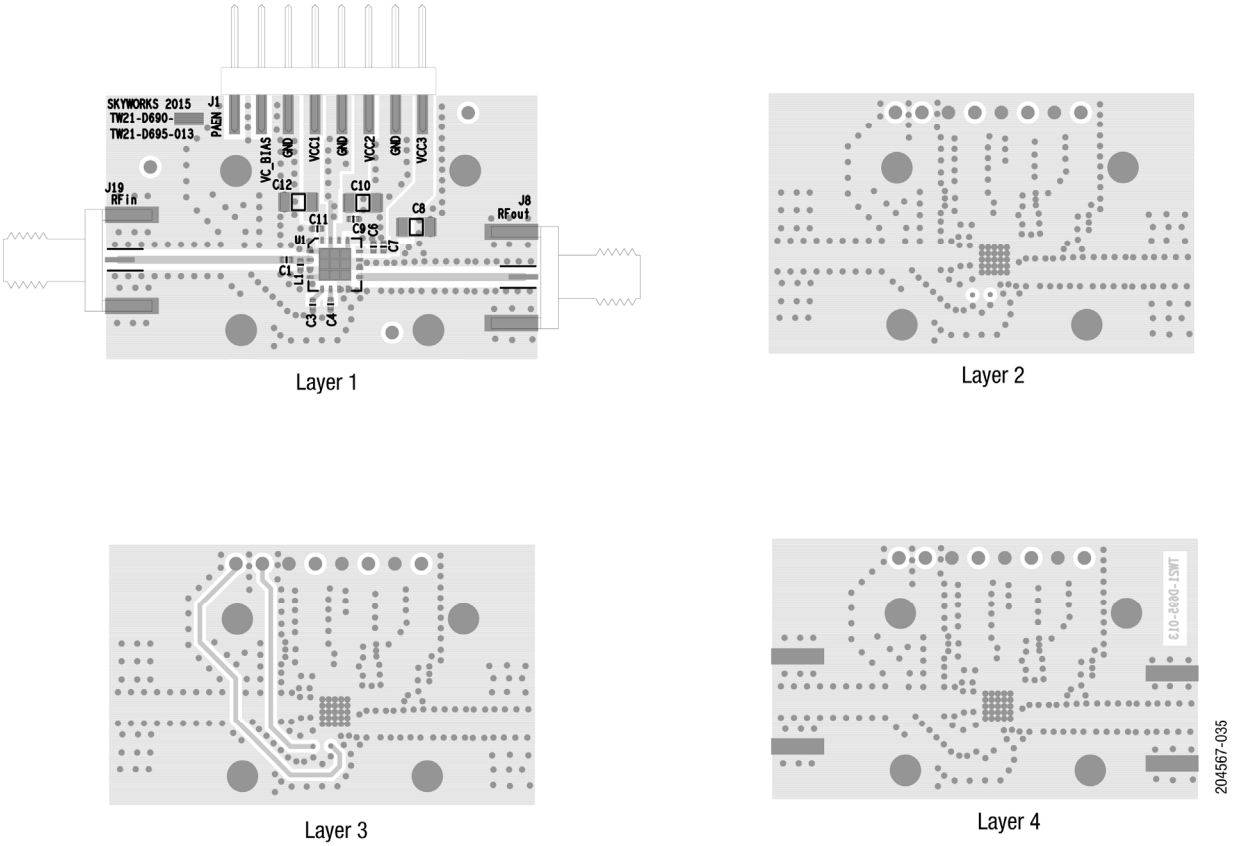


Figure 36. Board Layer Detail

50 Ohm	Cross Section	Name	Thickness (mm)	Materials
W = 0.500 mm		TMask	0.010	Solder Resist
		L1	0.035	Cu, 1 oz.
		Dielectric	0.250	R04350
		L2	0.035	Cu, 1 oz.
		Dielectric	0.350	FR4
		L3	0.035	Cu, 1 oz.
		Dielectric	0.250	FR4
		L4	0.035	Cu, 1 oz.
		BMask	0.010	Solder Resist

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Figure 37. Layer Detail Physical Characteristics

Application Circuit Notes

Center Ground. It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

GND (**pins 1**, **3**, **4**, **7**, **8**, **10**, **11**, **13**, and **15**). Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

VCBIAS (**pin 5**). The bias supply voltage for each stage, nominally set to +5 V.

RFOUT (**pin 9**). Amplifier RF output pin ($Z_0 = 50\ \Omega$). The module includes an internal DC blocking capacitor. All impedance matching is provided internal to the module.

VCC1, **VCC2**, and **VCC3** (**pin 16**, **15**, and **12**, respectively). Supply voltage for each stage collector bias is nominally set to 5 V. The evaluation board has inductors L1 and L2. These are place holders, and should be populated with 0 Ω resistors. Bypass and decoupling capacitors C6 through C12 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.

RFIN (**pin 2**). Amplifier RF input pin ($Z_0 = 50\ \Omega$). All impedance matching is provided internal to the module.

Package Dimensions

Typical part marking for the device is shown in Figure 38. The PCB layout footprint for the SKY66313-11 is shown in Figure 39. Package dimensions are shown in Figure 40, and tape and reel dimensions are provided in Figure 41.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY66313-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

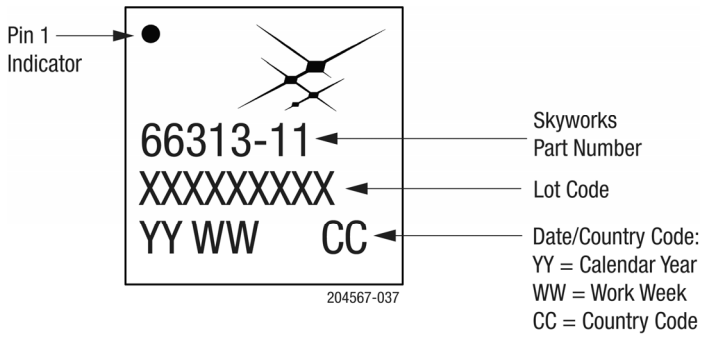
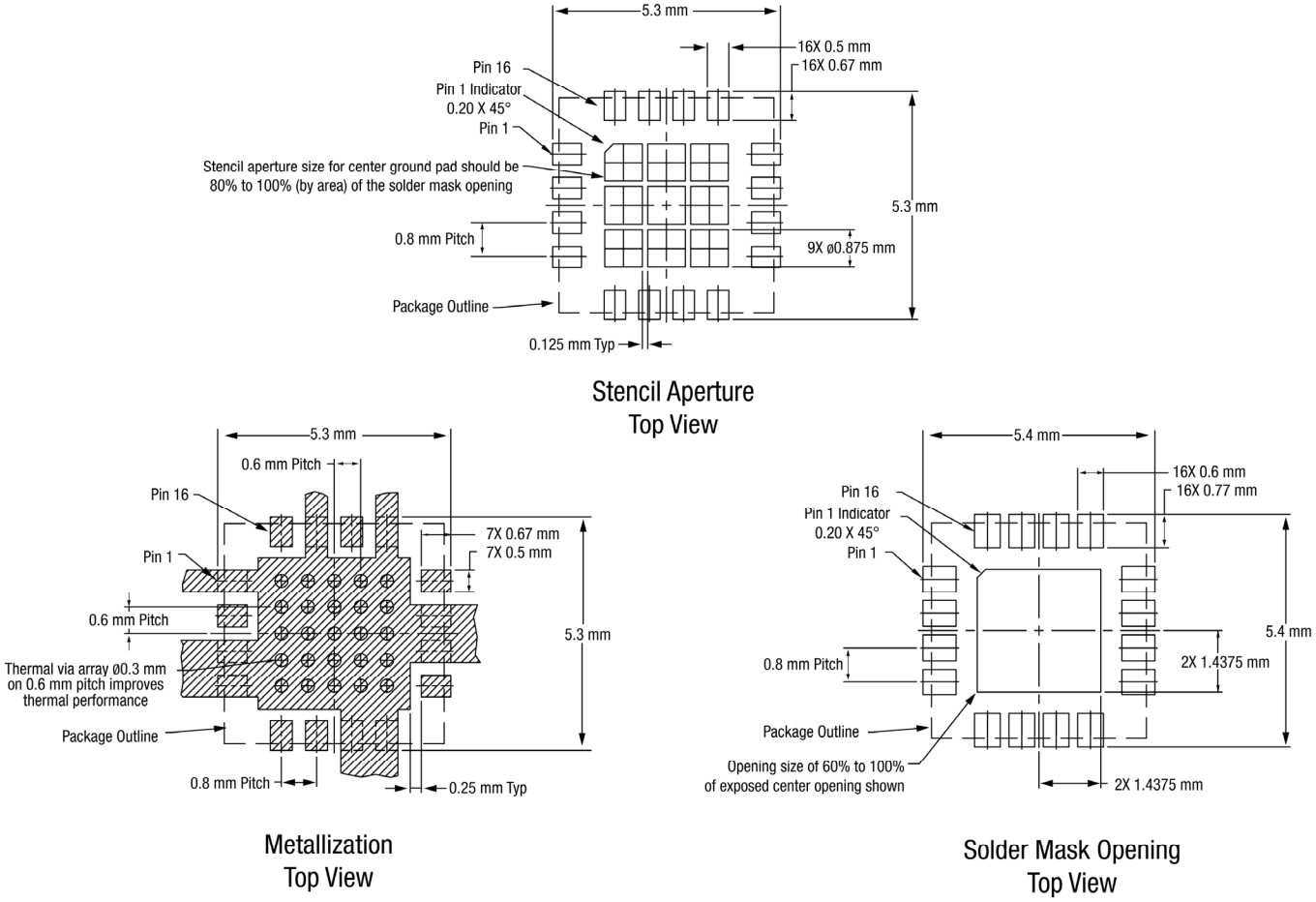


Figure 38. SKY66313-11 Typical Part Marking



Notes:

1. *Thermal vias should be resin filled and capped in accordance with IPC–4761 type VII vias.*
2. *Recommended Cu thickness is 30 to 35 µm.*

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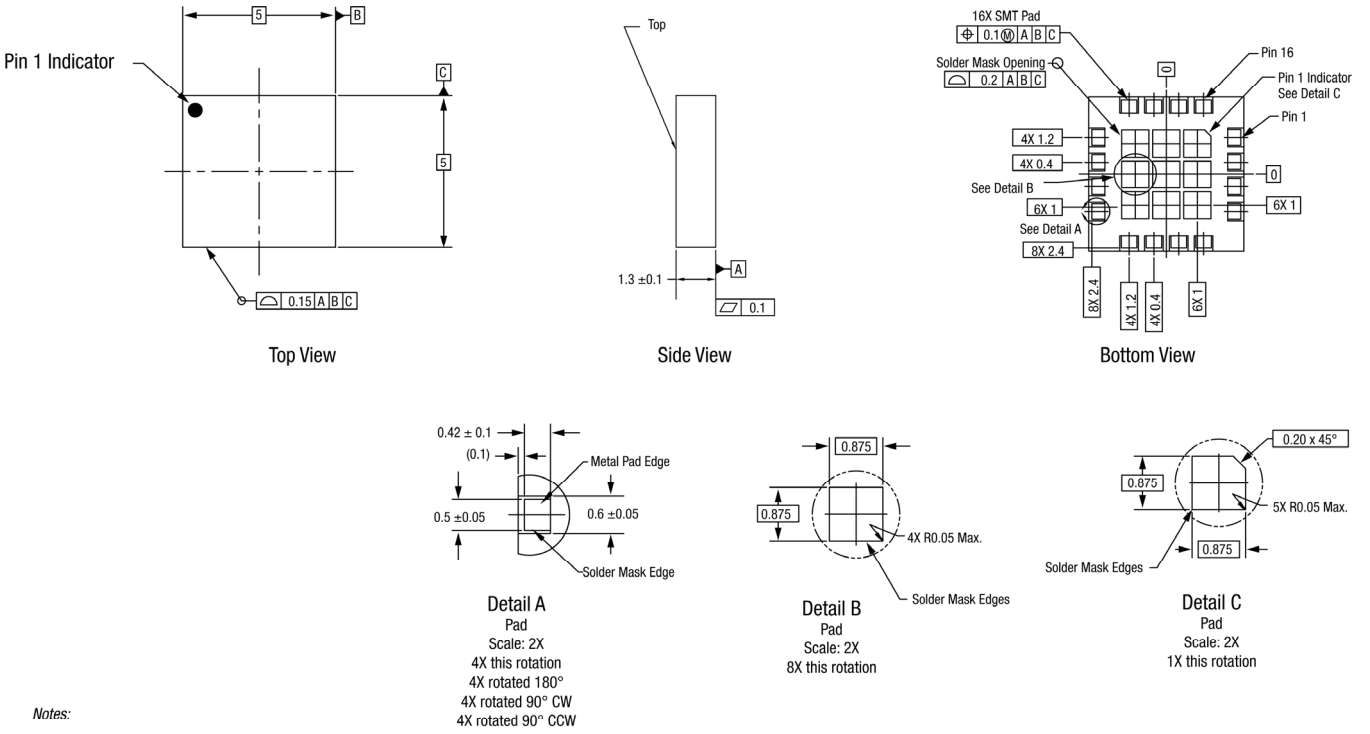
Figure 39. SKY66313-11 PCB Layout Footprint

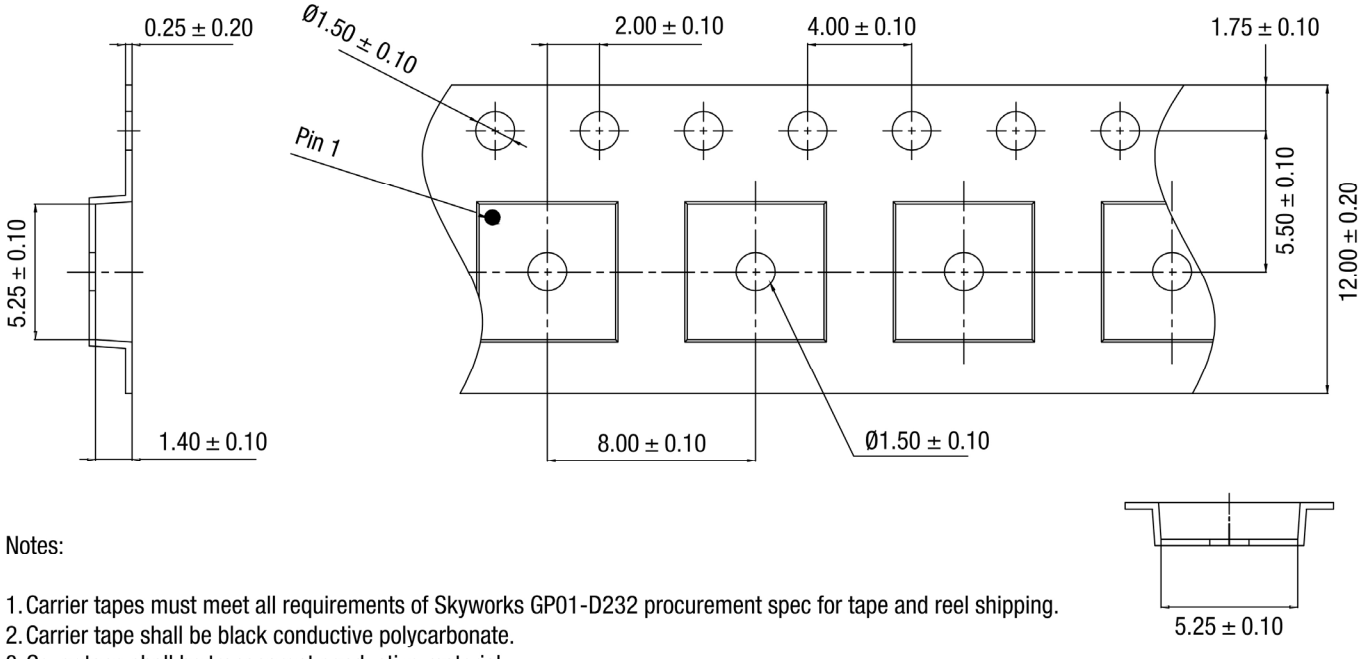


Notes:

1. Dimensions are in millimeters (unless otherwise specified).
2. Dimensions and tolerances are in accordance with ASME Y14.5M–1994.

204567-039

Figure 40. SKY66313-11 Package Dimensions



Notes:

1. Carrier tapes must meet all requirements of Skyworks GP01-D232 procurement spec for tape and reel shipping.
2. Carrier tape shall be black conductive polycarbonate.
3. Cover tape shall be transparent conductive material.
4. ESD-surface resistivity shall be $\leq 1 \times 10^{10}\,\Omega$/square per EIA, JEDEC TNR specification.
5. All measurements are in millimeters.

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Figure 41. SKY66313-11 Tape and Reel Dimensions