

DATA SHEET

# SKY66391-12: 1800 to 1900 MHz Wide Instantaneous Bandwidth High-Efficiency Power Amplifier

## Applications

- FDD and TDD 2G/3G/4G LTE systems
- 3GPP bands 3 and 9 small-cell base stations
- Driver amplifier for micro-base and macro-base stations
- Active antenna array and massive MIMO

## Features

- High-efficiency: PAE = 34.5% @ +28 dBm
- High linearity: +28 dBm with < -50 dBc ACLR with pre-distortion (40 MHz LTE, 8.5 dB PAR signal)
- High gain: 36 dB
- Excellent input and output return loss: to 50 Ω system
- Integrated active bias: performance compensated over temp
- Integrated enable On/Off function: PAEN = 1.7 to 2.5 V
- Single supply voltage: 5.0 V
- Pin-to-pin compatible PA family supporting all 3GPP bands
- Compact (16-pin, 5 × 5 × 1.3 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

## Description

The SKY66391-12 is a high-efficiency fully input/output matched power amplifier (PA) with high gain and linearity. The compact 5 × 5 mm PA is designed for FDD and TDD 2G/3G/4G LTE small cell base stations operating from 1800 to 1900 MHz. The active biasing circuitry is integrated to compensate PA performance over temperature, voltage, and process variation.

The SKY66391-12 is part of a high-efficiency, pin-to-pin compatible PA family supporting all 3GPP bands. Table 1 lists the pin-to-pin compatible parts in the PA family.

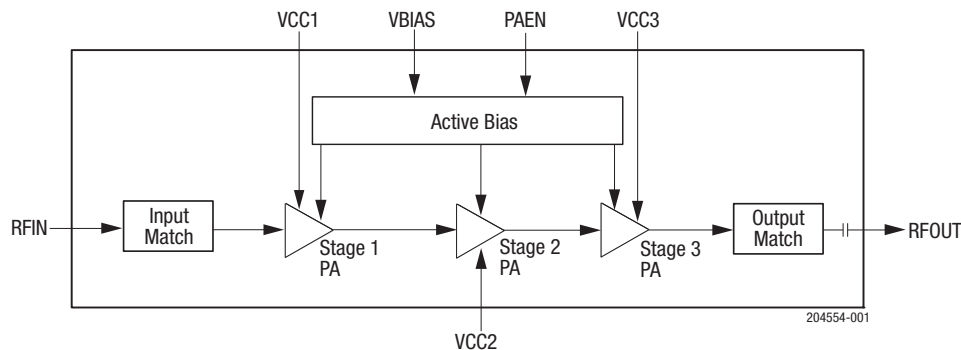
A block diagram of the SKY66391-12 is shown in Figure 1. The device package and pinout for the device are shown in Figure 2. Signal pin assignments and functional pin descriptions are described in Table 2.

**Table 1. Pin-to-Pin Compatible PA Family**

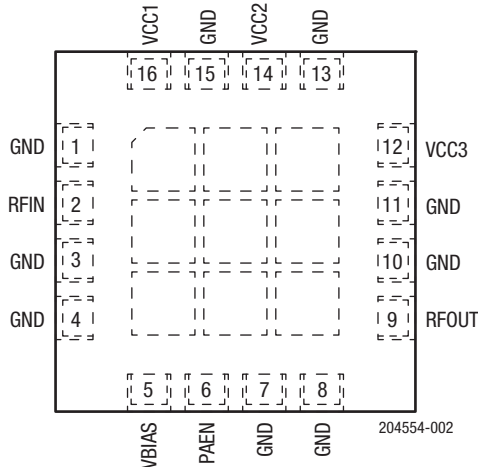
Part Number	Frequency (MHz)	3GPP Band
SKY66391-12	1800 to 1900	Bands 3 and 9
SKY66399-11	1900 to 2000	Bands 2, 25, 33, 36, and 37
SKY66394-11	2000 to 2300	Bands 1, 4, 10, and 23
SKY66397-12	2300 to 2700	Bands 7, 38, and 41



Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.



**Figure 1. SKY66391-12 Block Diagram**



**Figure 2. SKY66391-12 Pinout (Top View)**

**Table 2. SKY66391-12 Signal Descriptions<sup>1</sup>**

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	RFOUT	RF output port
2	RFIN	RF input port	10	GND	Ground
3	GND	Ground	11	GND	Ground
4	GND	Ground	12	VCC3	Stage 3 collector voltage
5	VBIAS	Bias voltage	13	GND	Ground
6	PAEN	PA enable	14	VCC2	Stage 2 collector voltage
7	GND	Ground	15	GND	Ground
8	GND	Ground	16	VCC1	Stage 1 collector voltage

<sup>1</sup> The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

### Technical Description

The matching circuits are contained within the device. An on-chip active bias circuit is included within the device for both input and output stages, which provides excellent gain tracking over temperature and voltage variations.

The SKY66391-12 is internally matched for maximum output power and efficiency. The input and output stages are independently supplied using the VCC1, VCC2, and VCC3 supply lines (pins 16, 14, and 12, respectively). The DC control voltage that sets the bias is supplied by the VCBIAS signal (pin 5).

### Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY66391-12 are provided in Table 3. Recommended operating conditions are specified in Table 4, and electrical specifications are provided in Table 5.

Typical performance characteristics are shown in Figures 3 through 16.

**Table 3. SKY66391-12 Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Minimum	Maximum	Units
RF input power (CW)	P <sub>IN</sub>		+8	dBm
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V <sub>CC</sub>		5.5	V
PA enable	V <sub>EN</sub>		2.8	V
Operating temperature	T <sub>C</sub>	-40	+100	°C
Storage temperature	T <sub>ST</sub>	-55	+125	°C
Junction temperature	T <sub>J</sub>		+150	°C
Power dissipation	P <sub>D</sub>		1.4	W
Device thermal resistance	θ <sub>JC</sub>		20.8	°C/W
Electrostatic discharge:	ESD			
Charged Device Model (CDM)			500	V
Human Body Model (HBM)			1000	V

<sup>1</sup> Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

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**ESD HANDLING:** *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

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**Table 4. SKY66391-12 Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V <sub>CC1</sub> , V <sub>CC2</sub> , V <sub>CC3</sub> , V <sub>BIAS</sub>	4.75	5	5.25	V
PA enable:	PAEN				
ON		1.7	2.0	2.5	V
OFF			0	0.5	V
PA enable current	I <sub>ENABLE</sub>		1	12	μA
Operating frequency	f	1800		1900	MHz
Operating temperature	T <sub>C</sub>	-40	+25	+85	°C

**Table 5. SKY66391-12 Electrical Specifications<sup>1</sup>**

**(Vcc1 = Vcc2 = Vcc3 = VBIAS = 5 V, PAEN = 2.0 V, f = 1842.5 MHz, Tc = +25 °C, Input/Output Load = 50 Ω, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	f		1800		1900	MHz
Small signal gain	IS21I	PIN = -30 dBm	33	35		dB
Gain @ +28 dBm	IS21I@+28dBm	POUT = +28 dBm	34.8	36		dB
Input return loss	IS11I	PIN = -20 dBm	11	16		dB
Output return loss	IS22I	PIN = -20 dBm	10	12		dB
Reverse isolation <sup>2</sup>	IS12I	PIN = -30 dBm		50		dB
ACLR @ +28 dBm	ACLR	POUT = +28 dBm (40 MHz LTE, 8.5 dB PAR signal)		-31	-27.5	dBc
Saturated output power	PSAT	CW, PIN = +5 dBm		+35		dBm
Output power at 3 dB gain compression	P3dB	CW, reference to small signal gain (PIN= -30 dBm)	+34.5	+36		dBm
2 <sup>nd</sup> harmonic	2fo	CW, POUT = +28 dBm		-30	-24	dBc
3 <sup>rd</sup> harmonic	3fo	CW, POUT = +28 dBm		-55	-45	dBc
Power-added efficiency	PAE	CW, POUT = +28 dBm	31	34.5		%
Quiescent current	ICCQ	No RF signal		80		mA

<sup>1</sup> Performance is guaranteed only under the conditions listed in this table.

<sup>2</sup> Not tested in production. Verified by design.

### Typical Performance Characteristics

( $V_{CC1} = V_{CC2} = V_{CC3} = V_{BIAS} = 5\text{ V}$ ,  $PAEN = 2.0\text{ V}$ ,  $f = 1842.5\text{ MHz}$ ,  $T_c = +25\text{ }^\circ\text{C}$ , Input/Output Load =  $50\ \Omega$ , Unless Otherwise Noted)

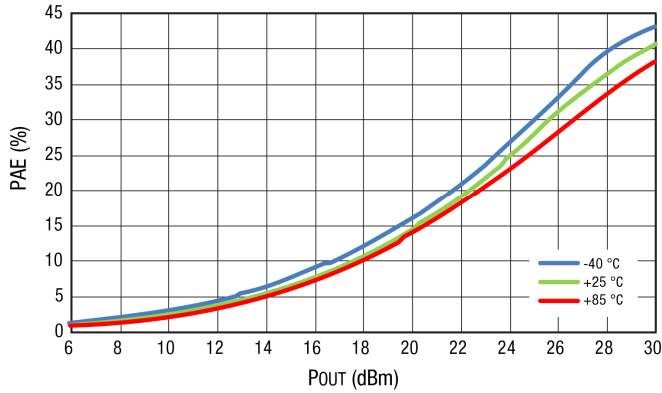


Figure 3. PAE vs Pout Across Frequency

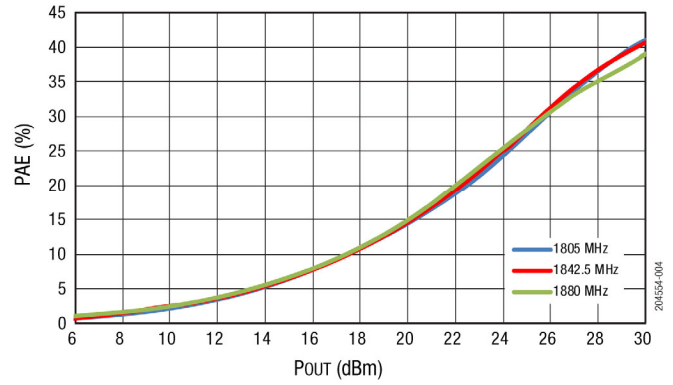


Figure 4. PAE vs Pout Across Temperature

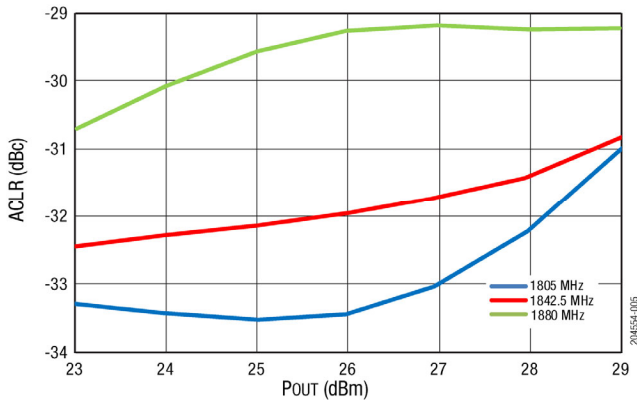


Figure 5. ACLR2 (2x20 MHz) vs. Pout Across Frequency

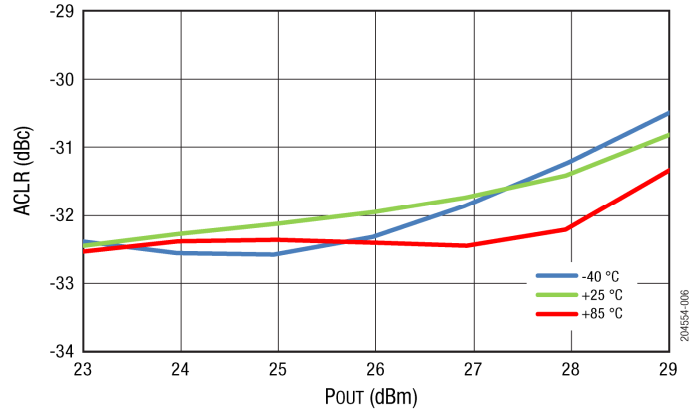


Figure 6. ACLR2 (2x20 MHz) vs Pout Across Temperature

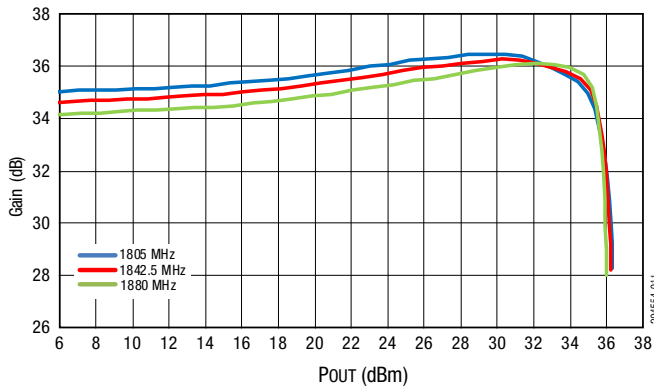


Figure 7. Gain vs. Pout Across Frequency

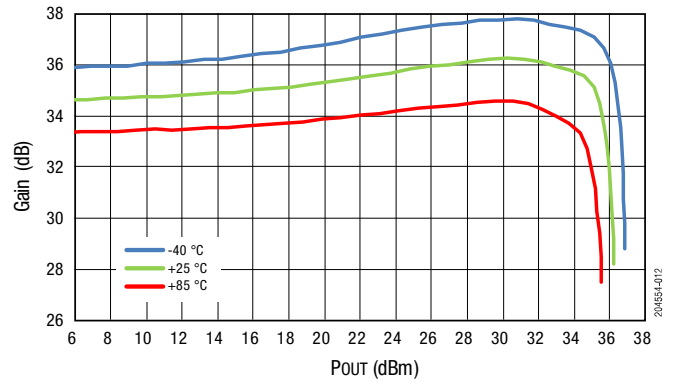


Figure 8. Gain vs Pout Across Temperature

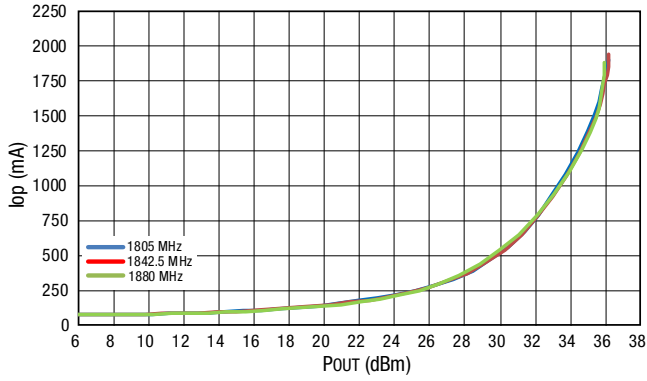


Figure 9. Iop vs. Pout Across Frequency

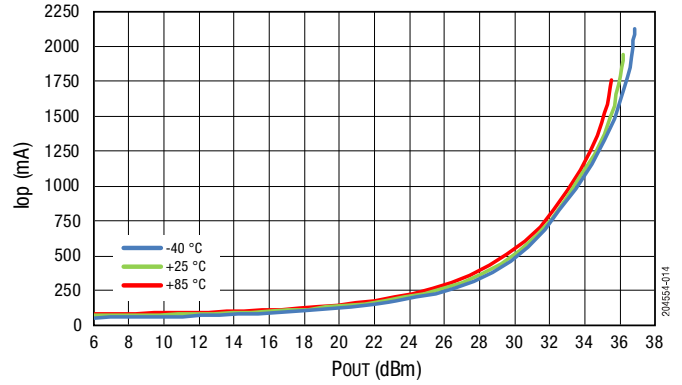


Figure 10. Iop vs Pout Across Temperature

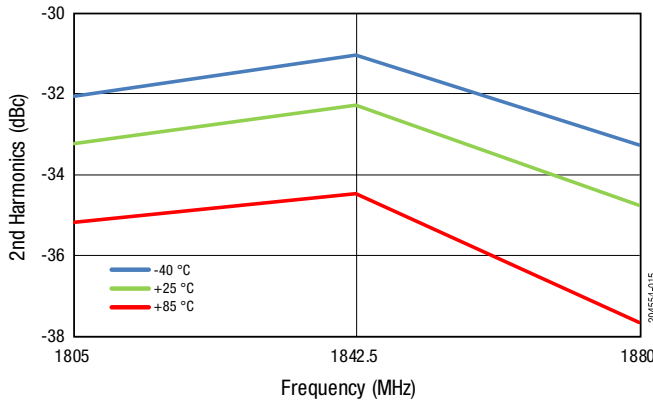


Figure 11. Second Harmonic @ +28 dBm (CW) vs Frequency Across Temperature

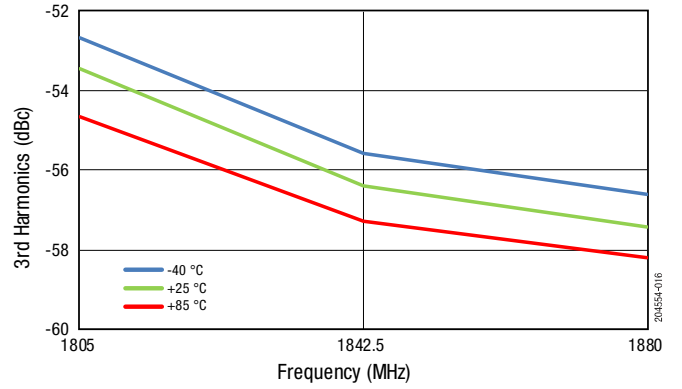


Figure 12. Third Harmonic @ +28 dBm (CW) vs Frequency Across Temperature

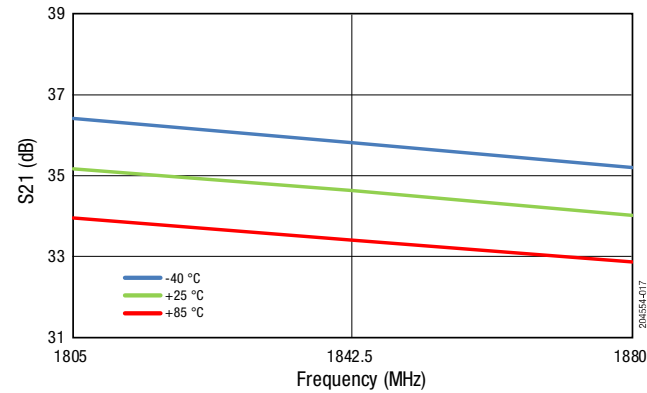


Figure 13. S21 vs Frequency Across Temperature (Pin = -20 dBm)

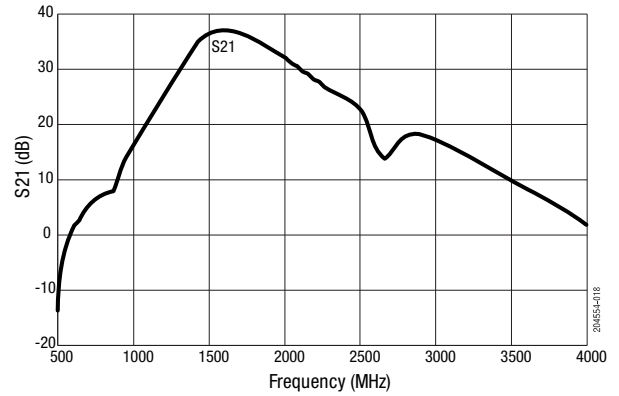
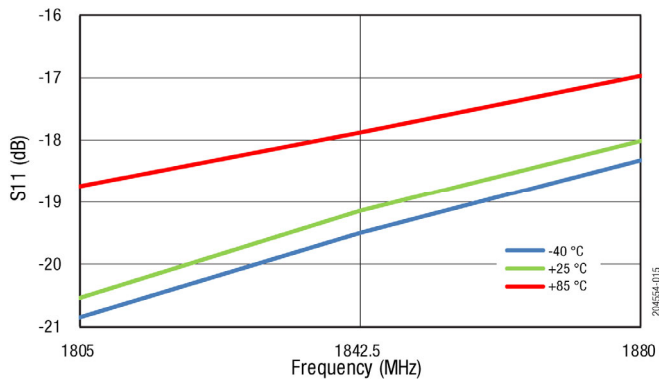
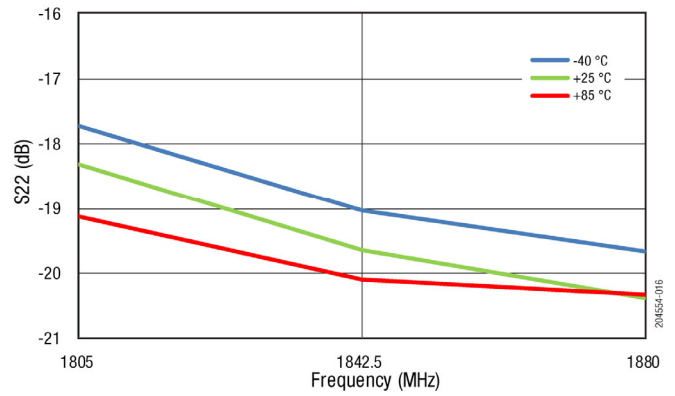


Figure 14. Wide Band Small Signal Gain vs Frequency



**Figure 15. S11 vs Frequency Across Temperature (P<sub>IN</sub> = -20 dBm)**



**Figure 16. S22 vs Frequency Across Temperature (P<sub>IN</sub> = -20 dBm)**

## Evaluation Board Description

The SKY66391-12 Evaluation Board is used to test the performance of the SKY66391-12 PA. An application schematic is provided in Figure 17. Table 6 provides the Bill of Materials (BOM) list for Evaluation Board components.

An assembly drawing for the Evaluation Board is shown in Figure 18. Board layer details are shown in Figure 19. Layer detail physical characteristics are noted in Figure 20.

## Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SKY66391-12 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Because the circuit board acts as the heat sink, it must shunt as much heat as possible from the device.

Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

**NOTE:** A poor connection between the ground pad and ground increases junction temperature ( $T_J$ ), which reduces the life of the device.

## Evaluation Board Test Procedure

### Turn-On Sequence

1. Connect 50  $\Omega$  Test Equipment or Load to the input and output RF ports of the Evaluation Board.
2. Connect the DC ground.
3. Connect all VCCs and VBIAS lines to a +5 V supply. Connect PAEN to a 2.0 V supply.
4. Without applying RF, turn on the 5 V supply, then turn on the 2 V PAEN.
5. Apply RF signal data at -30 dBm and observe that the gain of the device is approximately 35 dB. Begin measurements.

### Turn-Off Sequence

1. Turn off the RF input to the device.
2. Turn off PAEN (set to 0 V).
3. Turn off all VCCs and VBIAS.

**NOTE:** It is important to adjust the VCC voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.



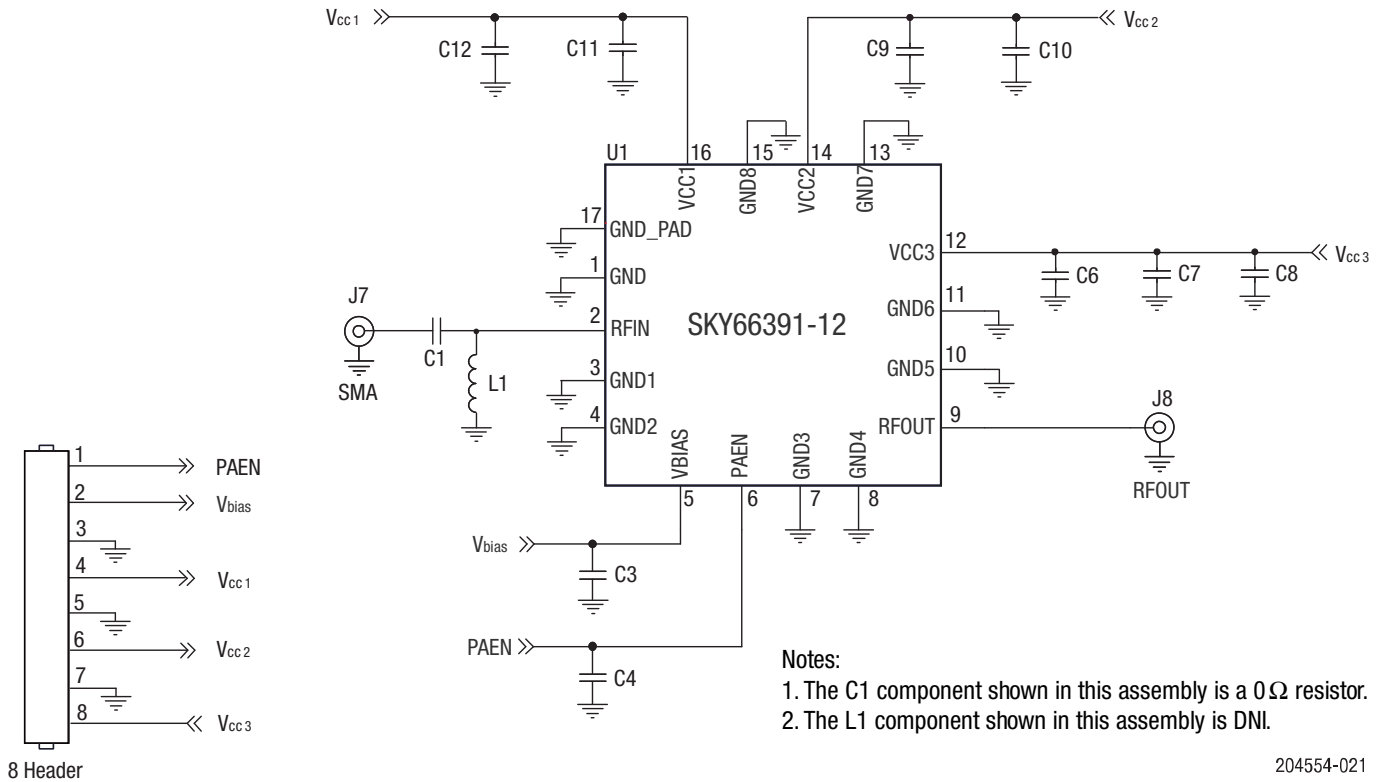
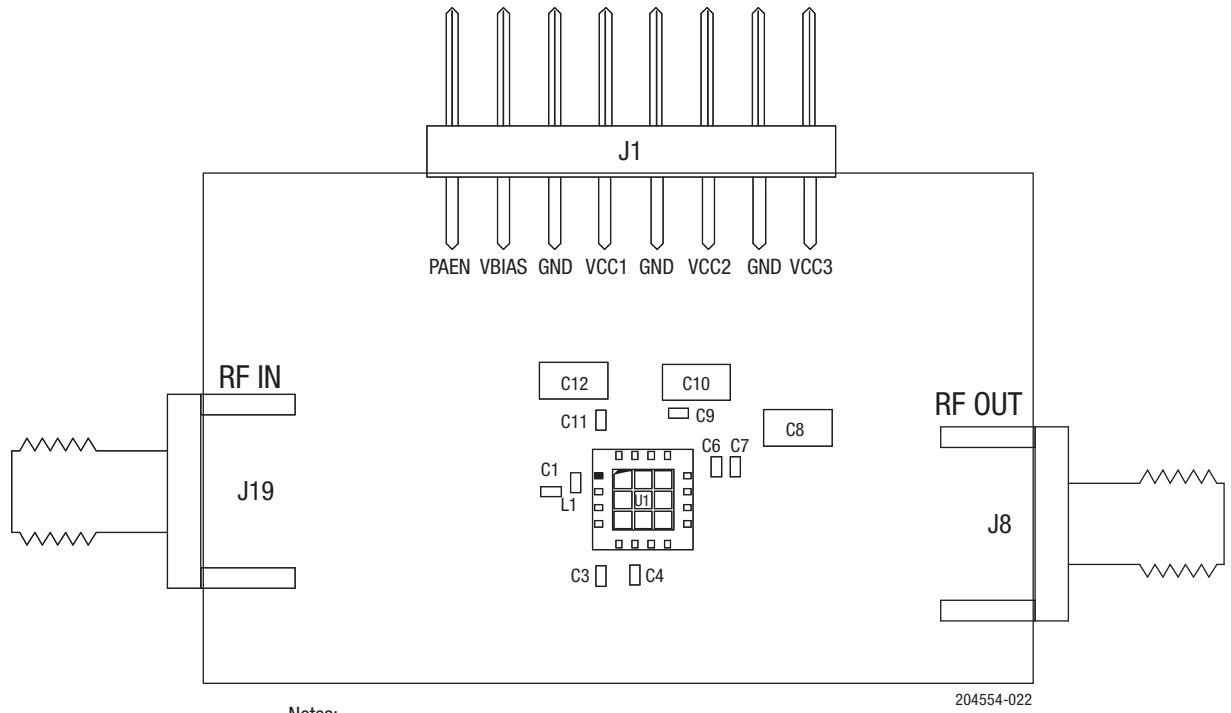


Figure 17. SKY66391-12 Application Schematic

Table 6. SKY66391-12 Evaluation Board Bill of Materials (BOM)

Component	Description	Size
C1	Resistor, 0 Ω, 0.063 W	0402
C3	Ceramic capacitor, 1 μF, ±10%, 16 V	0402
C4, C7	Ceramic capacitor, 3300 pF, X7R, ±10%, 50 V	0402
C6, C9, C11	Ceramic capacitor, 0.47 μF	0402
C8, C10, C12	Ceramic capacitor, 10 μF, X7R, ±10%, 16 V	1206
L1	DNI	
SKY66391-12EK1	Evaluation Board	



Notes:

1. Evaluation Board Gerber files are available on request.
2. The C1 component shown in this assembly is a 0Ω resistor.
3. The L1 component shown in this assembly is DNI.

**Figure 18. Evaluation Board Assembly Drawing**

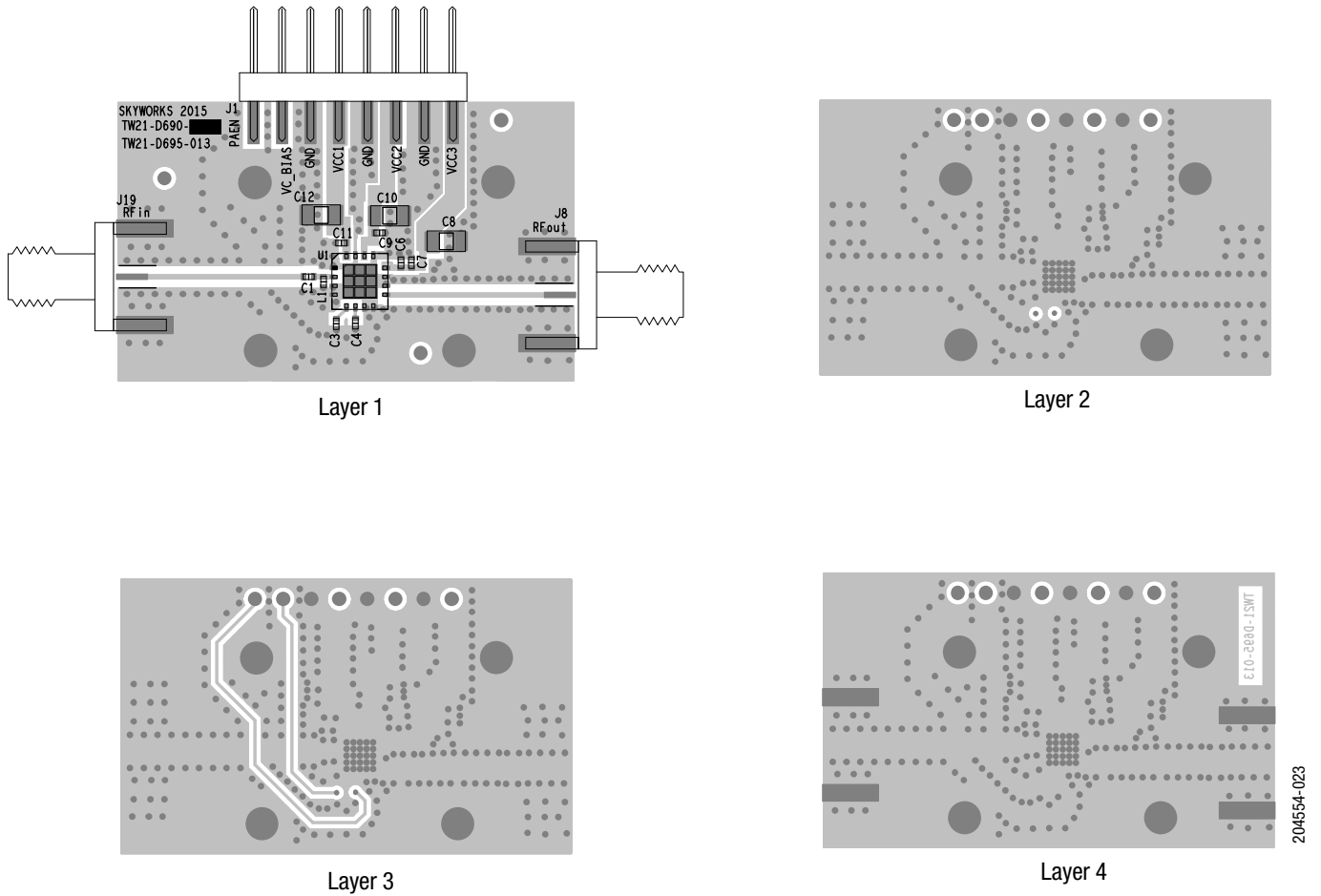


Figure 19. Board Layer Detail

50 Ohm	Cross Section	Name	Thickness (mm)	Materials
W = 0.500 mm 		TMask	0.010	Solder Resist
		L1	0.035	Cu, 1 oz.
		Dielectric	0.250	R04350
		L2	0.035	Cu, 1 oz.
		Dielectric	0.350	FR4
		L3	0.035	Cu, 1 oz.
		Dielectric	0.250	FR4
		L4	0.035	Cu, 1 oz.
		BMask	0.010	Solder Resist

204554-024

Figure 20. Layer Detail Physical Characteristics

## Application Circuit Notes

**Center Ground.** It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and work well under the device if solder migration is an issue.

**GND (pins 1, 3, 4, 7, 8, 10, 11, 13, and 15).** Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

**VCBIAS (pin 5).** The bias supply voltage for each stage, nominally set to +5 V.

**RFOUT (pin 9).** Amplifier RF output pin ( $Z_0 = 50 \Omega$ ). The module includes an internal DC blocking capacitor. All impedance matching is provided internal to the module.

**VCC1, VCC2, and VCC3 (pin 16, 15, and 12, respectively).** Supply voltage for each stage collector bias is nominally set to 5 V. The evaluation board has inductors L1 and L2. These are place holders, and should be populated with  $0 \Omega$  resistors. Bypass and decoupling capacitors C6 through C12 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.

**RFIN (pin 2).** Amplifier RF input pin ( $Z_0 = 50 \Omega$ ). All impedance matching is provided internal to the module.

## Package Dimensions

Typical part marking for the device is shown in Figure 21. The PCB layout footprint for the SKY66391-12 is shown in Figure 22. Package dimensions are shown in Figure 23, and tape and reel dimensions are provided in Figure 24.

## Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY66391-12 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

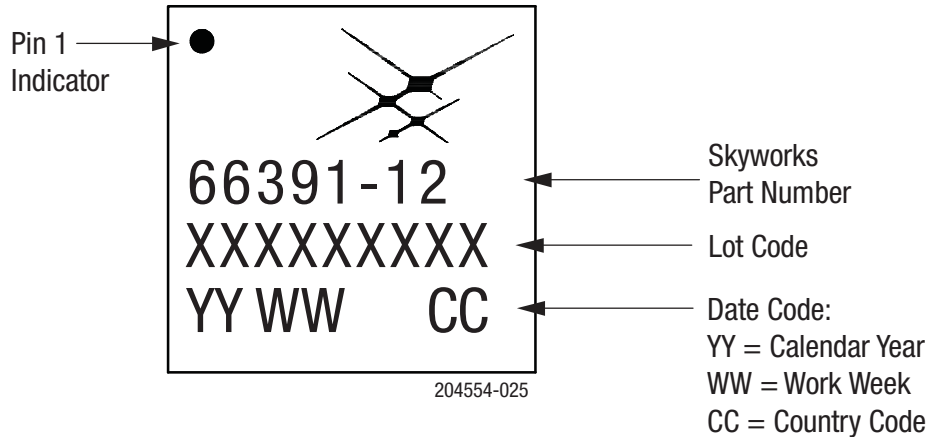


Figure 21. SKY66391-12 Typical Part Marking

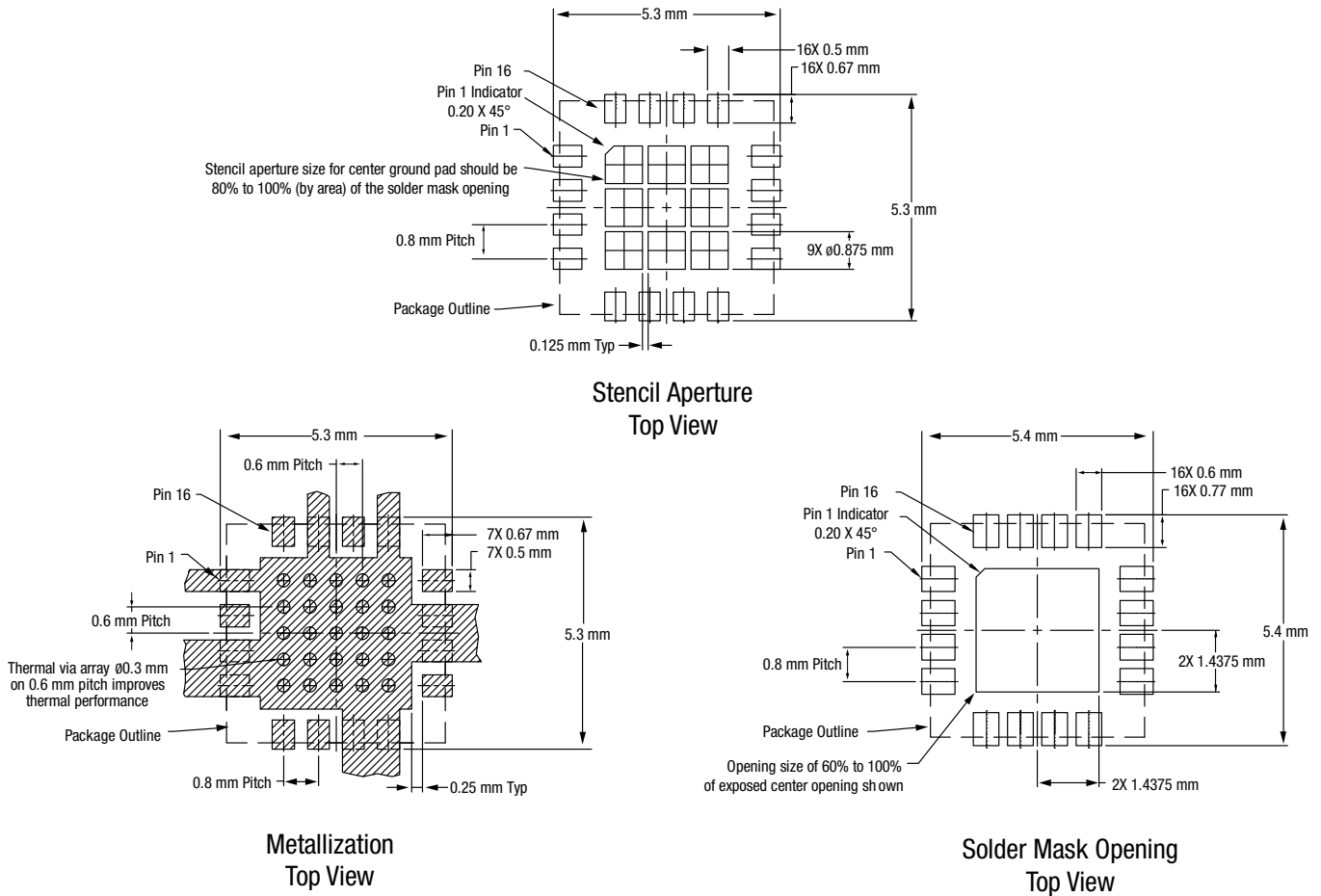


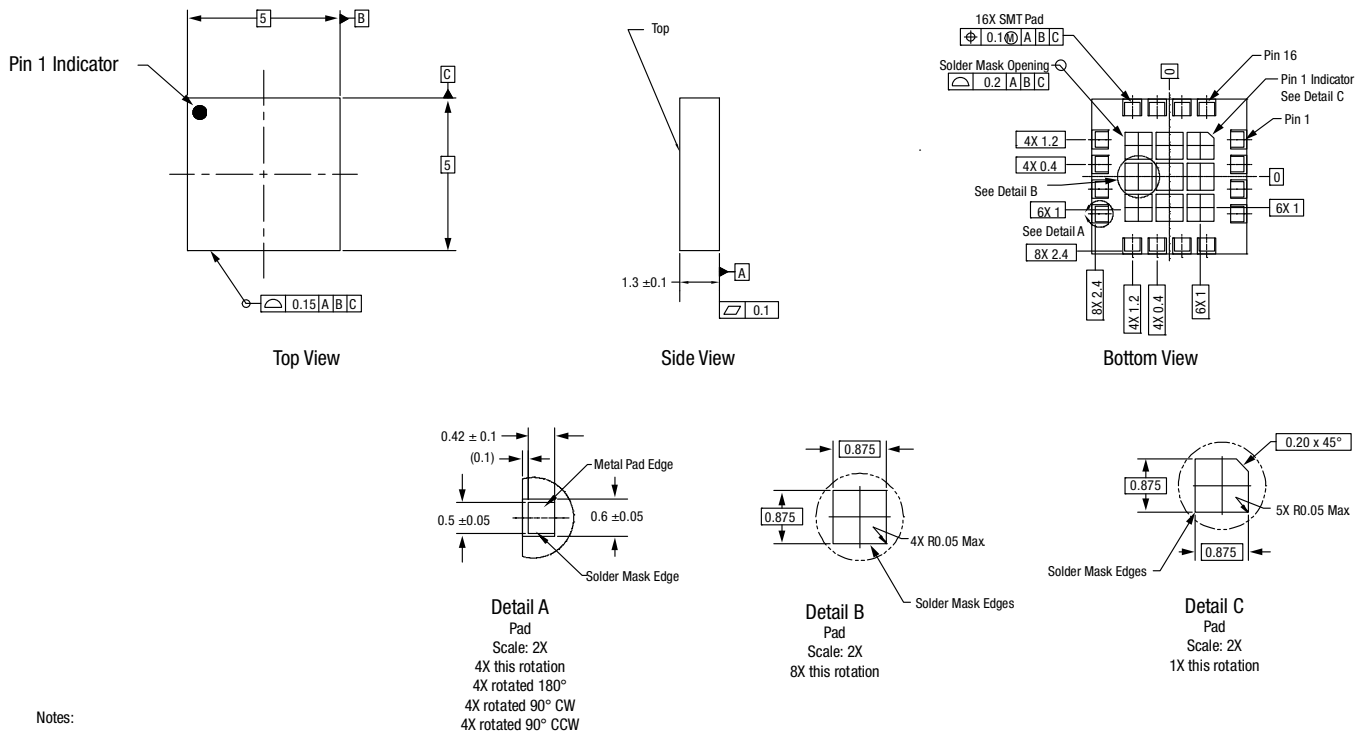
Figure 22. SKY66391-12 PCB Layout Footprint

Notes:

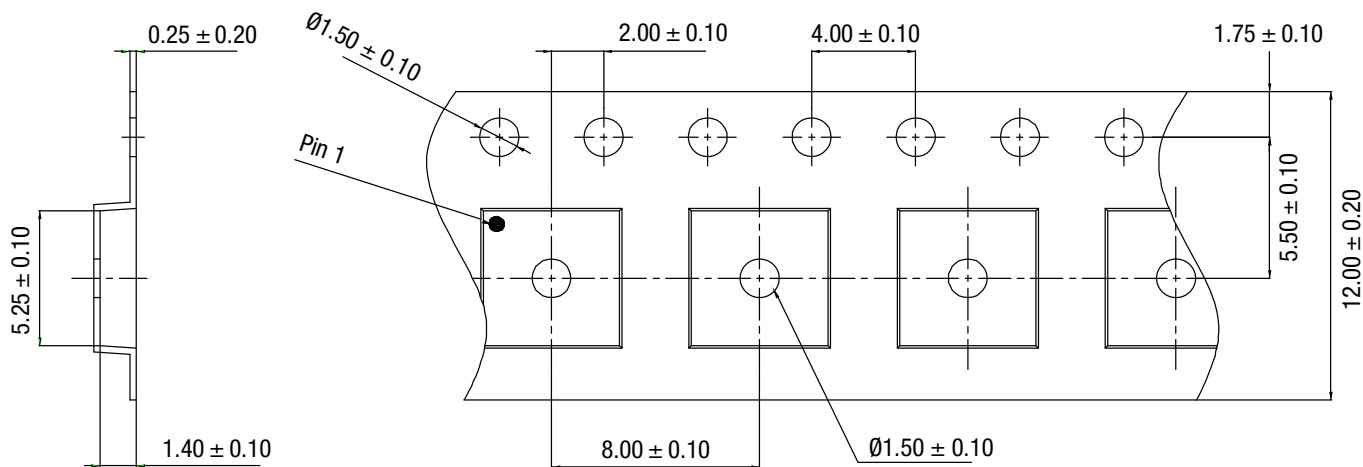
1. Thermal vias should be resin filled and capped in accordance with IPC-4761 type VII vias.
2. Recommended Cu thickness is 30 to 35  $\mu\text{m}$ .

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**Figure 23. SKY66391-12 Package Dimensions**



**Notes:**

1. Carrier tapes must meet all requirements of Skyworks GP01-D232 procurement spec for tape and reel shipping.
2. Carrier tape shall be black conductive polycarbonate.
3. Cover tape shall be transparent conductive material.
4. ESD-surface resistivity shall be  $\leq 1 \times 10^{10} \Omega/\text{square}$  per EIA, JEDEC TNR specification.
5. All measurements are in millimeters.

**Figure 24. SKY66391-12 Tape and Reel Dimensions**