DATA SHEET

SKY67183-396LF: 400 to 6000 MHz Broadband Low-Noise Amplifier

Applications

- FDD and TDD 4G LTE and 5G NR systems
- Active antenna array and massive MIMO
- Receive LNA for micro-cell, macro-cell, and small cell base stations
- Land mobile radios and military communications
- Low-noise broadband gain block and driver amplifier

Features

- Low-noise amplifier:
  - Very low noise figure
  - Temperature and process-stable active bias up to +115 °C
  - Wide operating voltage range
  - Low gain slope over operating band
  - Excellent input return loss
- Integrated controller:
  - Stable amplifier bias
  - Temperature compensation
  - True logic level thresholds
  - Fast response time
- Excellent broadband flat gain performance
- Minimal BOM count
- Low current I_{DD} 56 mA @ 5 V
- Fast rise/fall time ENABLE function suitable for TDD application
- Miniature DFN (8-pin, 2 x 2 mm) package (MSL1 @ 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

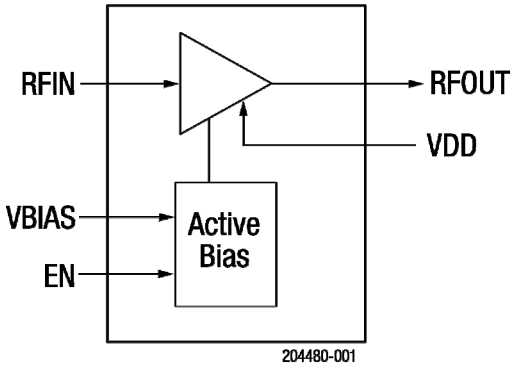


Figure 1. SKY67183-396LF Block Diagram

Description

The SKY67183-396LF is a wide-band low-noise amplifier with superior gain flatness and exceptional linearity.

The compact 2 x 2 mm, 8-pin Dual Flat No Lead packaged LNA is designed for FDD and TDD 4G LTE and 5G NR infrastructure systems operating from 400 to 6000 MHz.

The internal active bias circuitry provides stable performance over temperature and process variation.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

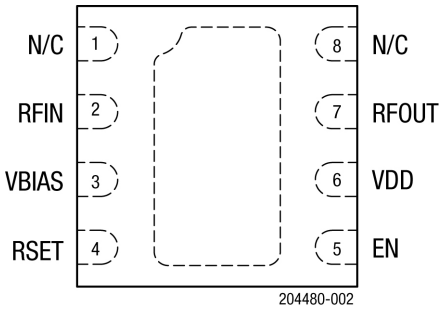


Figure 2. SKY67183-396LF Pinout (Top View)

Table 1. SKY67183-396LF Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	N/C	No connection (may be connected to ground with no change in performance)	5	EN	Enable voltage to LNA
2	RFIN	RF input (DC blocking capacitor required)	6	VDD	VDD voltage to LNA
3	VBIAS	Bias voltage for input gate	7	RFOUT	RF output. DC blocking capacitor is required.
4	RSET	External resistor to set bias current	8	N/C	No connection (may be connected to ground with no change in performance)

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY67183-396LF are provided in Table 2. Recommended operating conditions are shown in Table 3. Thermal data is shown in Table 4. Electrical specifications are provided in Tables 5, 6, 7, and 8.

Table 2. SKY67183-396LF Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}		5.5	V
LNA enable	EN	-0.5	2.8	V
Quiescent supply current	I_{DQ}		100	mA
RF input power (C/W)	P_{IN}		+22	dBm
Storage temperature	T_{STG}	-40	+150	°C
Operating temperature	T_A	-40	+115	°C
Junction temperature	T_J		+150	°C
Electrostatic discharge:	ESD			
Charged Device Model (CDM), Class C3			1000	V
Human Body Model (HBM), Class 1A			250	V

1 Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***ESD HANDLING**: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

Table 3. SKY67183-396LF Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply voltage	VDD	3.3	5.0	5.25	V
LNA enable:	EN				
ON			0	0.63	V
OFF		1.17	1.8	2.4	V

Table 4. SKY67183-396LF Electrical Specifications: Thermal Data[1]
(V_{DD} = 5.0 V, Enable = GND, T_A = +25 °C, P_{IN} = No RF, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Thermal resistance	θ_{JC}			79.8		°C/W
Channel temperature @ +115 °C reference (package heat slug)	T_J	V_{DD} = 5.0 V, I_{DQ} = 61 mA, no RF applied, dissipated power = 0.31 W		139		°C

[1] Performance is guaranteed only under the conditions listed in this table.

Table 5. SKY67183-396LF Electrical Specifications: 4200 to 4900 MHz Optimized BoM in Table 8[1]
(V_{DD} = 5.0 V, Enable = GND, T_A = +25 °C, P_{IN} = -20 dBm, Characteristic Impedance [Z_O] = 50 Ω, f = 4500 MHz, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
RF Specifications						
Noise figure	NF	@ 4200 MHz @ 4500 MHz @ 4900 MHz		0.5 0.5 0.6	1.0 1.0 1.1	dB dB dB
Small signal gain	|S21|	@ 4200 MHz @ 4500 MHz @ 4900 MHz	16.5	18.2 18.2 17.7		dB dB dB
Input return loss	|S11|	@ 4200 MHz @ 4500 MHz @ 4900 MHz	12	16.1 32.8 21.9		dB dB dB
Output return loss	|S22|	@ 4200 MHz @ 4500 MHz @ 4900 MHz	10	11.2 23.2 14.9		dB dB dB
Reverse isolation	|S12|	@ 4200 MHz @ 4500 MHz @ 4900 MHz	26	32 32 32		dB dB dB
Third order output intercept (-20 dBm input/1 MHz tone)	OIP3	@ 4200 MHz @ 4500 MHz @ 4900 MHz	+27	+29 +29 +28.5		dBm dBm dBm
1 dB output compression point	OP1dB	@ 4200 MHz @ 4500 MHz @ 4900 MHz	+16	+20 +19 +20		dBm dBm dBm
DC Specifications						
Supply voltage	V_{DD}			5.0		V
Quiescent current	IDD		45	56	67	mA
Settling time 0.3 dB[2] Settling time 0.1 dB[3]	TS1 TS2	@ 4500 MHz		0.3 0.31	0.9 0.9	us us

[1] Performance is guaranteed only under the conditions listed in this table.

[2] Settling time 0.3 dB is measured from the time the LNA enable reaches 50% of LNA enable “on” level to the time at which the RF output power achieves within 0.3 dB of the average steady-state “on” level.

[3] Settling time 0.1 dB is measured from the time the LNA enable reaches 50% of LNA enable "on" level to the time at which the RF output power achieves within 0.1 dB of the average steady-state “on” level.

Typical Performance Characteristics
4200 to 4900 MHz (VDD = 5 V, PIN = -20 dBm, Characteristic Impedance [Zo] = 50 Ω, Unless Otherwise Noted)

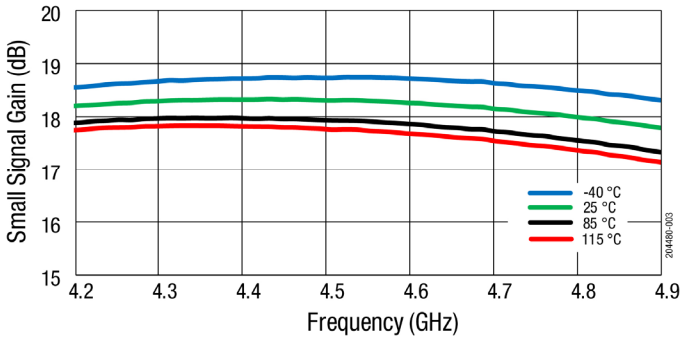


Figure 3. Small Signal Gain (dB) vs Frequency (GHz)

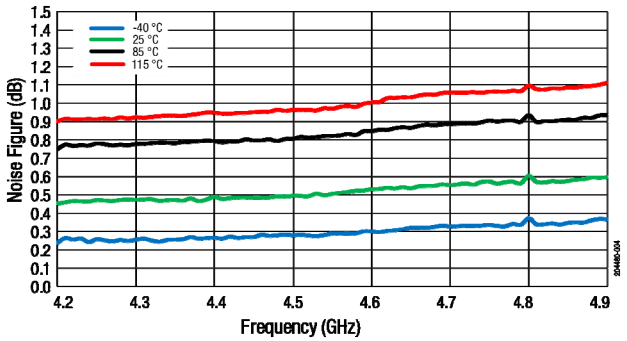


Figure 4. Noise Figure (dB) vs Frequency (GHz)

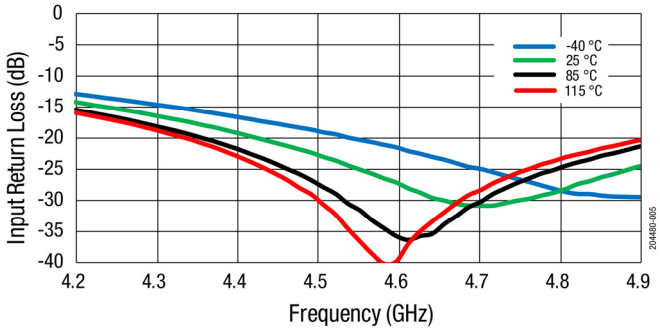


Figure 5. Input Return Loss (dB) vs Frequency

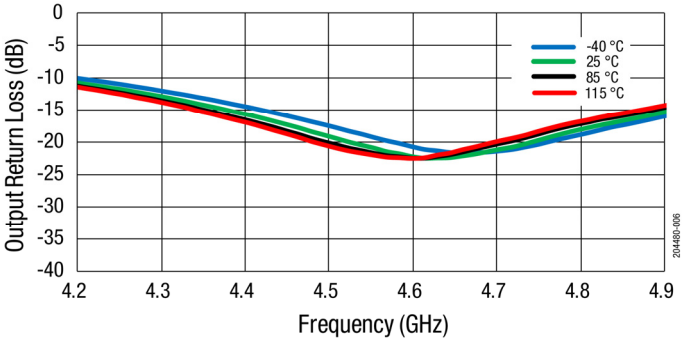


Figure 6. Output Return Loss (dB) vs Frequency

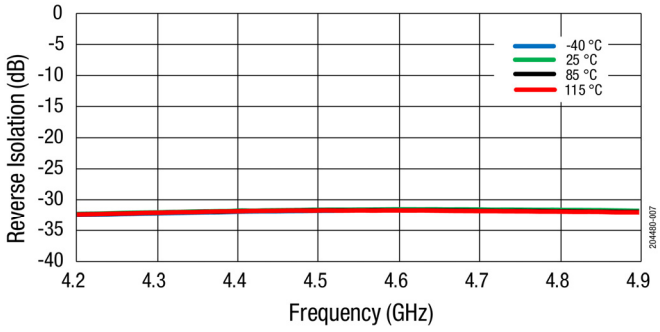


Figure 7. Reverse Isolation (dB) vs Frequency (GHz)

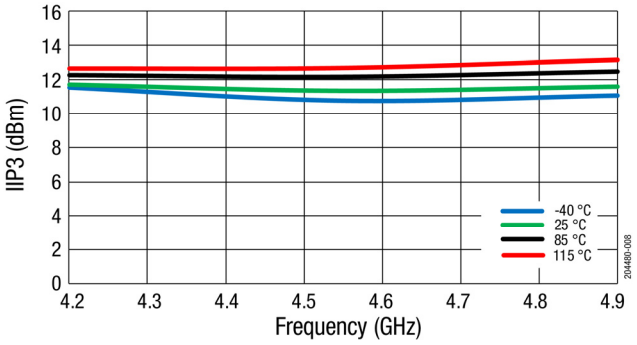


Figure 8. IIP3 (dBm) vs Frequency (GHz)

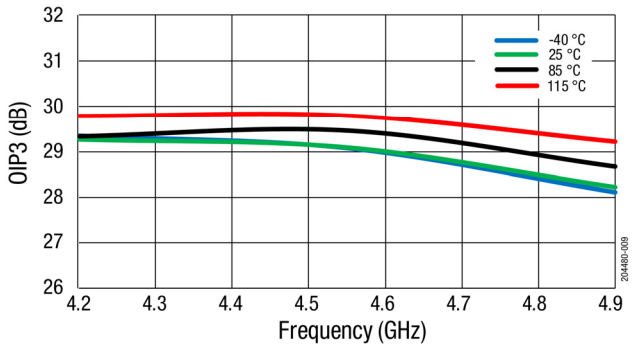


Figure 9. OIP3 (dBm) vs Frequency (GHz)

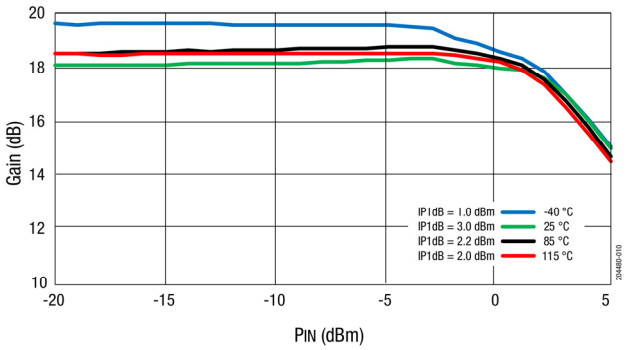


Figure 10. Gain (dB) vs PIN (dBm)

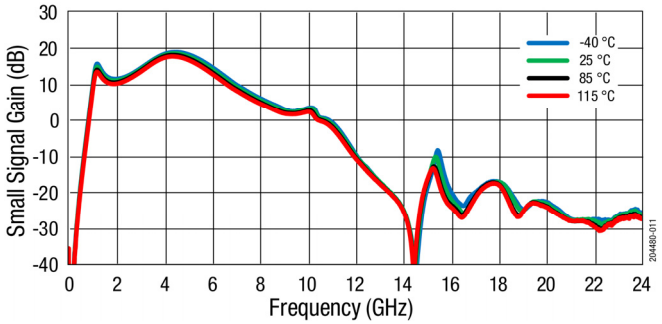


Figure 11. Small Signal Gain (dB) vs Frequency (GHz)

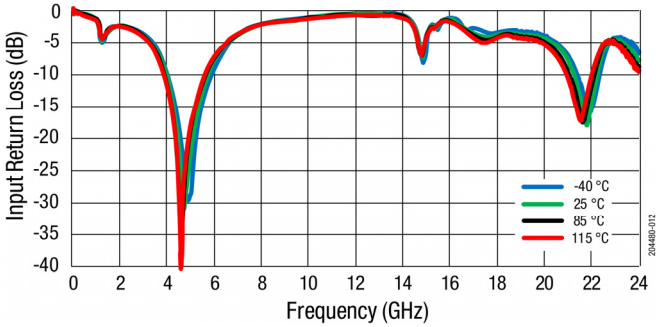


Figure 12. Input Return Loss (dB) vs Frequency (GHz)

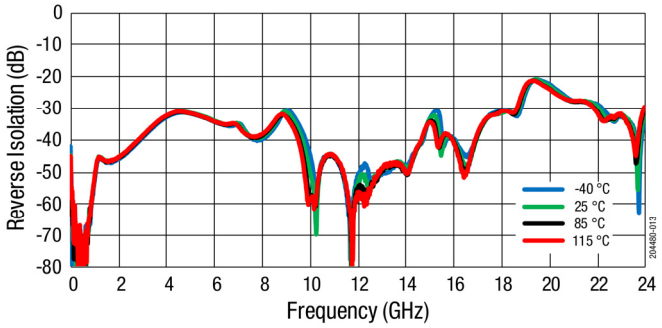


Figure 13. Reverse Isolation (dB) vs Frequency (GHz)

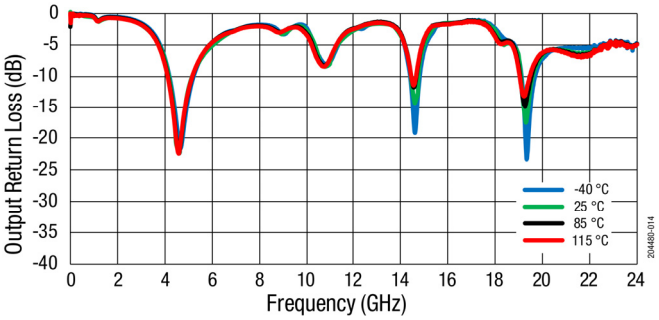


Figure 14. Output Return Loss (dB) vs Frequency (GHz)

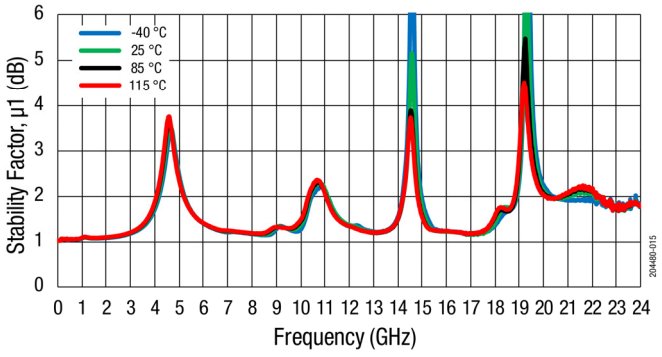


Figure 15. Stability Factor, µ1 (dB) vs Frequency (GHz)

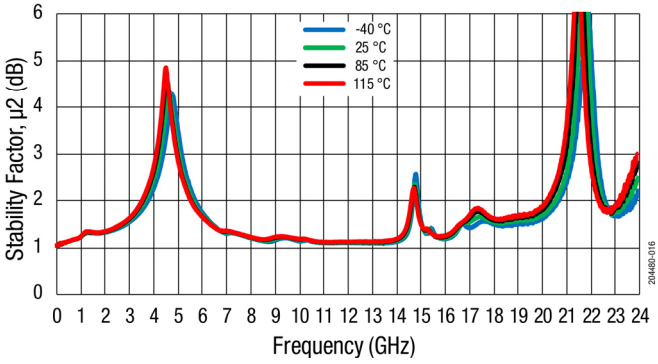


Figure 16. Stability Factor, µ2 (dB) vs Frequency (GHz)

Table 6. SKY67183-396LF Electrical Specifications: 3300 to 3800 MHz Optimized BOM in Table 9[1]
(V_{DD} = 5.0 V, Enable = GND, T_A = +25 °C, P_{IN} = -20 dBm, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
RF Specifications						
Noise figure	NF	@ 3300 MHz @ 3400 MHz @ 3600 MHz @ 3800 MHz		0.42 0.42 0.43 0.49	0.72 0.72 0.72 0.80	dB dB dB dB
Gain	|S21|	@ 3300 MHz @ 3400 MHz @ 3600 MHz @ 3800 MHz	16.9 17.0 17.0 16.9	19.1 19.1 19.1 18.9		dB dB dB
Input return loss	|S11|	@ 3300 MHz @ 3400 MHz @ 3600 MHz @ 3800 MHz	9.6 11.2 15.4 18.3	12.3 14.4 20.6 31.9		dB dB dB dB
Output return loss	|S22|	@ 3300 MHz @ 3400 MHz @ 3600 MHz @ 3800 MHz	6.5 7.7 10.1 13.1	9.8 11.8 16.4 19.0		dB dB dB dB
Reverse isolation	|S12|	@ 3300 MHz @ 3400 MHz @ 3600 MHz @ 3800 MHz	29.6 29.4 29.0 28.8	33.1 32.8 32.4 32.1		dB dB dB dB
Third order output intercept point	OIP3	P_{IN} = -20 dBm, Δ Tone = 1 MHz: @ 3300 MHz @ 3400 MHz @ 3600 MHz @ 3800 MHz	 27.0 27.1 25.8 28.9	 30.3 30.3 28.9 34.7		 dBm dBm dBm dBm
1 dB output compression point	OP1dB	@ 3300 MHz @ 3400 MHz @ 3600 MHz @ 3800 MHz	18.1 18.0 17.9 18.4	20.3 20.2 20.1 20.6		dBm dBm dBm dBm
DC Specifications						
Supply voltage	V_{DD}			5.0		V
Quiescent current	I_{DD}		45	56	67	mA
Settling time 0.3 dB[2] Settling time 0.1 dB[3]	T_{S1} T_{S2}	@ 3600 MHz		0.28 0.29		us us

[1] Verified by characterization.

[2] Settling time 0.3 dB is measured from the time the LNA enable reaches 50% of LNA enable “on” level to the time at which the RF output power achieves within 0.3 dB of the average steady-state “on” level.

[3] Settling time 0.1 dB is measured from the time the LNA enable reaches 50% of LNA enable "on" level to the time at which the RF output power achieves within 0.1 dB of the average steady-state “on” level.

Typical Performance Characteristics

3300 to 3800 MHz, (VDD = 5 V, TA = +25 °C, PIN = -20 dBm, Characteristic Impedance [Zo] = 50 Ω Unless Otherwise Noted)

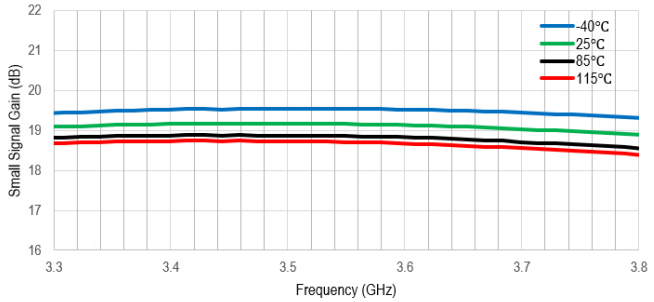


Figure 17. Small Signal Gain (dB) vs Frequency (GHz)

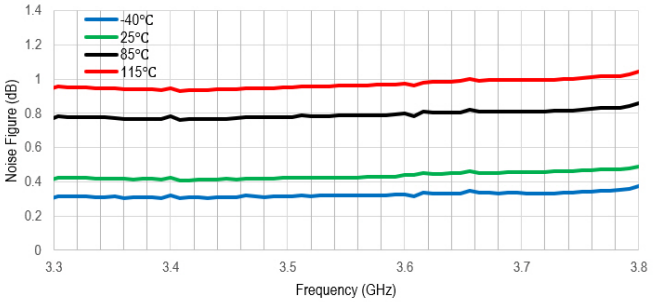


Figure 18. Noise Figure (dB) vs Frequency (GHz)

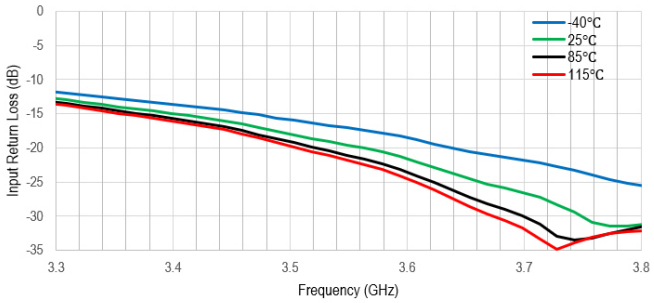


Figure 19. Input Return Loss (dB) vs Frequency

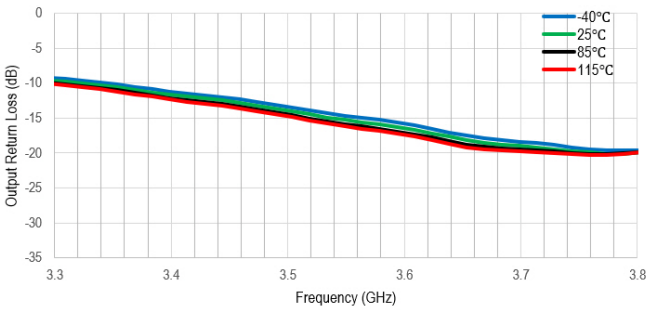


Figure 20. Output Return Loss (dB) vs Frequency

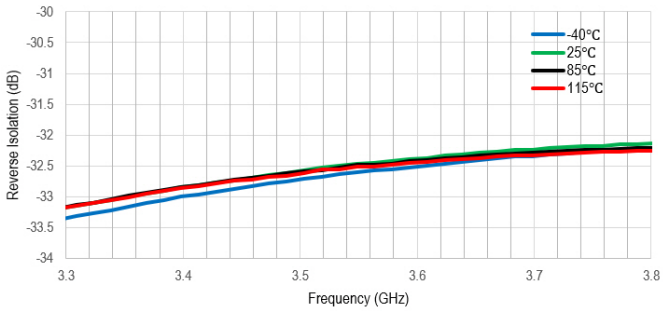


Figure 21. Reverse Isolation (dB) vs Frequency (GHz)

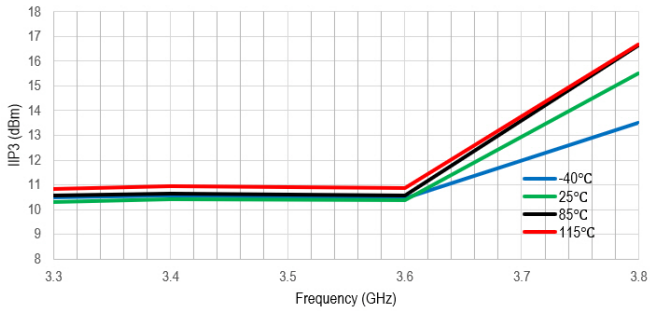


Figure 22. IIP3 (dBm) vs Frequency (GHz)

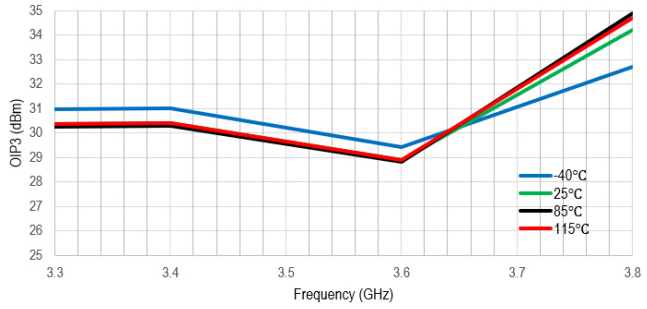


Figure 23. OIP3 (dBm) vs Frequency (GHz)

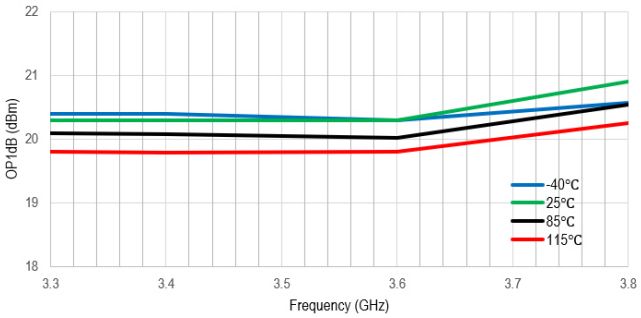


Figure 24. OP1dB (dBm) vs Frequency (GHz)

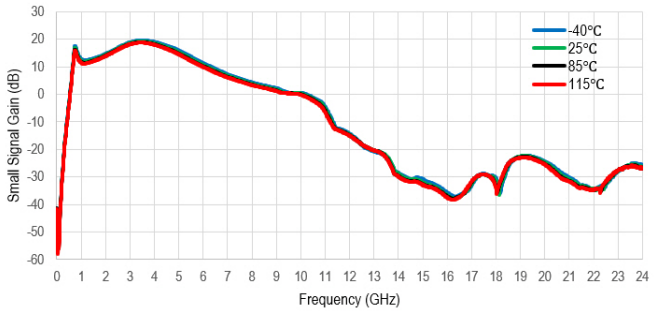


Figure 25. Small Signal Gain (dB) vs Frequency (GHz)

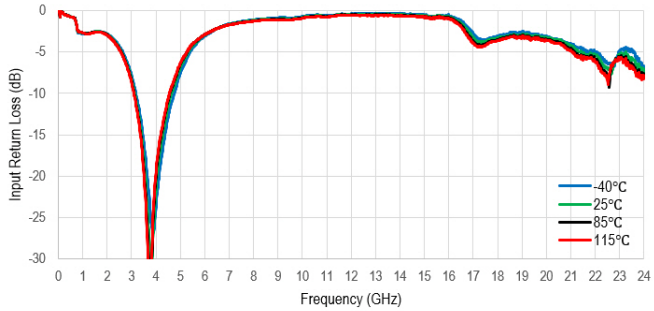


Figure 26. Input Return Loss (dB) vs Frequency (GHz)

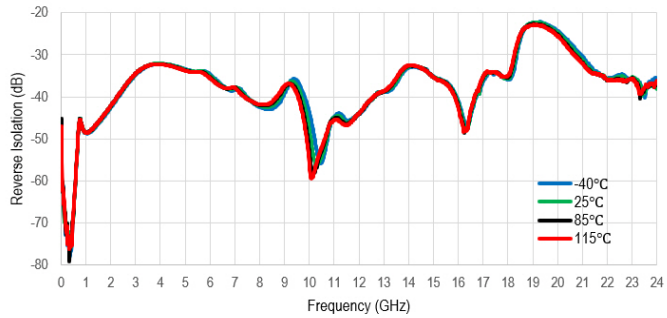


Figure 27. Reverse Isolation (dB) vs Frequency (GHz)

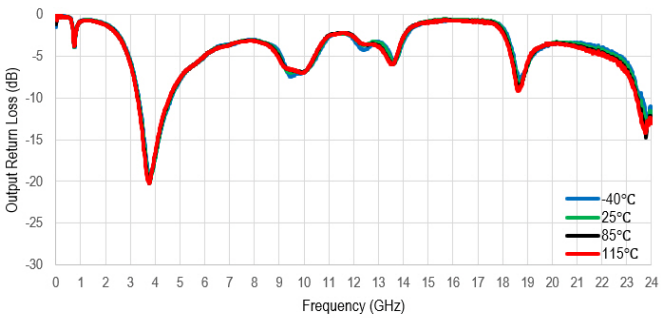


Figure 28. Output Return Loss (dB) vs Frequency (GHz)

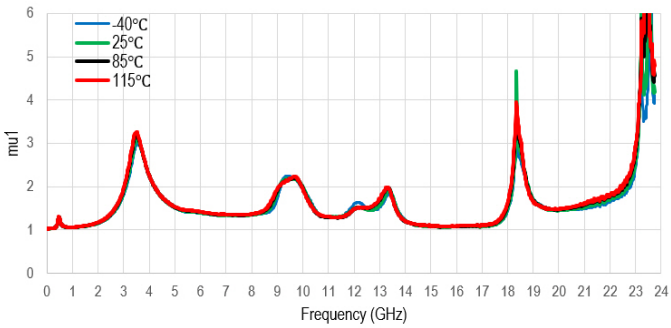


Figure 29. Stability Factor, µ1 (dB) vs Frequency (GHz)

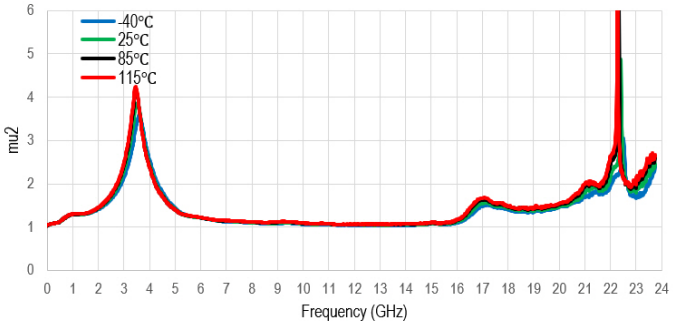


Figure 30. Stability Factor, µ2 (dB) vs Frequency (GHz)

Table 7. SKY67183-396LF Electrical Specifications: 2300 to 2700 MHz Optimized BoM in Table 10[1]
(V_{DD} = 5.0 V, Enable = GND, T_A = +25 °C, P_{IN} = -20 dBm, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
RF Specifications						
Noise figure	NF	@ 2300 MHz @ 2500 MHz @ 2700 MHz		0.36 0.41 0.43	0.75 0.75 0.85	dB dB dB
Gain	|S21|	@ 2300 MHz @ 2500 MHz @ 2700 MHz	20 20 19	21.7 21.4 20.9		dB dB dB
Input return loss	|S11|	@ 2300 MHz @ 2500 MHz @ 2700 MHz	9 10 10	13 16.4 18.7		dB dB dB
Output return loss	|S22|	@ 2300 MHz @ 2500 MHz @ 2700 MHz	7 9 9	11.2 13.5 12.6		dB dB dB
Reverse isolation	|S12|	@ 2300 MHz @ 2500 MHz @ 2700 MHz		33.8 33.4 33.2		dB dB dB
Third order output intercept point	OIP3	P_{IN} = -20 dBm, Δ Tone = 1 MHz: @ 2300 MHz @ 2500 MHz @ 2700 MHz	 29 29 29	 +32.2 +32.7 +33.4		 dBm dBm dBm
1 dB output compression point	OP1dB	@ 2300 MHz @ 2500 MHz @ 2700 MHz	18 20 20	+19.5 +22 +22.1		dBm dBm dBm
DC Specifications						
Supply voltage	V_{DD}			5.0		V
Quiescent current	I_{DD}			56		mA
Settling time 0.3 dB[2] Settling time 0.1 dB[3]	T_{S1} T_{S2}	@ 2500 MHz		0.3 0.33		us us

[1] Verified by characterization.

[2] Settling time 0.3 dB is measured from the time the LNA enable reaches 50% of LNA enable “on” level to the time at which the RF output power achieves within 0.3 dB of the average steady-state “on” level.

[3] Settling time 0.1 dB is measured from the time the LNA enable reaches 50% of LNA enable "on" level to the time at which the RF output power achieves within 0.1 dB of the average steady-state “on” level.

Typical Performance Characteristics

2300 to 2700 MHz, (VDD = 5 V, TA = +25 °C, PIN = -20 dBm, Characteristic Impedance (Zo) = 50 Ω, Unless Otherwise Noted)

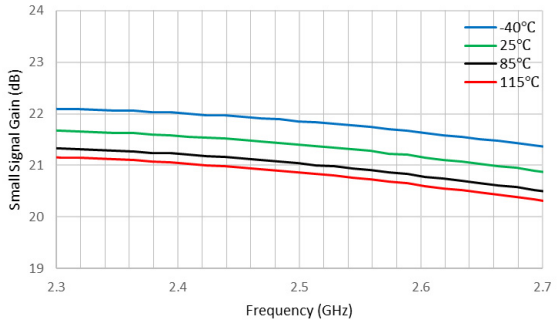


Figure 31. Small Signal Gain (dB) vs Frequency (GHz)

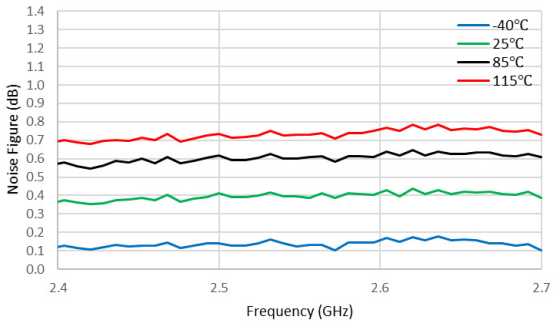


Figure 32. Noise Figure (dB) vs Frequency (GHz)

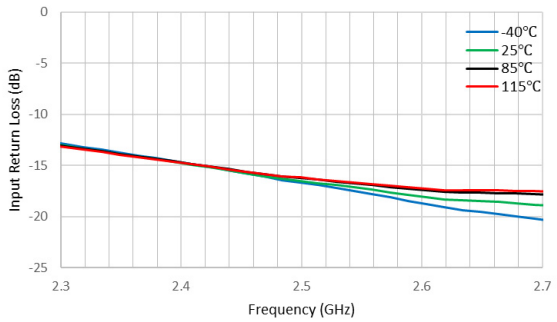


Figure 33. Input Return Loss (dB) vs Frequency

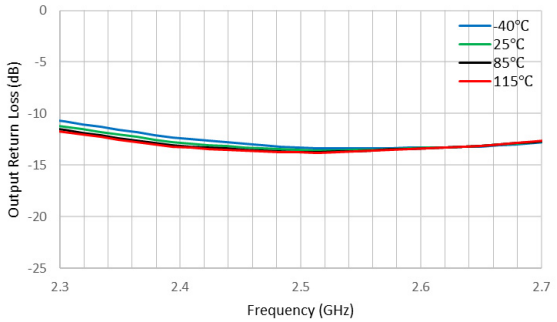


Figure 34. Output Return Loss (dB) vs Frequency

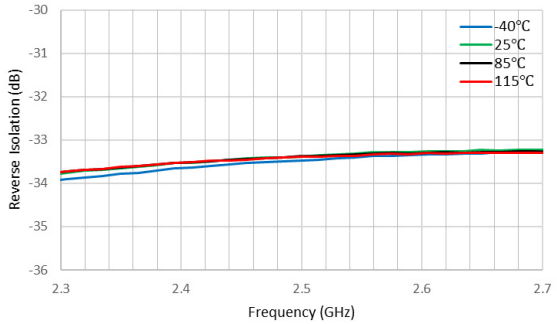


Figure 35. Reverse Isolation (dB) vs Frequency (GHz)

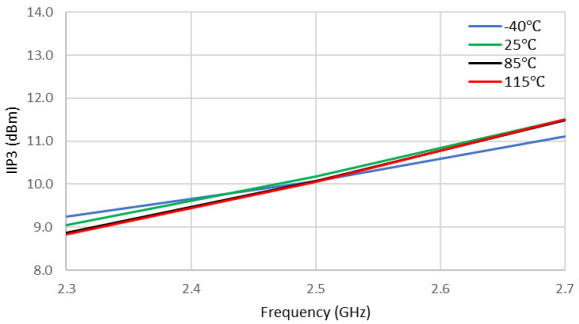


Figure 36. IIP3 (dBm) vs Frequency (GHz)

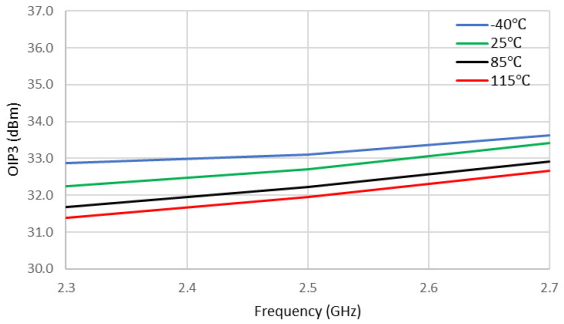


Figure 37. OIP3 (dBm) vs Frequency (GHz)

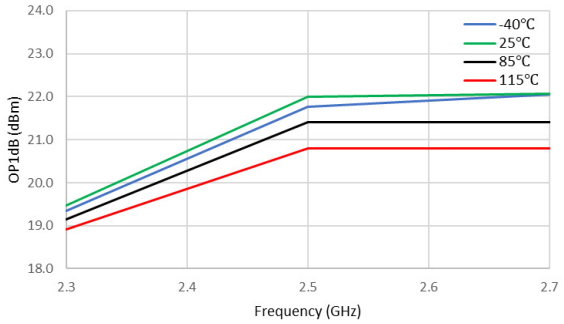


Figure 38. OP1dB (dBm) vs Frequency (GHz)

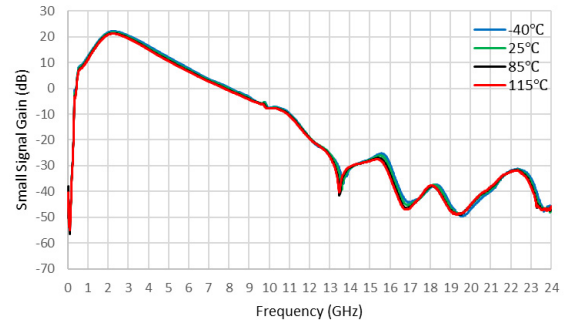


Figure 39. Small Signal Gain (dB) vs Frequency (GHz)

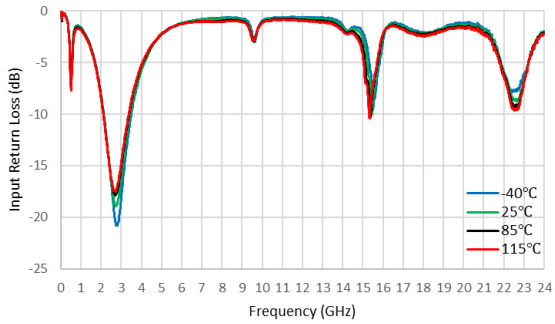


Figure 40. Input Return Loss (dB) vs Frequency (GHz)

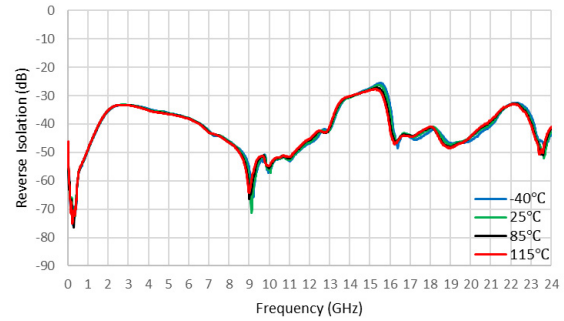


Figure 41. Reverse Isolation (dB) vs Frequency (GHz)

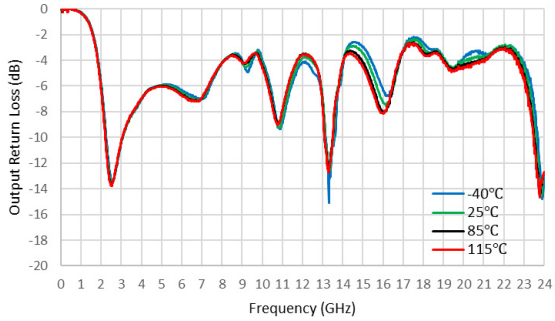


Figure 42. Output Return Loss (dB) vs Frequency (GHz)

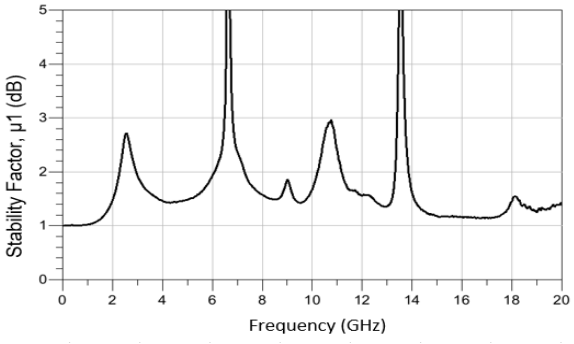


Figure 43. Stability Factor, µ1 (dB) vs Frequency (GHz) at -40 °C

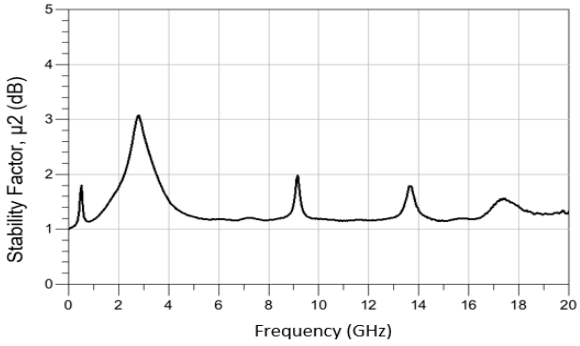


Figure 44. Stability Factor, µ2 (dB) vs Frequency (GHz) at -40 °C

Table 8. SKY67183-396LF Electrical Specifications: 1700 to 2200 MHz Optimized BOM in Table 10[1]
(VDD = 5.0 V, Enable = GND, TA = +25 °C, PIN = -20 dBm, Characteristic Impedance [Z0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
RF Specifications						
Noise figure	NF	@ 1700 MHz @ 1950 MHz @ 2200 MHz		0.34 0.38 0.41	0.75 0.75 0.85	dB dB dB
Gain	|S21|	@ 1700 MHz @ 1950 MHz @ 2200 MHz	21.5 21 19.5	23.2 22.7 21.5		dB dB dB
Input return loss	|S11|	@ 1700 MHz @ 1950 MHz @ 2200 MHz	10 10 10	15.7 26.2 14.8		dB dB dB
Output return loss	|S22|	@ 1700 MHz @ 1950 MHz @ 2200 MHz	7 10 10	9.7 25.2 20.6		dB dB dB
Reverse isolation	|S12|	@ 1700 MHz @ 1950 MHz @ 2200 MHz		34.4 34.2 34.6		dB dB dB
Third order output intercept point	OIP3	PIN = -20 dBm, Δ Tone = 1 MHz: @ 1700 MHz @ 1950 MHz @ 2200 MHz	 28 28 28	 +31.8 +32.2 +32.5		 dBm dBm dBm
1 dB output compression point	OP1dB	@ 1700 MHz @ 1950 MHz @ 2200 MHz	17.5 18.0 19.0	+19.1 +20.2 +21.1		dBm dBm dBm
DC Specifications						
Supply voltage	V_{DD}			5		V
Quiescent current	I_{DD}			56		mA
Settling time 0.3 dB[2] Settling time 0.1 dB[3]	T_{S1} T_{S2}	@ 1950 MHz		0.3 0.33		us us

[1] Verified by characterization.

[2] Settling time 0.3 dB is measured from the time the LNA enable reaches 50% of LNA enable “on” level to the time at which the RF output power achieves within 0.3 dB of the average steady-state “on” level.

[3] Settling time 0.1 dB is measured from the time the LNA enable reaches 50% of LNA enable "on" level to the time at which the RF output power achieves within 0.1 dB of the average steady-state “on” level.

Typical Performance Characteristics
1700 to 2200 MHz (VDD = 5 V, PIN = -20 dBm, Characteristic Impedance [Zo] = 50 Ω, Unless Otherwise Noted

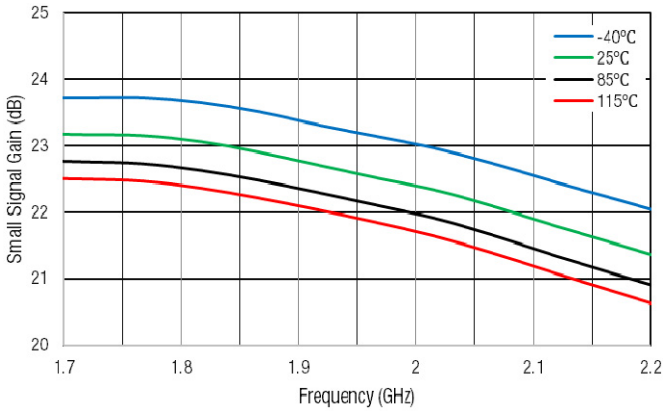


Figure 45. Small Signal Gain (dB) vs Frequency (GHz)

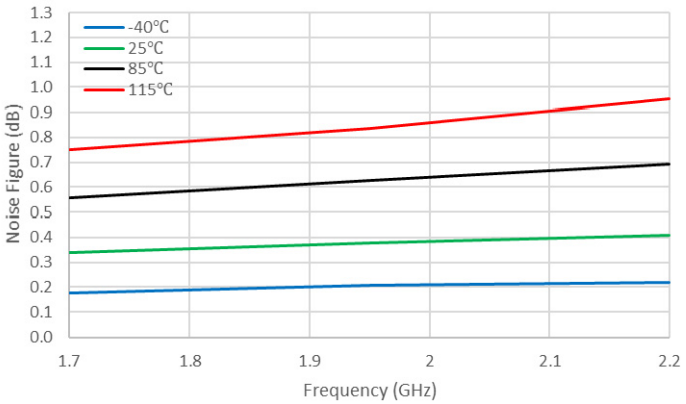


Figure 46. Noise Figure (dB) vs Frequency (GHz)

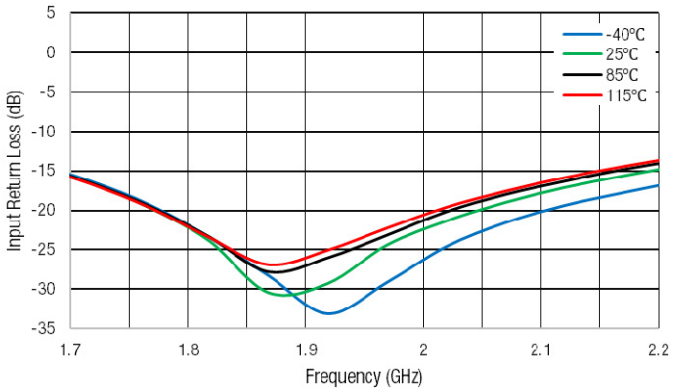


Figure 47. Input Return Loss (dB) vs Frequency

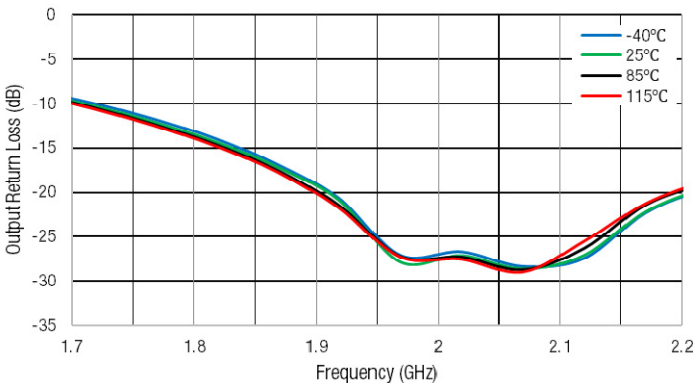


Figure 48. Output Return Loss (dB) vs Frequency

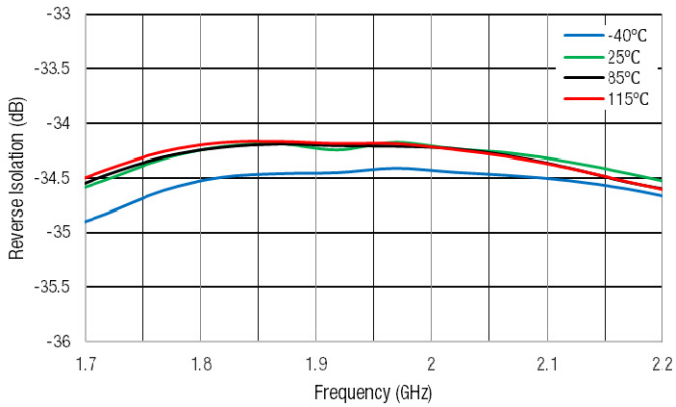


Figure 49. Reverse Isolation (dB) vs Frequency (GHz)

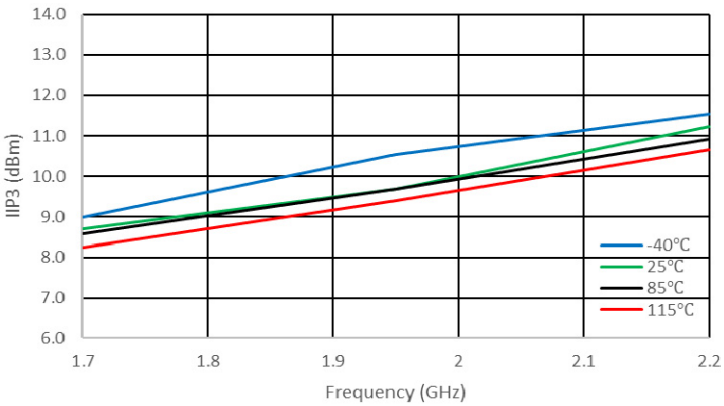


Figure 50. IIP3 (dBm) vs Frequency (GHz)

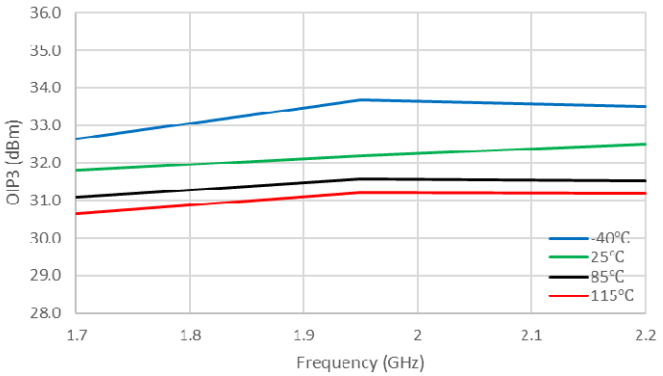


Figure 51. OIP3 (dBm) vs Frequency (GHz)

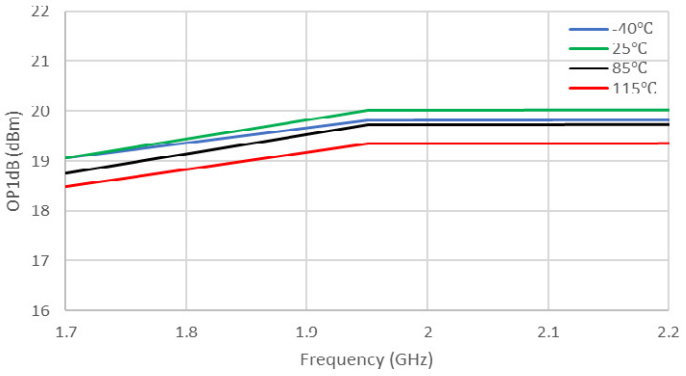


Figure 52. OP1dB (dBm) vs Frequency (GHz)

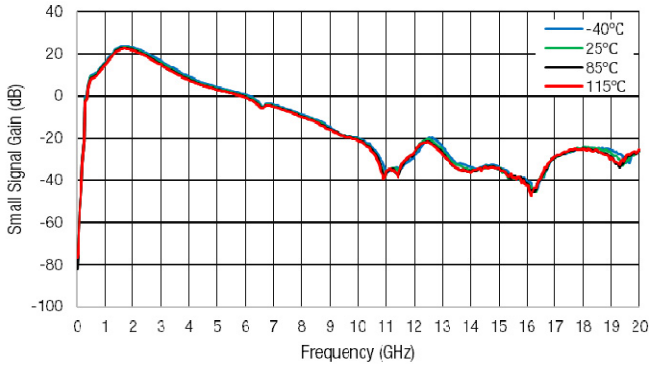


Figure 53. Small Signal Gain (dB) vs Frequency (GHz)

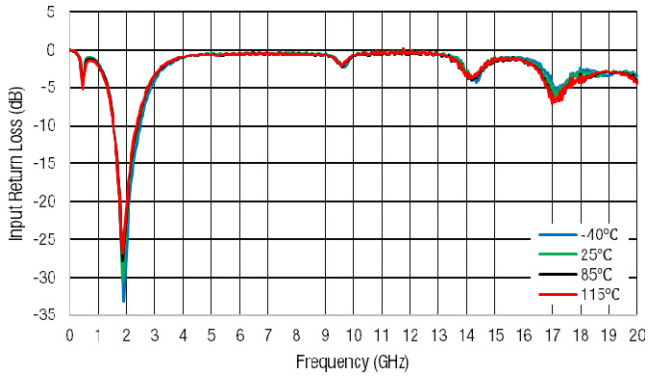


Figure 54. Input Return Loss (dB) vs Frequency (GHz)

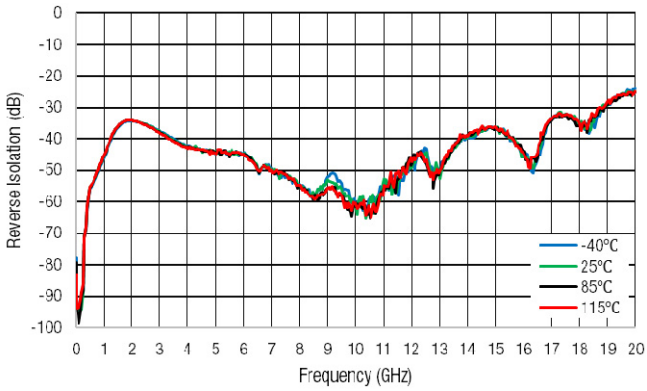


Figure 55. Reverse Isolation (dB) vs Frequency (GHz)

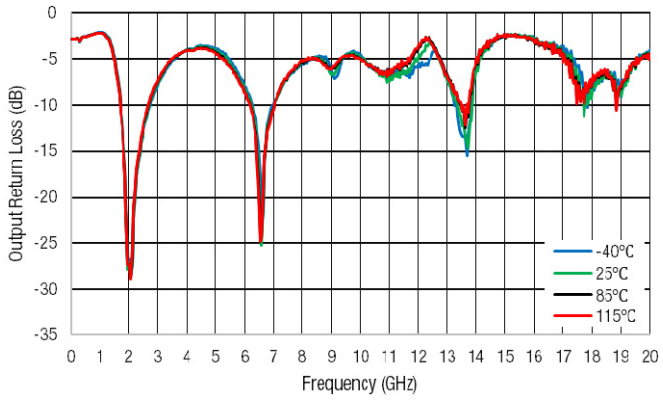


Figure 56. Output Return Loss (dB) vs Frequency (GHz)

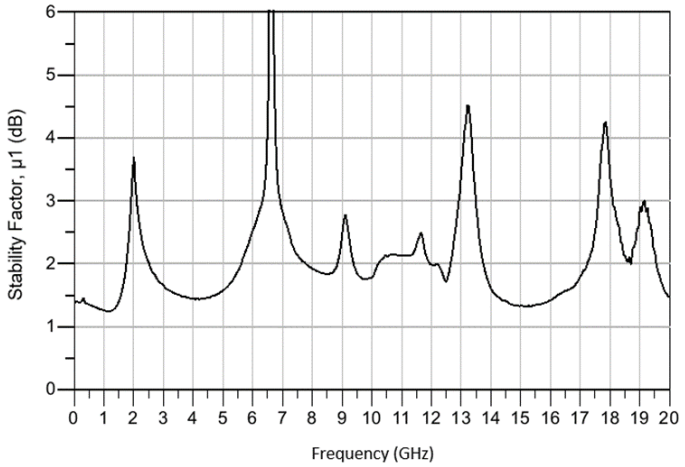


Figure 57. Stability Factor, µ1 (dB) vs Frequency (GHz) at -40 °C

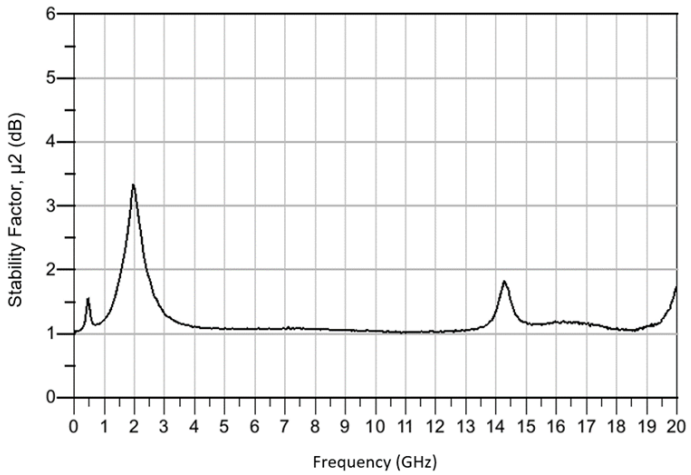
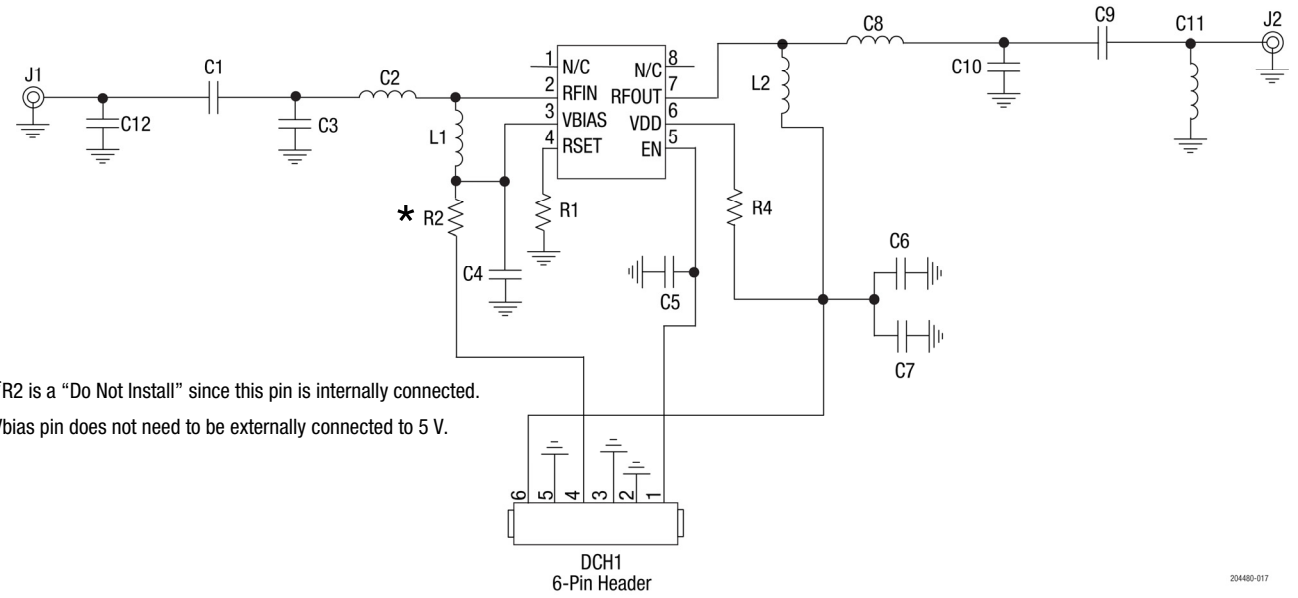


Figure 58. Stability Factor, µ2 (dB) vs Frequency (GHz) at -40 °C

Evaluation Board Description

The SKY67183-396LF Evaluation Board is used to test the performance of the SKY67183-396LF LNA. An Evaluation Board schematic diagram is shown below. Bill of Materials (BOMs) for Evaluation Boards optimized for 4200 to 4900 MHz, 3300 to 3800, 2300 to 2700 MHz, and 1700 to 2200 MHz appear in the following pages. An EVB assembly diagram and layer details are also included in this data sheet.



*R2 is a "Do Not Install" since this pin is internally connected.

Vbias pin does not need to be externally connected to 5 V.

Figure 59. SKY67183-396LF Evaluation Board Schematic

Table 9. SKY67183-396 Evaluation Board Bill of Materials (BOM) for 4200 to 4900 MHz Tuning

Component	Value	Size	Part Number
C1	1.8 pF	0402	GJM1555C1H1R8BB01D
C2	0.8 nH	03015	LQW04AN0N8C00D
C3	0.4 pF	0402	GJM1555C1HR40WB01D
C4	DNI		
C5	DNI		
C6	DNI		
C7	4.7 uF	0402	GRM155C80J475MEAAD
C8	2.2 pF	0402	GRM1555C1H2R2BA01D
C9	0 Ω	0402	Not critical
C10	1.0 nH	0402	LQG15HS1N0S02D
C11	DNI		
C12	DNI		
L1	18 nH	0402	LQW15AN18NG8ZD
L2	6.2 nH	0402	LQG15HS6N2S02D
R1	8.2 kΩ	0201	Not critical
R2	DNI		
R4	100 Ω	0201	Not critical

Table 10. SKY67183-396LF Evaluation Board Bill of Materials (BOM) for 3300 to 3800 MHz Tuning

Component	Value	Size	Part Number
C1	1.8 pF	0402	GJM1555C1H1R8BB01
C2	1.8 nH	0402	LQW15AN1N8C00
C3	0.4 pF	0402	GJM1555C1HR40WB01D
C4	DNI		
C5	DNI		
C6	DNI		
C7	4.7 uF	0402	GRM155C80J475MEAAD
C8	5.6 pF	0402	GRM1555C1H5R6BA01D
C9	0 Ω	0402	Not critical
C10	1.8 nH	0402	LQG15HS1N8S02D
C11	DNI		
C12	DNI		
L1	12 nH	0402	LQW15AN12NG8ZD
L2	5.6 nH	0402	LQG15HS5N6S02D
R1	8.2 kΩ	0201	Not critical
R2	DNI		
R4	100 Ω	0201	Not critical

Table 11. SKY67183-396LF Evaluation Board Bill of Materials (BOM) for 2300 to 2700 MHz Tuning

Component	Value	Size	Part Number
C1	5.0 pF	0402	GJM1555C1H5R0BB01D
C2	2.7 nH	0402	LQW15AN2N7B8ZD
C3	0.4 pF	0402	GJM1555C1HR40WB01D
C4	10 pF	0402	GRM1555C1H100JA01D
C5	DNI		
C6	DNI		
C7	4.7 uF	0402	GRM155C80J475MEAAD
C8	22 pF	0402	GRM1555C1H220JA01
C9	1.8 pF	0402	GRM1555C1H1R8BA01D
C10	3.3 nH	0402	LQG15HS3N3S02D
C11	DNI		
C12	DNI		
L1	22 nH	0402	LQW15AN22NG8ZD
L2	5.6 nH	0402	LQG15HS5N6S02D
R1	8.2 kΩ	0201	Not critical
R2	DNI		
R4	100 Ω	0201	Not critical

Table 12. SKY67183-396LF Evaluation Board Bill of Materials (BOM) for 1700 to 2200 MHz Tuning

Component	Value	Size	Part Number
C1	5.0 pF	0402	GJM1555C1H5R0BB01D
C2	4.7 nH	0402	LQW15AN4N7B8ZD
C3	0.4 pF	0402	GJM1555C1HR40WB01D
C4	15 pF	0402	GRM1555C1H150JA01D
C5	DNI		
C6	DNI		
C7	4.7 uF	0402	GRM155C80J475MEAAD
C8	22 pF	0402	GRM1555C1H220JA01
C9	1.8 pF	0402	GRM1555C1H1R8BA01D
C10	6.2 nH	0402	LQG15HS6N2S02D
C11	300 Ohm	0402	ERJ-2RKF3000C
C12	DNI		
L1	22 nH	0402	LQW15AN22NG8ZD
L2	5.6 nH	0402	LQG15HS5N6S02D
R1	8.2 KOhm	0201	ERJ-1GNF8201C
R2	DNI		
R4	100 Ohm	0201	ERJ-1GNF1000C

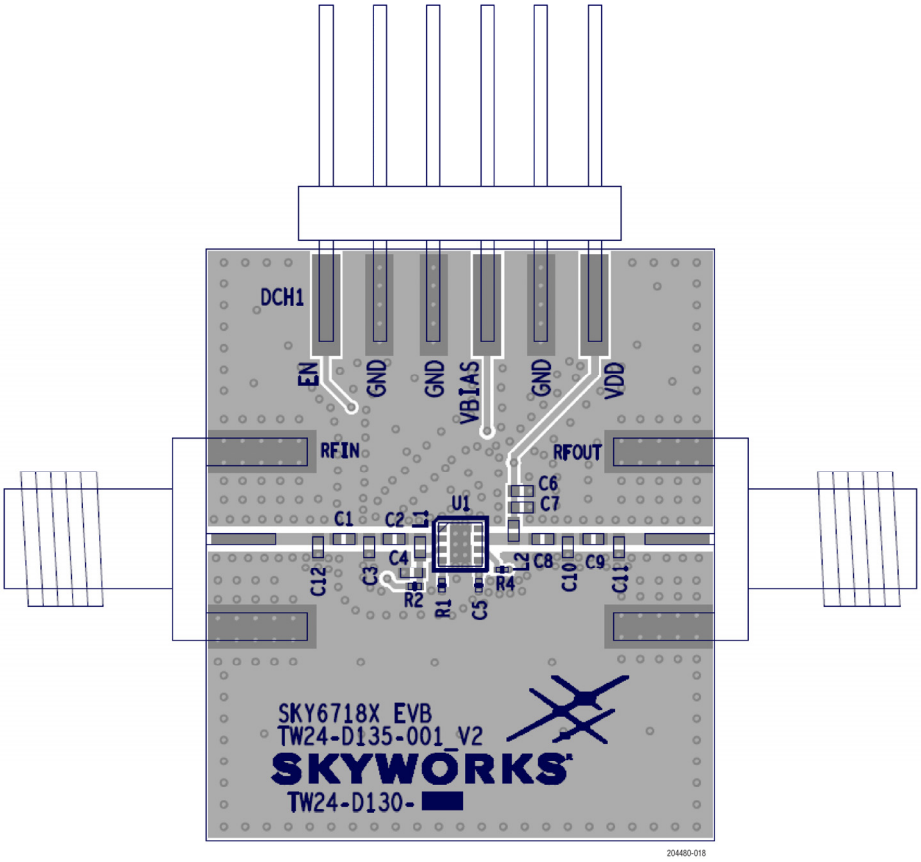


Figure 60. SKY67183-396LF EVB Assembly Diagram

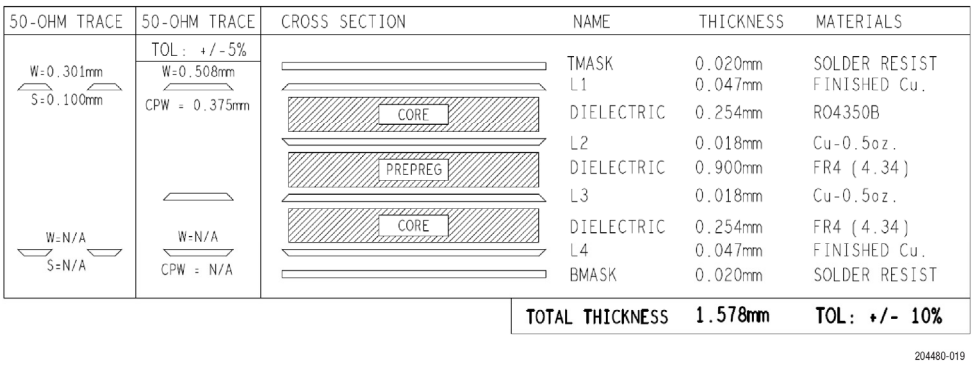


Figure 61. SKY67183-396LF EVB Layer Details

Package Dimensions

Typical part marking and PCB layout footprint for the SKY67183-396LF appear below, followed by package and tape and reel dimensions.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY67183-396LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

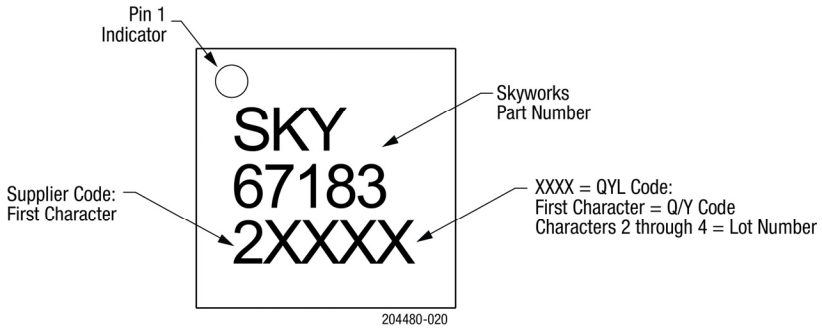


Figure 62. SKY67183-396LF Typical Part Marking

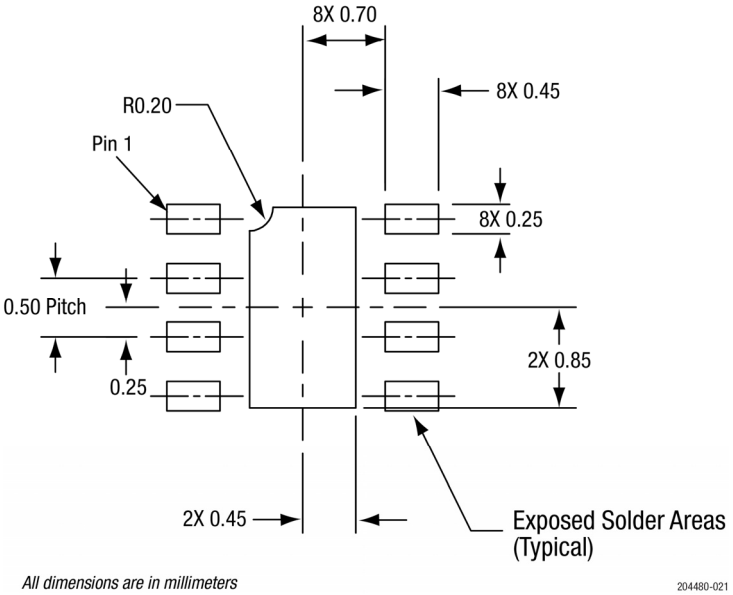
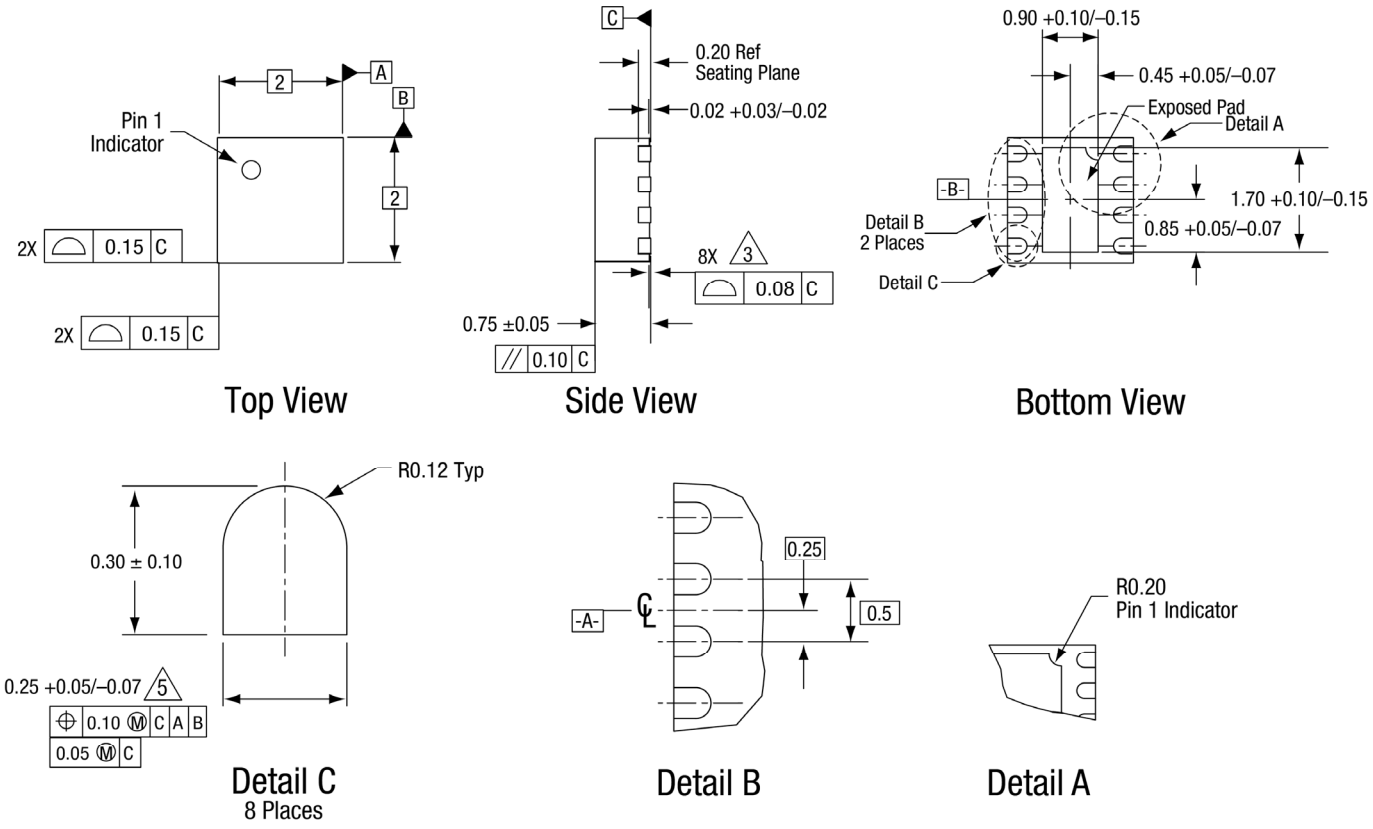


Figure 63. SKY67183-396LF PCB Layout Footprint

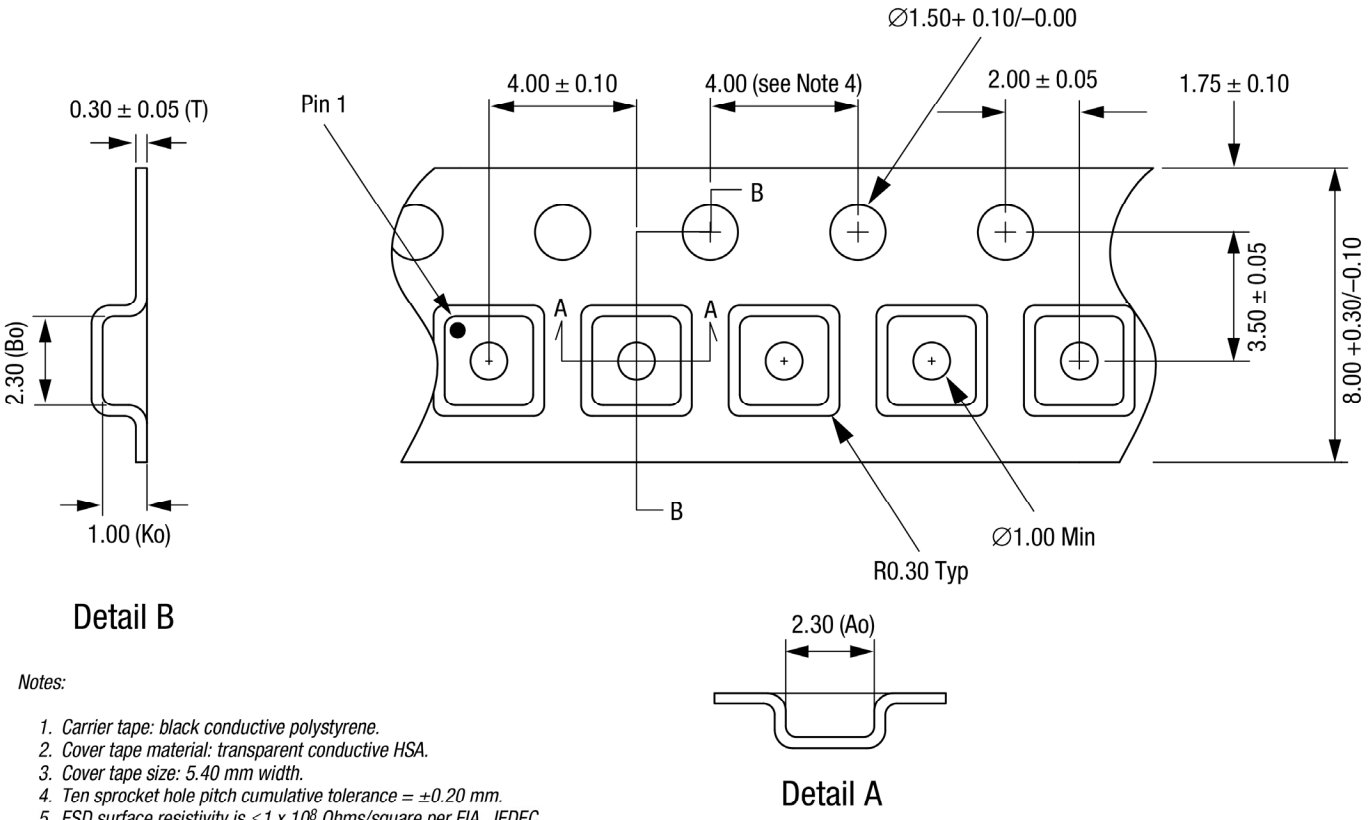


Notes:

1. *All measurements are in millimeters.*
2. *Dimensions and tolerances according to ASME Y14.5M-1994.*
3. *Coplanarity applies to the exposed heat sink ground pad as well as the terminals.*
4. *Plating requirement per source control drawing (SCD) 2504.*
5. *Dimension applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.*

204480-022

Figure 64. SKY67183-396LF Package Dimensions



Notes:

1. *Carrier tape: black conductive polystyrene.*
2. *Cover tape material: transparent conductive HSA.*
3. *Cover tape size: 5.40 mm width.*
4. *Ten sprocket hole pitch cumulative tolerance = ±0.20 mm.*
5. *ESD surface resistivity is ≤1 x 10^8 Ohms/square per EIA, JEDEC tape and reel specification.*
6. *Ao and Bo measurement point to be 0.30 mm from bottom pocket.*
7. *All measurements are in millimeters.*

Figure 65. SKY67183-396LF Tape and Reel Dimensions