DATA SHEET

SKY85712-21: 5 GHz WLAN Front-End Module

Applications

- 802.11ac networking and personal computing systems
- PC cards, PCMCIA cards, mini-cards, and half mini-cards
- WLAN-enabled wireless video systems

Features

- Integrated high-performance 5 GHz PA, LNA with bypass, and T/R switch
- Fully-matched input and output
- Integrated power detector and directional coupler
- Transmit gain: 27 dB
- Receive gain: 12 dB
- Output power: +19 dBm @ 1.8% EVM, HT80, MCS9, 5 V/4.2 V
- Output power: +20 dBm @ 3% EVM, HT40, MCS7, 5 V/4.2 V
- Small QFN (16-pin, 3 x 3 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

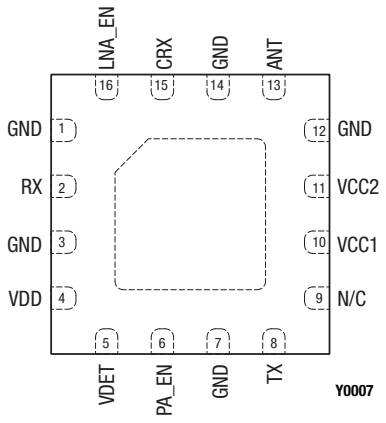


Figure 2. SKY85712-21 Pinout (Top View)

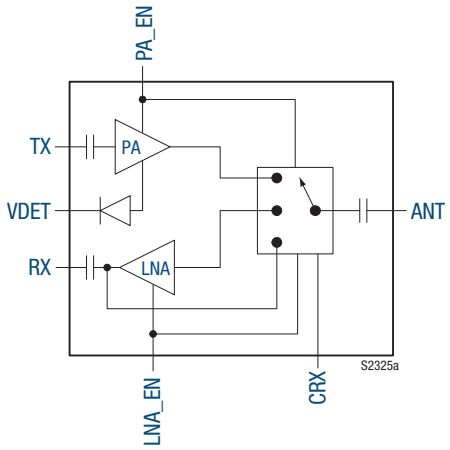


Figure 1. SKY85712-21 Block Diagram

Description

The SKY85712-21 is a highly integrated, 5 GHz front-end module (FEM) incorporating a 5 GHz single-pole, double-throw (SPDT) transmit/receive (T/R) switch, a 5 GHz low-noise amplifier (LNA) with bypass, and a 5 GHz power amplifier (PA) intended for mobile/portable 802.11ac applications and systems.

The LNA and PA disable functions ensure low leakage current in off mode. An integrated power detector is included to provide closed-loop power control within the system.

The device is provided in a compact, 16-pin 3 x 3 mm Quad Flat No-Lead (QFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

Table 1. SKY85712-21 Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	GND	Ground	9	N/C	No connection
2	RX	RF receive output	10	VCC1	PA supply voltage
3	GND	Ground	11	VCC2	PA supply voltage
4	VDD	LNA supply voltage	12	GND	Ground
5	VDET	Detector output voltage	13	ANT	Antenna
6	PA_EN	PA enable	14	GND	Ground
7	GND	Ground	15	CRX	Switch control voltage
8	TX	RF transmit input	16	LNA_EN	LNA enable

Technical Description

The SKY85712-21 is comprised of a high-performance 5 GHz PA, 5 GHz LNA, and broadband SPDT switch. The device is fully-matched, and requires few external components for optimal performance, which makes it ideal for small portable/mobile applications. The FEM provides up to +27 dB of gain over the frequency band. The LNA supports an enable/disable mode for power savings when not in receive mode and a bypass function for increased receive dynamic range. The PA can be shut off using the PA_EN signal (pin 6).

The low-loss broadband switch provides the T/R switching function on the SKY85712-21 and has a 1 dB Output Compression Point (OP1dB) of approximately +25 dBm.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY85712-21 are provided in Table 2. The recommended operating conditions are specified in Table 3, and electrical specifications are provided in Table 4.

The state of the SKY85712-21 is determined by the logic provided in Table 5.

Table 2. SKY85712-21 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V_{CC1}, V_{CC2}	–0.3	+6.0	V
Supply voltage	V_{DD}		+6.0	V
DC input on control pins (PA_EN, LNA_EN, CRX)	V_{IN}	–0.3	+3.6	V
Input power (50 Ω load)	P_{IN}		+10	dBm
Supply current	I_{CC}		400	mA
Storage temperature	T_{ST}	–40	+150	°C
Junction temperature	T_J		170	°C
Electrostatic discharge: Human Body Model (HBM), Class 1C			 1000	 V

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. SKY85712-21 Recommended Operating Conditions (Note 1)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	V_{CC1}, V_{CC2}, V_{DD}	3.9	5.0	5.5	V
Control logic: High Low	 V_{IH} V_{IL}	 2.5 0		 3.6 0.4	 V V
Operating temperature	T_{OP}	–40		+85	°C

Note 1: During production test, devices will be tested at 5 V.

Table 4. SKY85712-21 Electrical Specifications (1 of 2) (V_{CC} = V_{DD} = 5 V, Unless Otherwise Specified, T_{OP} = 25 °C, Unless Otherwise Noted) (Note 1)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency range	f	Main frequency band	5.15		5.85	GHz
Transmit Mode						
Gain	G		24	27	31	dB
Gain flatness		Over any 40 MHz bandwidth	–0.5		+0.5	dB
Output power	P_{OUT}	With –45 dB EVM source, V_{CC} = 5.0 V:				
		MCS9, HT80, 1.8 % DEVM, AT off	+17	+19		dBm
		MCS7, HT40, 3 % DEVM, AT off	+18	+20		dBm
		MCS0, mask compliance	+21	+24		dBm
		With –45 dB EVM source, V_{CC} = 4.2 V:				
		MCS9, HT80, 1.8 % DEVM, AT off		+19		dBm
		MCS7, HT40, 3 % DEVM, AT off		+20		dBm
		MCS0, mask compliance		+24		dBm
Current consumption	I_{TOT}	Modulated signal:				
		Idle current, VEN = 0		20	35	µA
		@ Quiescent		230		mA
		@ +19 dBm		275		mA
		@ +20 dBm		300		mA
		@ +22 dBm		330		mA
2nd and 3rd harmonics	2fo, 3fo	+22 dBm MCS0			–50	dBm/MHz
All spurious		+22 dBm OFDM, 6 Mbps		–28	–25	dBm
Isolation		From ANT to either TX or RX pin		40		dB
Input return loss	|S11|		7	10		dB
Output return loss	|S22|		10	12		dB
Power detector output:						
V_{CC1} = V_{CC2} = V_{DD} = 5.0 V:						
@ No RF				0.30		V
@ +19 dBm				0.75		V
@ +23 dBm				1.05		V
V_{CC1} = V_{CC2} = V_{DD} = 4.2 V:						
@ No RF				0.3		V
@ +19 dBm				0.7		V
@ +23 dBm				1.0		V
Power detector output impedance	Z_{OUT_DET}	RF output = –30 dBm		700		Ω
PA enable current	I_{ENABLE}			0.5		mA
Ruggedness	RU	Maximum input power at which PA can survive 10:1 mismatch with no permanent damage.			+10	dBm

Table 4. SKY85712-21 Electrical Specifications (2 of 2) (V_{CC} = V_{DD} = 5 V Unless Otherwise Specified, T_{OP} = 25 °C, Unless Otherwise Noted) (Note 1)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Receive Mode						
Gain	G		9	12	16	dB
1 dB Input compression point	IP1dB	LNA active LNA bypass		–5 +10		dBm dBm
Gain step			19	21	23	dB
Gain flatness		Over any 40 MHz bandwidth	–0.25		+0.25	dB
Noise figure	NF			2.7	3.0	dB
Input return loss	|S11|	LNA active LNA bypass	6 10			dB dB
Output return loss	|S22|		5	8		dB
Third order input intercept point	IIP3			+8		dBm
Switching time	t_{SW}	LNA ↔ bypass RX ↔ TX: From 10% ↔ 90% power change of rising or falling edge, state 1			200 400	ns ns
LNA bias current	I_{DD}			11	15	mA
LNA enable current					10	µA
CRX enable current					10	µA
Idle current	I_{IDLE}	State 1			20	µA
Receive Bypass Mode						
Insertion loss	|S21|			–9		dB

Note 1: Performance is guaranteed only under the conditions listed in this table.

Table 5. SKY85712-21 Logic

Mode	State	CRX (J5, Pin 15)	LNA_EN (J5, Pin 16) (Note 1)	PA_EN (J5, Pin 6) (Note 2)
All off (switch in TX mode)	1	0	0	0
WLAN receive	2	1	1	0
WLAN receive bypass mode	3	1	0	0
WLAN transmit	4	0	0	1

Note 1: LNA is on while LNA_EN is high. LNA is off and in bypass mode when LNA_EN is low.

Note 2: PA_EN controls only the PA. It does not control the switch.

Evaluation Board Description

The SKY85712-21 Evaluation Board is used to test the performance of the SKY85712-21 FEM. A suggested application schematic diagram is shown in Figure 3. A photograph of the Evaluation Board is shown in Figure 4. Table 6 provides the Bill of Materials (BOM) list for Evaluation Board components.

Evaluation Board Setup Procedure

1. Connect system ground to pin 2 of the J4 header and to pin 2 of the J5 header.
2. Apply 5 V to pins 1 and 3 of the J4 header and to pin 3 of the J5 header.
3. Select a path according to the information in Table 5:
   L = 0 V
   H = 3.3 V
4. Connect a DMM to pin 12 of the J5 header to monitor the power detector voltage.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

- Paths to ground should be made as short as possible.
- The ground pad of the SKY85712-21 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Because the circuit board acts as the heat sink, it must shunt as much heat as possible from the device.

  Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

NOTE: *A poor connection between the ground pad and ground increases junction temperature (T_J), which reduces the life of the device.*

- Place component C7 close to pin 11.
- Place component C6 close to pin 10.
- The ANT port is DC-blocked and does not require a DC blocking capacitor.
- There is no DC present on the RX port. This pin needs to be DC-blocked with a general purpose 4.7 pF capacitor if there is > 2.6 V DC on the trace connecting to the RX port.
- There is no DC present on the TX port. This pin needs to be DC-blocked with a general purpose 4.7 pF capacitor if there is > 3.2 V DC on the trace connecting to the TX port.
- Each VCC pin needs to be individually decoupled as shown in the Evaluation Board schematic. Place C7 close to pin 11. Place C6 close to pin 10.
- VCC1 and VCC2 should not be shorted together at the device pins. Refer to the layout for details.
- The DNI components and 0 Ω resistors can be eliminated.
- The ANT and LNA OUT trace losses are 0.18 dB. The TX IN trace losses are 0.22 dB.

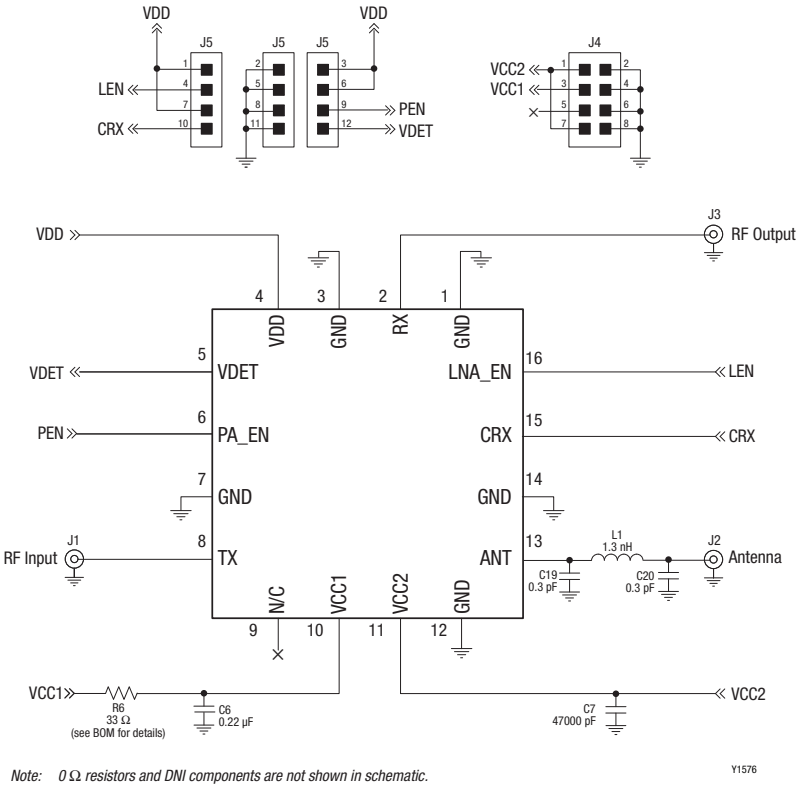


Figure 3. SKY85712-21 Application Schematic

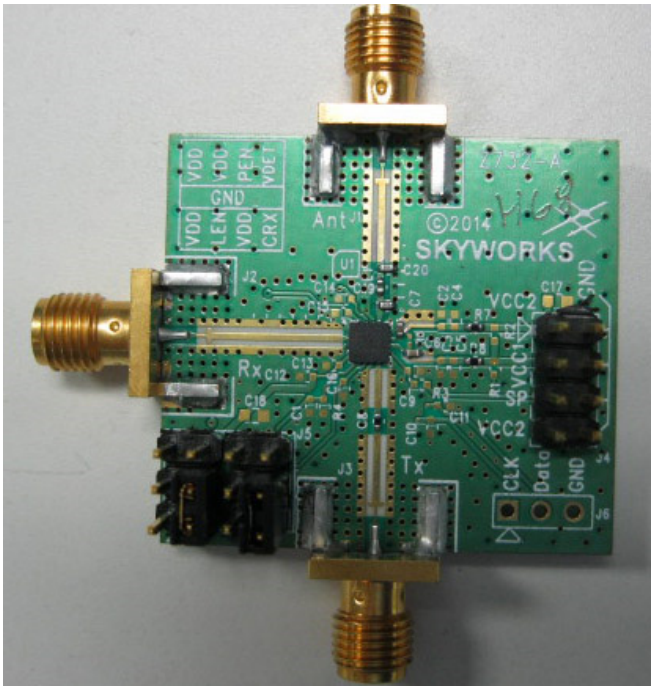


Figure 4. SKY85712-21 Evaluation Board

Table 6. SKY85712-21 Evaluation Board Bill of Materials

Component	Value	Size	Vendor	Mfr Part Number	Description
C6	0.22 µF	0402	Murata	GRM155R60J224KE01	Multilayer ceramic
C7	47000 pF	0402	Murata	GRM155R71E473KA88	Multilayer ceramic
R6	33 Ω when VCC = 5 V 0 Ω when VCC = ≤ 4.2 V	0402	Panasonic	ERJ2GEJ330	Thick film chip resistor
C19, C20	0.3 pF	0402	Murata	GJM1555C1HR30BB01	Multilayer ceramic
L1	1.3 nH	0402	Murata	LQG15HN1N3S02D	High-frequency multilayer

Note: 0 Ω resistors and DNI components are not shown in the Bill of Materials.

Package Dimensions

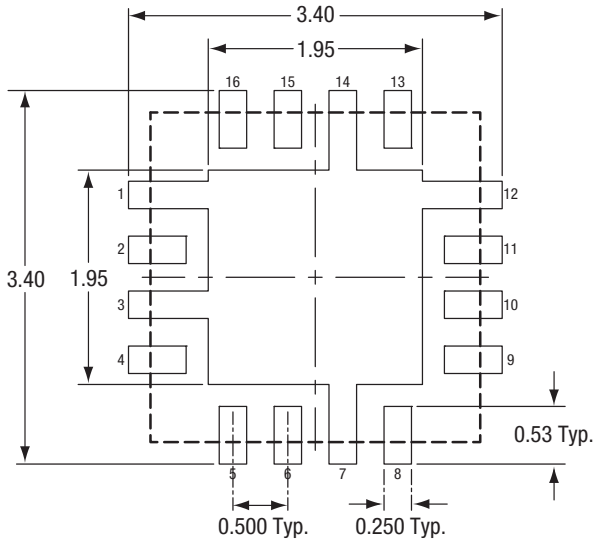
The PCB layout footprint for the SKY85712-21 is shown in Figure 5. Typical part markings are shown in Figure 6. Package dimensions for the 16-pin QFN are shown in Figure 7, and tape and reel dimensions are provided in Figure 8.

Package and Handling Information

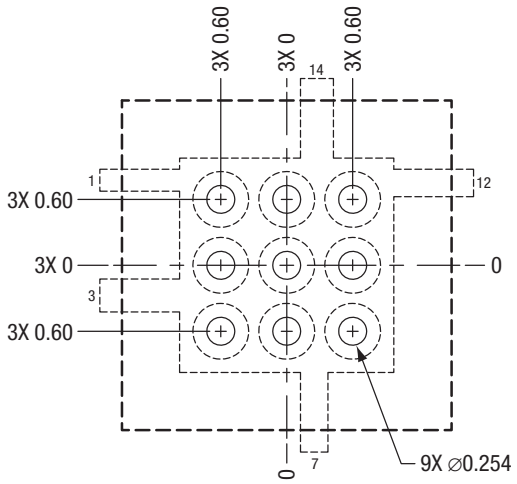
Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY85712-21 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

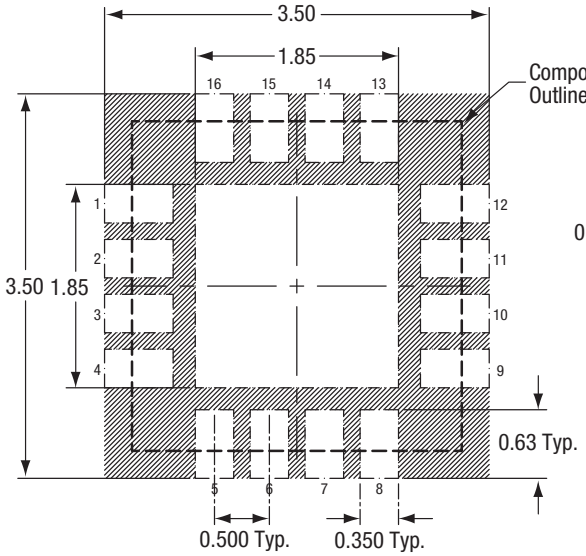
Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.



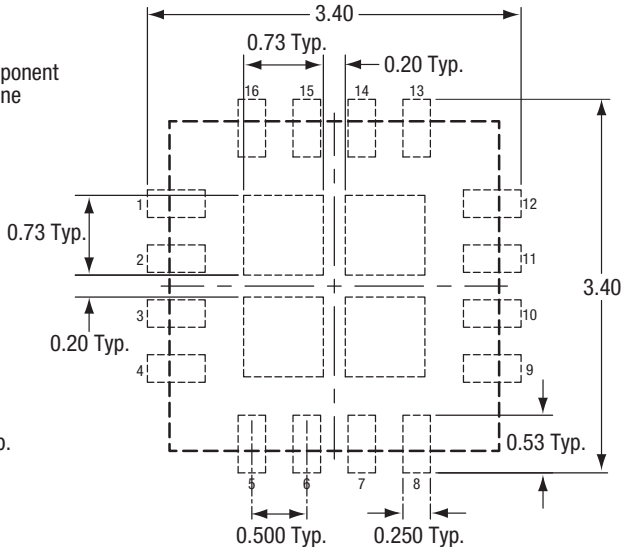
Board Metal



Via Pattern
(Note 1)



Solder Mask Pattern
(Note 2)



Stencil Pattern
(Note 3)
61% solder coverage
on center pad

Notes:

1. *Via hole recommendations:*
   0.025 mm Cu via wall plating (minimum), solder mask on the far side should tent or plug via holes.
2. *Solder mask recommendations:*
   Contact board fabricator for recommended solder mask offset and tolerance.
3. *Stencil recommendations:*
   0.125 mm stencil thickness, laser cut apertures, trapezoidal walls and rounded corners offer better paste release.
4. *Dimensions and tolerances according to ASME Y14.5M-1994.*
5. *Unless specified, dimensions are symmetrical about center lines.*
6. *All dimensions are in millimeters.*

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Figure 5. SKY85712-21 PCB Layout Footprint
(Top View)

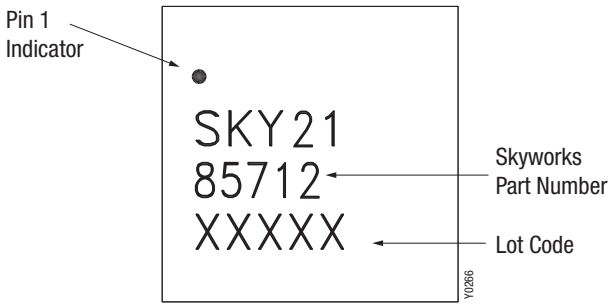
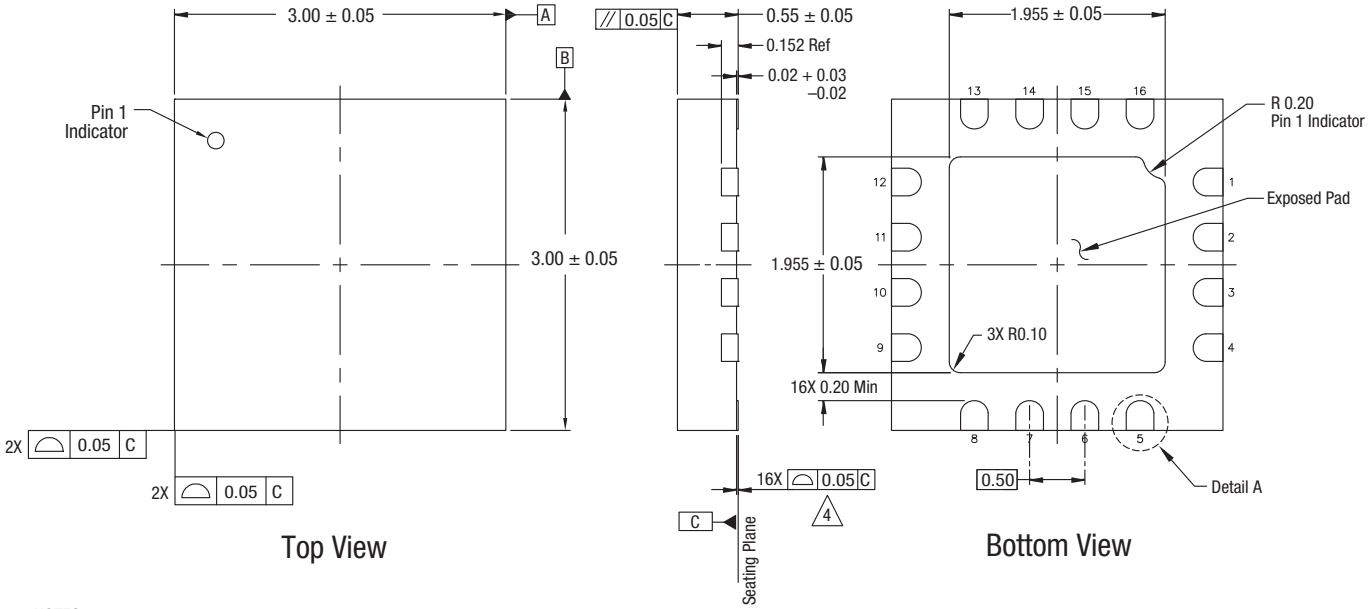


Figure 6. Typical Part Markings (Top View)



NOTES:

1. *All measurements are in millimeters.*
2. *Dimensioning and tolerancing according to ASME Y14.5M-1994.*
3. *Unless otherwise specified, the following values apply:*
   Decimal Tolerance: Angular Tolerance:
   X.X (1 place) ± 0.1 mm ± 0.5°
   X.XX (2 places) ± 0.05 mm
   X.XXX (3 places) ± 0.025 mm
4. *Coplanarity applies to the terminals as well as other bottom surface metallization.*
5. *Dimension applies to metallized terminal. If terminal tip has a radius, dimension should not be measured in that radius area.*
6. *Unless specified, dimensions are symmetrical about center lines.*

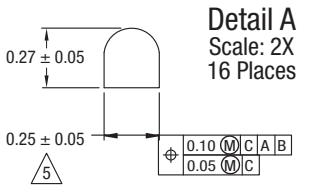


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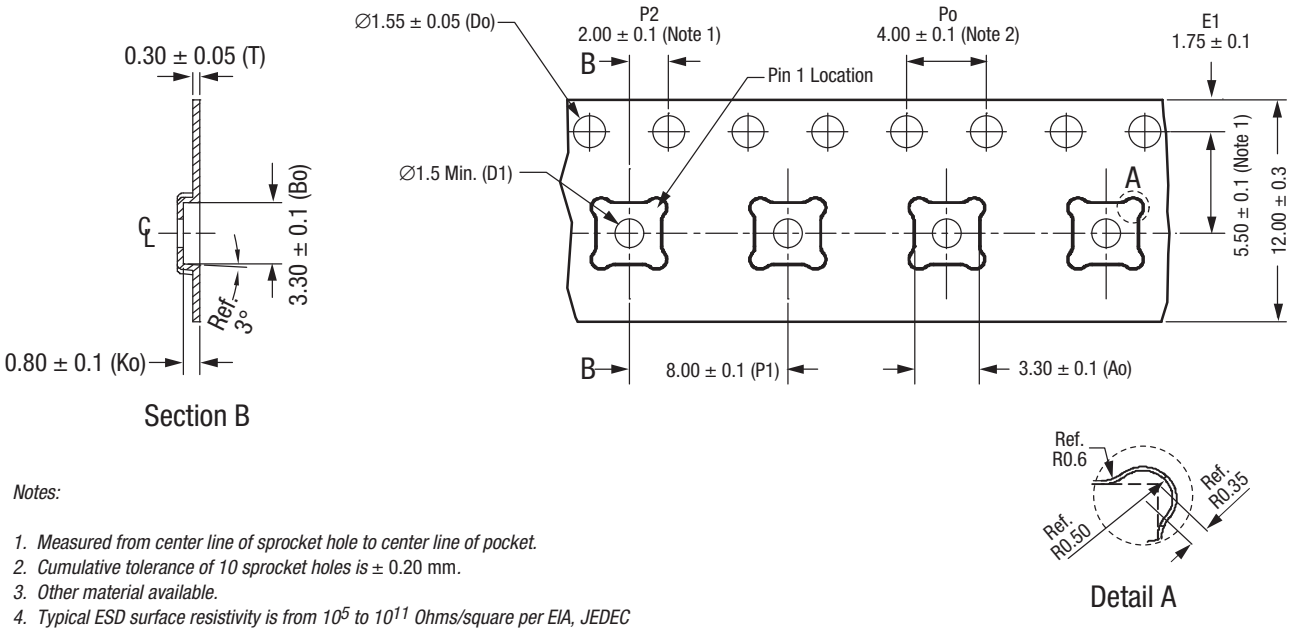
Figure 7. SKY85712-21 Package Dimensions



Notes:

1. *Measured from center line of sprocket hole to center line of pocket.*
2. *Cumulative tolerance of 10 sprocket holes is* ± 0.20 mm.
3. *Other material available.*
4. *Typical ESD surface resistivity is from 10^5 to 10^{11} Ohms/square per EIA, JEDEC tape and reel specification.*
5. *All measurements are in millimeters.*

Figure 8. SKY85712-21 Tape and Reel Dimensions