General Description

The SLG47512/13 provides a small, low voltage and low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, and the macrocells of the SLG47512/13. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

Key Features

- Two High Speed General Purpose Analog Comparators (ACMPxH)
- Integrated Voltage References (Vref)
- Fifteen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs or Shift Registers
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Ten Selectable DFF/LATCH or 3-bit LUTs or Shift Registers
  - One Selectable DFF/LATCH or 4-bit LUTs or Shift Register
- Eight Multi-Function Macrocells
  - Seven Selectable DFF/LATCH or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCH or 4-bit LUT + 16-bit Delay/Counter
- Serial Communications
  - I^2C Protocol Interface
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Two Oscillators (OSC)
  - 2.048 kHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor
- Power-On Reset (POR) with CRC Check
- Read Back Protection (Read Lock)
- Power Supply
  - $1.0\ V \le V_{DD} \le 1.65\ V$
- Operating Temperature Range: -40 °C to 85 °C
- RoHS Compliant/Halogen-Free
- Available Package
  - 12-pin STQFN: 1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm pitch
  - 16-pin MSTQFN: 1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm pitch

Applications

- Notebook and Tablet PCs
- Smartphones and Fitness Bands
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

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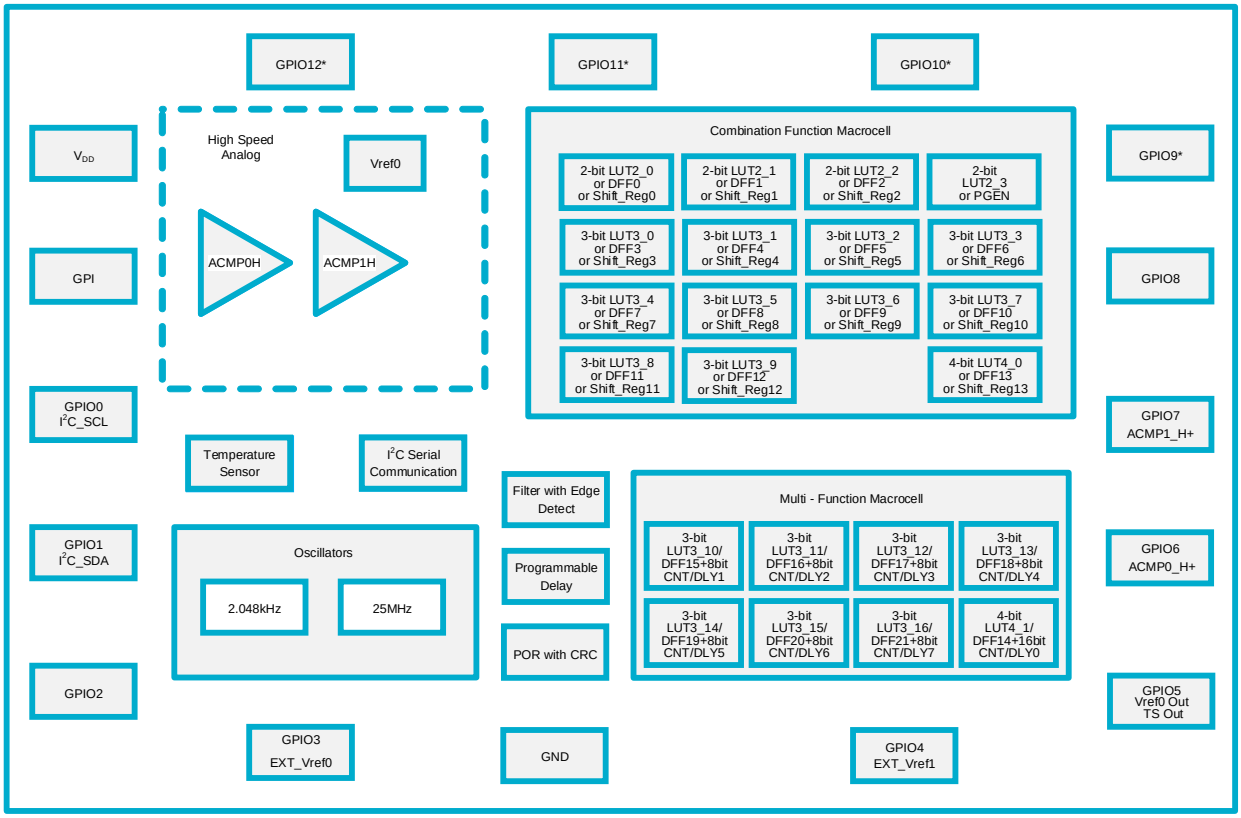
1 Block Diagram

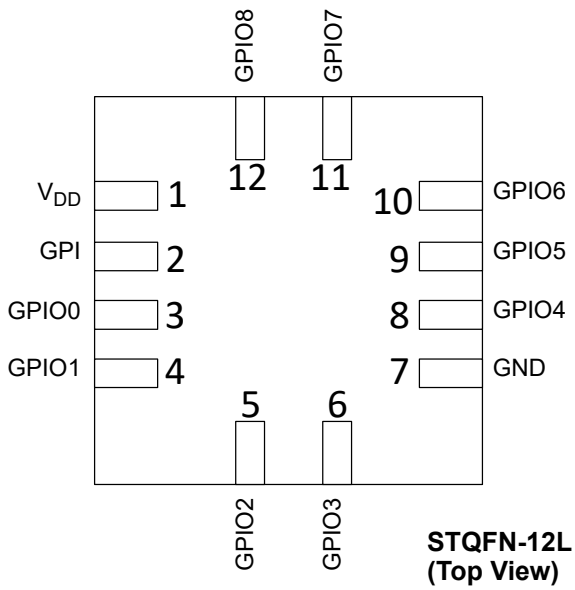


*Note *: GPIO 9, 10, 11, and 12 are available in 16-pin package only.*

Figure 1: Block Diagram

2 Pinout

2.1 PIN CONFIGURATION - STQFN- 12L



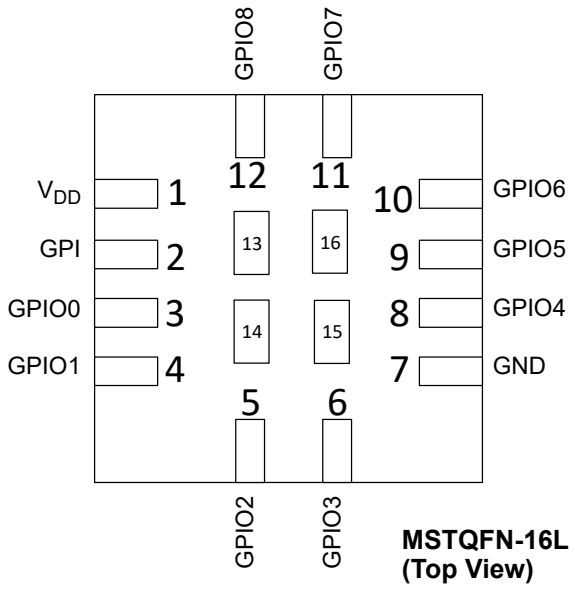
STQFN-12L
(Top View)

Pin #	Pin Name	Pin Functions
1	V_{DD}	Power Supply
2	GPI	GPI, SLA_0
3	GPIO0	GPIO, I^2C SCL
4	GPIO1	GPIO, I^2C SDA
5	GPIO2	GPIO with OE, EXT_OSC1_IN
6	GPIO3	GPIO with OE, EXT_Vref0, SLA_1
7	GND	Ground
8	GPIO4	GPIO with OE, EXT_Vref1, SLA_2
9	GPIO5	GPIO with OE, Vref_OUT, TS_OUT
10	GPIO6	GPIO with OE, ACMP0_H+
11	GPIO7	GPIO with OE, ACMP1_H+
12	GPIO8	GPIO with OE, SLA_3, EXT_OSC0_IN

Legend:

OE: Output Enable
ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
I^2C SCL: I^2C Clock Input
I^2C SDA: I^2C Data Input/Output
Vref: Voltage Reference Output
EXT_CLKx: External Clock Input
SLA: Slave Address
TS_OUT: Temperature Output

2.2 PIN CONFIGURATION - MSTQFN- 16L



MSTQFN-16L (Top View)

Pin #	Pin Name	Pin Functions
1	V_{DD}	Power Supply
2	GPI	GPI, SLA_0
3	GPIO0	GPIO, I^2C SCL
4	GPIO1	GPIO, I^2C SDA
5	GPIO2	GPIO with OE, EXT_OSC1_IN
6	GPIO3	GPIO with OE, EXT_Vref0, SLA_1
7	GND	Ground
8	GPIO4	GPIO with OE, EXT_Vref1, SLA_2
9	GPIO5	GPIO with OE, Vref_OUT, TS_OUT
10	GPIO6	GPIO with OE, ACMP0_H+
11	GPIO7	GPIO with OE, ACMP1_H+
12	GPIO8	GPIO with OE, SLA_3, EXT_OSC0_IN
13	GPIO9	GPIO with OE
14	GPIO10	GPIO with OE
15	GPIO11	GPIO with OE
16	GPIO12	GPIO with OE

Legend:

OE: Output Enable
ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
I^2C SCL: I^2C Clock Input
I^2C SDA: I^2C Data Input/Output
Vref: Voltage Reference Output
EXT_CLKx: External Clock Input
SLA: Slave Address
TS_OUT: Temperature Output

Table 1: Functional Pin Description

Pin #		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN-12L	MSTQFN-16L					
1	1	V_{DD}	V_{DD}	Power Supply	--	--
2	2	GPI	GPI	General Purpose Input	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
			I^2C Slave Address 0		--	--

Table 1: Functional Pin Description (Continued)

Pin #		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN-12L	MSTQFN-16L					
3	3	GPIO0	GPIO0	General Purpose IO (Note 1)	Digital Input without Schmitt Trigger	Open-Drain NMOS (1x)
					Digital Input with Schmitt Trigger	
					Low Voltage Digital Input	--
			I^2C SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
4	4	GPIO1	GPIO1	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (1x)
					Digital Input with Schmitt Trigger	
					Low Voltage Digital Input	
			I^2C SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
5	5	GPIO2	GPIO2	General Purpose IO with OE (Note 1)	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			EXT_OSC1_IN	External Clock Connection	--	--
6	6	GPIO3	GPIO3	General Purpose IO with OE (Note 1)	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			EXT_VREF0	Analog Comparator Negative Input	Analog	--
			I^2C Slave Address 1		--	--
7	7	GND	GND	Power Supply	--	--
8	8	GPIO4	GPIO4	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	

Table 1: Functional Pin Description (Continued)

Pin #		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN-12L	MSTQFN-16L					
8	8		EXT_VREF1	Analog Comparator Negative Input	Analog	--
			I^2C Slave Address 2		--	--
9	9	GPIO5	GPIO5	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			Vref0	Vref0 Output	Analog	--
			TS_OUT	Temperature Sensor Output	Analog	--
10	10	GPIO6	GPIO6	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP0_H+	Analog Comparator 0_H Positive Input	Analog	--
11	11	GPIO7	GPIO7	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP1_H+	Analog Comparator 1_H Positive Input	Analog	--
12	12	GPIO8	GPIO8	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			I^2C Slave Address 3		--	--
			EXT_OSC0_IN	External Clock Connection	--	--
--	13	GPIO9	GPIO9	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--

Table 1: Functional Pin Description (Continued)

Pin #		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN-12L	MSTQFN-16L					
--	14	GPIO10	GPIO10	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
--	15	GPIO11	GPIO11	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
--	16	GPIO12	GPIO12	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--

Note 1 General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure or as a 3-state output.

Table 2: Pin Type Definitions

Pin Type	Description
V_{DD}	Power Supply
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GND	Ground

3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} relative to GND			2.2	V
DC Input Voltage		GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	OD 1x	--	11	
	OD 2x	--	21	
Current at Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitive Level		1		

3.2 ELECTROSTATIC DISCHARGE RATINGS

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1000	--	V

3.3 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		1.0	1.65	V
Operating Temperature		-40	85	°C
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}+ 0.3	V
Typical Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

3.4 ELECTRICAL CHARACTERISTICS

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 1.0 V to 1.65 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input **(Note 1)**	0.6x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with 10 kΩ Pull-up **(Note 1)**	0.52x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with 10 kΩ Pull-down **(Note 1)**	0.83x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger (Positive Going Threshold Voltage min = 0.4xV_{DD}; max = 0.7xV_{DD})	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger (Positive Going Threshold Voltage min = 0.4xV_{DD}; max = 0.7xV_{DD}), with 10 kΩ Pull-up	0.62x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger (Positive Going Threshold Voltage min = 0.4xV_{DD}; max = 0.7xV_{DD}), with 10 kΩ Pull-down	0.88x V_{DD}	--	V_{DD}+ 0.3	V
		Low-Level Logic Input **(Note 1)**	0.6	--	--	V
		Low-Level Logic Input with 10 kΩ Pull-up **(Note 1)**	0.44	--	--	V
		Low-Level Logic Input with 10 kΩ Pull-down **(Note 1)**	0.75	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input **(Note 1)**	GND-0.3	--	0.35x V_{DD}	V
		Logic Input with 10 kΩ Pull-up **(Note 1)**	V_{DD}-0.3	--	0.19x V_{DD}	V
		Logic Input with 10 kΩ Pull-down **(Note 1)**	V_{DD}-0.3	--	0.37x V_{DD}	V
		Logic Input with Schmitt Trigger (Negative Going Threshold Voltage min = 0.3xV_{DD}; max = 0.6xV_{DD})	GND-0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt Trigger (Negative Going Threshold Voltage min = 0.3xV_{DD}; max = 0.6xV_{DD}), with 10 kΩ Pull-up	V_{DD}-0.3	--	0.16x V_{DD}	V
		Logic Input with Schmitt Trigger (Negative Going Threshold Voltage min = 0.3xV_{DD}; max = 0.6xV_{DD}), with 10 kΩ Pull-down	V_{DD}-0.3	--	0.37x V_{DD}	V
		Low-Level Logic Input **(Note 1)**	GND-0.3	--	0.27	V
		Low-Level Logic Input with 10 kΩ Pull-up **(Note 1)**	V_{DD}-0.3	--	0.08	V
		Low-Level Logic Input with 10 kΩ Pull-down **(Note 1)**	V_{DD}-0.3	--	0.33	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage		0.07	0.21	0.33	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 1.0 V to 1.65 V Unless Otherwise Noted (Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Schmitt Trigger Hysteresis Voltage	With 10 kΩ Pull-up/Pull-down	0.09x V_{DD}	0.25x V_{DD}	0.36x V_{DD}	V
		V_{DD} = 1.0 V	0.14	0.22	0.30	V
		V_{DD} = 1.2 V	0.12	0.23	0.33	V
		V_{DD} = 1.5 V	0.08	0.16	0.26	V
		V_{DD} = 1.65 V	0.07	0.14	0.22	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 1x Drive, I_{OH} = 100 µA	V_{DD}-0.01	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 2 mA	0.85x V_{DD}	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 100 µA	V_{DD} - 0.005	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 2 mA	0.93x V_{DD}	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, 1x Drive, I_{OL}= 100 µA	--	--	0.01	V
		Push-Pull, 1x Drive, I_{OL}= 1 mA	--	--	0.1x V_{DD}	V
		Push-Pull, 2x Drive, I_{OH} = 100 µA	--	--	0.005	V
		Push-Pull, 2x Drive, I_{OH} = 2 mA	--	--	0.1x V_{DD}	V
		NMOS OD, 1x Drive, I_{OL} = 100 µA	--	--	0.005	V
		NMOS OD, 1x Drive, I_{OL} = 2 mA	--	--	0.1x V_{DD}	V
		NMOS OD, 2x Drive, I_{OL} = 100 µA	--	--	0.002	V
		NMOS OD, 2x Drive, I_{OL} = 2 mA	--	--	0.05x V_{DD}	V
I_{OH}	HIGH-Level Output Pulse Current **(Note 2)**	Push-Pull, 1x Drive, V_{OH} = 0.8x V_{DD}	2.3	6.1	11.6	mA
		Push-Pull, 2x Drive, V_{OH} = 0.8x V_{DD}	4.3	11.5	22.2	mA
I_{OL}	LOW-Level Output Pulse Current **(Note 2)**	Push-Pull, 1x Drive, V_{OL} = 0.2x V_{DD}	1.6	5.0	9.1	mA
		Push-Pull, 2x Drive, V_{OL} = 0.2x V_{DD}	3.2	9.9	18.2	mA
		NMOS OD, 1x Drive, V_{OL} = 0.1x V_{DD}	2.0	5.9	11.2	mA
		NMOS OD, 2x Drive, V_{OL} = 0.1x V_{DD}	3.9	11.5	21.7	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}, t_{RAMP} = 1 µs	--	2.243	3.213	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	0.749	0.878	1.027	V
		T = -20 °C to 85 °C, V_{DD} Level Required to Start Up the Chip	0.758	0.878	0.990	V

Table 6: EC at T = -40 °C to +85 °C, V_{DD} = 1.0 V to 1.65 V Unless Otherwise Noted (Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.409	0.510	0.704	V
R_{PULL}	Pull-up or Pull-down Resistance	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k For Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	10	--	kΩ
C_{IN}	Input Capacitance	T = 25 °C, V_{DD} = 1.2 V		3.2		pF

Note 1 No hysteresis.
Note 2 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

3.5 I^2C PINS ELECTRICAL CHARACTERISTICS

Table 7: EC of the I^2C Pins for DI Mode at T = -40 °C to +85 °C, Full V_{DD} Range Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	0.3xV_{DD}	-0.5	0.3xV_{DD}	V
V_{IH}	HIGH-level Input Voltage		0.7xV_{DD}	V_{DD}	0.7xV_{DD}	V_{DD}	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05xV_{DD}	--	0.05xV_{DD}	--	V
V_{OL}	LOW-Level Output Voltage	Open-Drain at 2 mA sink current	0	0.2xV_{DD}	0	0.2xV_{DD}	V
		Open-Drain at 3 mA sink current	0	0.4	--	--	V
		Open-Drain at 20 mA sink current	--	--	--	0.21	V
I_{OL}	LOW-Level Output Current	V_{DD} = 1.2 V, V_{OL} = 0.2 V	3	--	20	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax}		--	250	--	120	ns
I_i	Input Current each IO Pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	-10	+10	mA
C_i	Capacitance for each IO Pin	T = 25 °C, V_{DD} = 1.2 V to 1.7 V	--	10	--	10	pF

Note 1 For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see register [1329] in section 17.

Table 8: EC of the I^2C Pins for DILV Mode at T = -40 °C to +85 °C, Full V_{DD} Range Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Unit
			Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	0.3xV_{DD}	V
V_{IH}	HIGH-level Input Voltage		0.7xV_{DD}	V_{DD}	V

Table 8: EC of the I²C Pins for DILV Mode at T = -40 °C to +85 °C, Full V_{DD} Range Unless Otherwise Noted (Continued)

Parameter	Description	Condition	Fast-Mode		Unit
			Min	Max	
V_{OL}	LOW-Level Output Voltage	Open-Drain at 2 mA sink current	0	$0.2xV_{DD}$	V
		Open-Drain at 3 mA sink current	0	0.4	V
I_{OL}	LOW-Level Output Current	V_{DD} = 1.3 V, V_{OL} = 0.2 V	3	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax}		--	250	ns
I_i	Input Current each IO Pin	$0.1xV_{DD} < V_I < 0.9xV_{DDmax}$	-10	+10	mA
C_i	Capacitance for each IO Pin	T = 25 °C, V_{DD} = 1.2 V to 1.7 V	--	10	pF

Table 9: I²C Pins Timing Characteristics for DI Mode, T = -40 °C to +85 °C, Full V_{DD} Range Unless Otherwise Noted

Parameter	Description	Condition	Speed				Unit
			400 kHz		1 MHz		
			Min	Max	Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	--	1000	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	500	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	260	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)		50	--	50	--	ns
t_{VD_ACK}	Data Valid Acknowledge Time		--	900	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	500	--	ns
t_{HD_STA}	Start Hold Time		600	--	260	--	ns
t_{SU_STA}	Start Set-up Time		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time **(Note 1)**		55	--	55	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
t_R	Inputs Rise Time		--	300	--	120	ns
t_F	Inputs Fall Time		--	300	--	120	ns
t_{SU_STO}	Stop Set-up Time		600	--	260	--	ns
t_{VD_DAT}	Data Valid Time		--	900	--	450	ns

Note 1 Does not meet standard I²C specifications: t_{HD_DAT} = 0 ns (min) for Fast-Mode and Fast-Mode Plus.
Note 2 Timing diagram can be found in Figure 99.

Table 10: I²C Pins Timing Characteristics for DILV Mode, T = -40 °C to +85 °C, Full V_{DD} Range Unless Otherwise Noted

Parameter	Description	Condition	Speed		Unit
			400 kHz		
			Min	Max	
F_{SCL}	Clock Frequency, SCL		--	400	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)		50	--	ns

Table 10: I^2C Pins Timing Characteristics for DILV Mode, T = -40 °C to +85 °C, Full V_{DD} Range Unless Otherwise Noted

Parameter	Description	Condition	Speed		Unit
			400 kHz		
			Min	Max	
t_{VD_ACK}	Data Valid Acknowledge Time		--	900	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	ns
t_{HD_STA}	Start Hold Time		600	--	ns
t_{SU_STA}	Start Set-up Time		600	--	ns
t_{HD_DAT}	Data Hold Time **(Note 1)**		200	--	ns
t_{SU_DAT}	Data Set-up Time **(Note 1)**		223	--	ns
t_R	Inputs Rise Time		--	300	ns
t_F	Inputs Fall Time		--	300	ns
t_{SU_STO}	Stop Set-up Time		600	--	ns
t_{VD_DAT}	Data Valid Time		--	900	ns

Note 1 Does not meet standard I^2C specifications: t_{HD_DAT} = 0 ns (min), t_{SU_DAT} = 100 ns (min).
Note 2 Timing diagram can be found in Figure 99.

3.6 MACROCELLS CURRENT CONSUMPTION

Table 11: Typical Current Estimated for Each Macrocell at T = 25 °C

Parameter	Description	Note	V_{DD} = 1.0 V	V_{DD} = 1.2 V	V_{DD} = 1.5 V	V_{DD} = 1.65 V	Unit
I_{DD}	Current	PDET+I^2C	0.32	0.40	0.56	0.70	µA
		PDET+BG+I^2C	0.83	0.93	1.14	1.31	µA
		PDET+BG+I_{BIAS}+ Vref Source+Buffer (Buffer Selection: Any ACMPxH Vref)	14.90	15.06	15.33	15.52	µA
		Temperature Sensor+PDET+BG+I_{BIAS}+ Vref Source+TPS+Buffer	15.70	15.86	16.13	16.32	µA
		PDET+BG+I_{BIAS}+Buffer (Vref Source - External, Buffer Selection: Any ACMPxH Vref)	8.04	8.17	8.41	8.59	µA
		OSC0+BG+PDET, Pre-divider = 1	1.04	1.18	1.46	1.66	µA
		OSC0+BG+PDET, Pre-divider = 4	1.04	1.18	1.46	1.66	µA
		OSC0+BG+PDET, Pre-divider = 8	1.04	1.18	1.46	1.66	µA
		OSC1+BG+PDET, Pre-divider = 1	67.94	79.49	96.28	107.51	µA
		OSC1+BG+PDET, Pre-divider = 4	70.33	82.36	99.85	111.55	µA
		OSC1+BG+PDET, Pre-divider = 8	69.12	80.91	98.08	109.57	µA
		PDET+BG+I_{BIAS}+ACMPH0+ ACMPH1 +Vref Source (Vref Source - Internal, V_{IN+} = V_{DD}, V_{IN-} = 25 mV)	17.80	18.23	18.78	19.07	µA
		PDET+BG+I_{BIAS}+ACMPH0+ ACMPH1 (V_{IN+} = V_{DD}, External Vref = 650 mV)	9.63	11.22	11.81	12.11	µA
		PDET+BG+I_{BIAS}+ACMPH0 (V_{IN+} = V_{DD}, External Vref = 650 mV)	5.42	6.28	6.69	6.92	µA

3.7 TIMING CHARACTERISTICS

Table 12: Typical Delay Estimated for Each Macrocell at T = 25 °C

Parameter	Description	Note	V_{DD} = 1.0 V		V_{DD} = 1.2 V		V_{DD} = 1.5 V		V_{DD} = 1.65 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input to PP 1x	18	18	12	12	8	8	7	7	ns
tpd	Delay	Digital Input to PP 2x	18	18	12	12	8	8	7	7	ns

Table 12: Typical Delay Estimated for Each Macrocell at T = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 1.0 V		V_{DD} = 1.2 V		V_{DD} = 1.5 V		V_{DD} = 1.65 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input with Schmitt Trigger to PP 1x	18	18	12	12	8	8	7	7	ns
tpd	Delay	Low Voltage Digital Input to PP 1x	18	18	12	12	8	8	7	7	ns
tpd	Delay	Digital input to NMOS 1x	--	18	--	12	--	8	--	7	ns
tpd	Delay	Digital input to NMOS 2x	--	18	--	12	--	8	--	7	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 1	19	--	12	--	10	--	9	--	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 0	--	19	--	12	--	10	--	9	ns
tpd	Delay	PP 1x 3 State Hi-Z to 1	19	--	12	--	10	--	9	--	ns
tpd	Delay	PP 1x 3 State Hi-Z to 0	--	19	--	12	--	10	--	9	ns
tpd	Delay	PP 2x 3 State Hi-Z to 1	19	--	11	--	10	--	9	--	ns
tpd	Delay	PP 2x 3 State Hi-Z to 0	--	19	--	11	--	10	--	9	ns
tpd	Delay	LATCH Q	13	13	8	8	5	5	4	4	ns
tpd	Delay	LATCH nQ	13	13	8	8	5	5	4	4	ns
tpd	Delay	LATCH nRESET High Q	13	13	8	8	5	5	4	4	ns
tpd	Delay	LATCH nRESET High nQ	13	13	8	8	5	5	4	4	ns
tpd	Delay	LATCH nRESET Low Q	13	13	8	8	5	5	4	4	ns
tpd	Delay	LATCH nRESET Low nQ	13	13	8	8	5	5	4	4	ns
tpd	Delay	LATCH nSET High Q	13	13	8	8	5	5	4	4	ns
tpd	Delay	LATCH nSET High nQ	13	13	8	8	5	5	4	4	ns
tpd	Delay	LATCH nSET Low Q	14	13	10	10	6	6	4	4	ns
tpd	Delay	LATCH nSET Low nQ	14	13	10	9	6	6	4	4	ns
tpd	Delay	Multi-Function LATCH Q	13	13	9	9	6	6	4	4	ns
tpd	Delay	Multi-Function LATCH nQ	13	13	9	9	6	6	4	4	ns
tpd	Delay	Multi-Function LATCH nRESET Q	13	13	9	9	6	6	4	4	ns
tpd	Delay	Multi-Function LATCH nRESET nQ	13	13	9	9	6	6	4	4	ns
tpd	Delay	Multi-Function LATCH nSET Q	13	13	9	9	6	6	4	4	ns
tpd	Delay	Multi-Function LATCH nSET nQ	13	13	9	9	6	6	4	4	ns
tpd	Delay	2-bit LUT	13	13	6	6	6	6	4	4	ns
tpd	Delay	3-bit LUT	13	13	9	8	6	6	4	4	ns
tpd	Delay	4-bit LUT	13	13	8	8	6	6	4	4	ns
tpd	Delay	Multi-Function 3-bit LUT	13	13	9	9	6	6	4	4	ns
tpd	Delay	Multi-Function 3-bit LUT, CNT Delay	13	13	9	9	6	6	4	4	ns
tpd	Delay	Multi-Function 4-bit LUT	13	13	9	9	6	6	4	4	ns
tpd	Delay	Multi-Function 4-bit LUT, CNT Delay	13	13	9	9	6	6	4	4	ns
tpd	Delay	Edge detect	10	10	5	5	4	4	3	3	ns

Table 12: Typical Delay Estimated for Each Macrocell at T = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 1.0 V		V_{DD} = 1.2 V		V_{DD} = 1.5 V		V_{DD} = 1.65 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	Rising	Falling	
tw	Width	Edge detect	227	227	155	155	137	137	126	126	ns
tpd	Delay	Edge detect Delayed	238	238	162	162	139	139	129	129	ns
tpd	Delay	DFF Q	12	12	7	7	5	5	4	4	ns
tpd	Delay	DFF nQ	12	12	7	7	5	5	4	4	ns
tpd	Delay	DFF nRESET High Q	--	12	--	7	5	5	--	4	ns
tpd	Delay	DFF nRESET High nQ	12	--	7	--	5	--	4	--	ns
tpd	Delay	DFF nRESET Low Q	--	12	--	7	--	5	--	4	ns
tpd	Delay	DFF nRESET Low nQ	12	--	7	--	5	--	4	--	ns
tpd	Delay	DFF nSET High Q	12	--	7	--	5	--	4	--	ns
tpd	Delay	DFF nSET High nQ	--	12	--	7	--	5	--	4	ns
tpd	Delay	DFF nSET Low Q	12	--	7	--	5	--	4	--	ns
tpd	Delay	DFF nSET Low nQ	--	12	--	7	--	5	--	4	ns
tpd	Delay	Multi-Function DFF Q	13	13	6	6	5	5	4	4	ns
tpd	Delay	Multi-Function DFF nQ	13	13	6	6	5	5	4	4	ns
tpd	Delay	Multi-Function DFF nRESET Q	--	13	--	6	5	5	--	4	ns
tpd	Delay	Multi-Function DFF nRESET nQ	13	--	6	--	5	--	4	--	ns
tpd	Delay	Multi-Function DFF nSET Q	13	--	6	--	5	--	4	--	ns
tpd	Delay	Multi-Function DFF nSET nQ	--	13	--	6	--	5	--	5	ns
tpd	Delay	Shift Registers Q	14	14	7	7	6	6	5	5	ns
tpd	Delay	Shift Registers nQ	14	14	7	7	6	6	5	5	ns
tpd	Delay	Multi-Function Reset CNT Q	19	--	9	--	7	--	6	--	ns
tpd	Delay	Multi-Function Reset CNT nQ	--	19	--	9	--	7	--	6	ns
tpd	Delay	Multi-Function CNT Delay Q	19	19	9	9	7	7	6	6	ns
tpd	Delay	Multi-Function CNT Delay nQ	19	19	9	9	7	7	6	6	ns
tpd	Delay	Multi-Function CNT Edge Detect Q	19	--	9	--	7	--	6	--	ns
tpd	Delay	Multi-Function CNT Edge Detect nQ	--	19	--	9	--	7	--	6	ns
tw	Width	Multi-Function CN T Edge Detect Q	159	--	91	--	70	--	62	--	ns
tw	Width	Multi-Function CNT Edge Detect nQ	--	159	--	91	--	70	--	62	ns
tpd	Delay	Multi-Function CNT Frequency Detect Q	32	32	18	18	14	14	12	12	ns
tpd	Delay	Multi-Function CNT Frequency Detect nQ	32	32	18	18	14	14	12	12	ns
tpd	Delay	Multi-Function CNT One Shot Q	15	--	9	--	7	--	6	--	ns
tpd	Delay	Multi-Function CNT One Short nQ	--	15	--	9	--	7	--	6	ns
tpd	Delay	PGen CLK	10	10	5	5	4	4	4	4	ns
tpd	Delay	PGen nRESET Hi-Z to 0	--	10	--	5	--	4	--	4	ns
tpd	Delay	PGen nRESET Hi-Z to 1	10	--	5	--	4	--	4	--	ns

Table 12: Typical Delay Estimated for Each Macrocell at T = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 1.0 V		V_{DD} = 1.2 V		V_{DD} = 1.5 V		V_{DD} = 1.65 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Filter Q	86	86	55	55	46	46	41	41	ns
tpd	Delay	Filter nQ	86	86	54	54	46	46	40	40	ns

Table 13: Programmable Delay Expected Typical Delays and Pulse Widths at T = 25 °C

Parameter	Description	Note	V_{DD} = 1.0 V	V_{DD} = 1.2 V	V_{DD} = 1.5 V	V_{DD} = 1.65 V	Unit
tw1	Pulse Width, 1 cell	mode: (any) edge detect, edge detect output	220	168	132	122	ns
tw2	Pulse Width, 2 cell	mode: (any) edge detect, edge detect output	444	338	266	244	ns
tw3	Pulse Width, 3 cell	mode: (any) edge detect, edge detect output	669	510	399	368	ns
tw4	Pulse Width, 4 cell	mode: (any) edge detect, edge detect output	898	682	534	492	ns
time1	Delay, 1 cell	mode: (any) edge detect, edge detect output	9	6	4	3	ns
time1	Delay, 2 cell	mode: (any) edge detect, edge detect output	9	6	4	3	ns
time1	Delay, 3 cell	mode: (any) edge detect, edge detect output	9	6	4	3	ns
time1	Delay, 4 cell	mode: (any) edge detect, edge detect output	9	6	4	3	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	229	173	135	124	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	453	343	268	247	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	679	514	402	369	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	910	688	537	494	ns

Table 14: Typical Filter Pulse Width

Parameter	Condition	V_{DD} = 1.0 V	V_{DD} = 1.2 V	V_{DD} = 1.5 V	V_{DD} = 1.65 V	Unit
Filtered Pulse Width, t_{block}	T = 25 °C	< 60.5	< 45	< 32.5	< 27.5	ns
	T = -40 °C to +85 °C	< 52	< 37	< 27	< 21.5	ns

3.8 COUNTER/DELAY CHARACTERISTICS

Table 15: Typical Counter/Delay Offset at T = 25 °C

Parameter	OSC Freq	OSC Power	V_{DD} = 1.0 V	V_{DD} = 1.2 V	V_{DD} = 1.5 V	V_{DD} = 1.65 V	Unit
Power-On time	25 MHz	auto	0.05	0.04	0.03	0.03	µs
Power-On time	2.048 kHz	auto	471	480	486	492	µs
frequency settling time	25 MHz	auto	0.8	0.8	0.8	0.8	µs

Table 15: Typical Counter/Delay Offset at T = 25 °C (Continued)

Parameter	OSC Freq	OSC Power	V_{DD} = 1.0 V	V_{DD} = 1.2 V	V_{DD} = 1.5 V	V_{DD} = 1.65 V	Unit
frequency settling time	2.048 kHz	auto	963	963	963	963	µs
variable (CLK period)	25 MHz	forced	0-40.6	0-40.6	0-40.6	0-40.6	ns
variable (CLK period)	2.048 kHz	forced	0.490	0-490	0-490	0-490	µs
tpd (non-delayed edge)	25 MHz/ 2.048 kHz	either	15	9	6	5	ns

3.9 OSCILLATOR CHARACTERISTICS

Table 16: Oscillators Frequency Limits, V_{DD} = 1.0 V to 1.65 V

Parameter	Temperature Range					
	+25 °C			-40 °C to +85 °C		
	Minimum Value, kHz	Maximum Value, kHz	Error, %	Minimum Value, kHz	Maximum Value, kHz	Error, %
2.048 kHz RC OSC0	2.0205	2.0754	+1.3	1.7655	2.1444	+4.7
			-1.3			-13.8
25 MHz RC OSC1	24100	25644	+2.6	22141	26250	+5.0
			-3.6			-11,4

3.9.1 OSC Power-On Delay

Table 17: Oscillators Power-On Delay at T = 25 °C, V_{DD} = 1.0 V to 1.65 V, OSC Power Setting: "Auto Power-On"

OSC0 2.048 kHz		OSC1 25 MHz		OSC1 25 MHz Start with Delay	
Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns	Typical Value, ns	Maximum Value, ns
476	--	40.45	55.33	152	--

3.10 ACMP CHARACTERISTICS

Table 18: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 1.0 V to 1.65 V Unless Otherwise Noted

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	V_{DD}	V
V_{offset}	ACMP Input Offset	Vhys = 0 mV, Gain = 1, Vref = 25 mV to 850 mV		-7.3	--	7.2	mV
I_{LKG}	ACMP Input Leakage			--	2	228	nA
t_{start}	ACMP Startup Time	ACMPxH Power-On delay, Minimal required wake time for the "Wake and Sleep function"	BG always On	--	--	78	µs
V_{HYS}	ACMP0H, ACMP1H Built-in Hysteresis **(Note 1)**	V_{HYS} = 25 mV	T = 25 °C	21.9	24.2	25.7	mV
		V_{HYS} = 150 mV	T = 25 °C	146.3	149.3	152.4	mV
		V_{HYS} = 25 mV		19.2	24.6	28.8	mV
		V_{HYS} = 150 mV		133.4	149.4	162.4	mV

Table 18: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 1.0 V to 1.65 V Unless Otherwise Noted (Continued)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
R_{sin}	Series Input Resistance	Gain = 1x		--	3.3	--	GΩ
		Gain = 0.5x		1.0	1.2	1.5	MΩ
PROP	Propagation Delay, Response Time	Gain = 1, Vref = 25 mV to 850mV, Overdrive = 100 mV	Low to High	--	0.6	2.8	µs
			High to Low	--	0.8	1.8	µs
		Gain = 1, Vref = 250 mV to 650mV, Overdrive = 100 mV	Low to High	--	0.6	2.8	µs
			High to Low	--	0.7	1.4	µs
G	Gain error	G = 1		--	1	--	
		G = 0.5	Vref > 250 mV	0.495	0.500	0.504	
Vref	Vref Accuracy, Buffer Disabled	Vref = 25 mV	T = 25 °C	-1.67	--	1.55	%
				-8.26	--	4.52	%
		Vref = 25 mV to 850 mV	T = 25 °C	-1.67	--	1.55	%
				-8.26	--	4.52	%
		Vref = 50 mV to 850 mV	T = 25 °C	-1.32	--	1.42	%
				-7.99	--	4.35	%
		Vref = 250 mV to 850 mV	T = 25 °C	-0.89	--	0.78	%
				-7.55	--	3.75	%
		Vref = 850 mV	T = 25 °C	-0.66	--	0.74	%
	Vref Output Buffer Offset	Vref = 25 mV to 450 mV	T = 25 °C	-5.54	--	7.56	mV
				-6.58	--	10.03	mV
	Vref Output Capacitance Loading		Load Resistance = 1 MΩ, Vref = 25 mV to 850 mV	--	--	50	pF
			Load Resistance = 1 kΩ, Vref = 25 mV to 850 mV	--	--	200	pF

Note 1 V_{IL} = Vin - V_{HYS}, V_{IH} = Vin.

3.11 ANALOG TEMPERATURE SENSOR CHARACTERISTICS

Temperature Sensor typical nonlinearity ±0.97 % for output at V_{DD} = 1.2 V.

Table 19: TS Output vs Temperature

T, °C	V_{DD} = 1.0 V		V_{DD} = 1.2 V		V_{DD} = 1.5 V		V_{DD} = 1.65 V	
	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %	Typical, mV	Accuracy, %
-40	834	±4.12	824	±1.98	818	±1.74	816	±1.73
-30	817	±3.32	807	±1.58	801	±1.46	799	±1.47
-20	799	±2.66	789	±1.26	783	±1.20	782	±1.22
-10	781	±2.06	771	±0.98	766	±0.99	764	±1.02
0	764	±1.54	753	±0.77	748	±0.81	746	±0.85
10	746	±1.09	735	±0.62	730	±0.67	728	±0.71
20	728	±0.84	717	±0.56	712	±0.60	710	±0.64
30	709	±0.88	698	±0.57	694	±0.59	692	±0.63
40	691	±1.20	680	±0.65	675	±0.65	674	±0.66
50	673	±1.66	661	±0.79	657	±0.76	655	±0.77
60	655	±2.19	642	±0.97	638	±0.91	637	±0.92
70	636	±2.73	623	±1.13	619	±1.05	618	±1.04
80	618	±3.31	604	±1.30	600	±1.22	599	±1.21
85	608	±3.62	595	±1.39	591	±1.31	589	±1.30

4 User Programmability

The SLG47512/13 is a user programmable device with one time programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

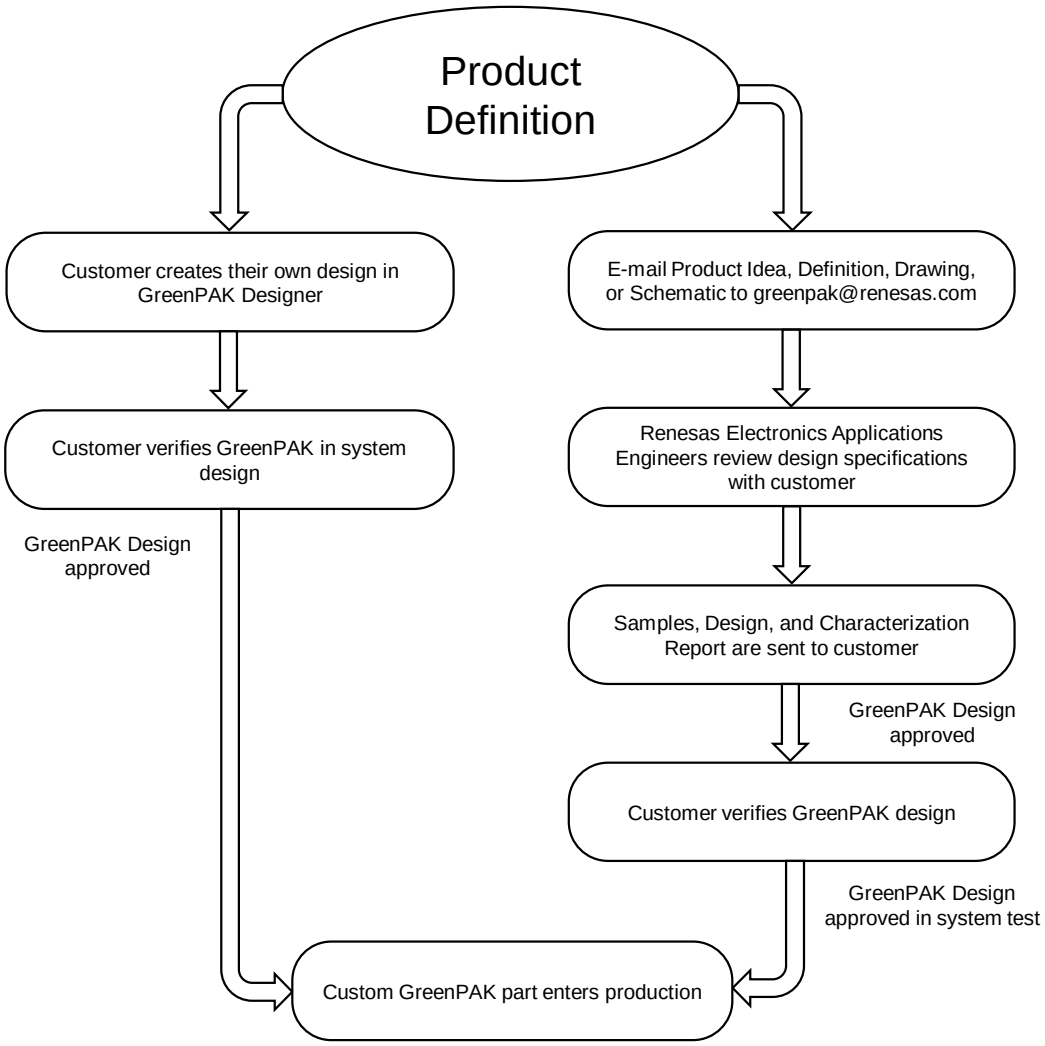


Figure 2: Steps to Create a Custom GreenPAK Device

5 IO Pins

The SLG47512/13 has a total of 9 GPIOs (13 GPIOs for 16-PIN version) which can operate as Input or Output, and 1 GPI Pin which can operate as Input, as well as serve as a special function (such as outputting the voltage reference).

5.1 GPIO PINS

Pins from GPIO0 to GPIO12 serve as General Purpose IO Pins.

5.2 GPI PIN

GPI serves as a General Purpose Input Pin.

5.3 PULL-UP/DOWN RESISTORS

All IO Pins, except GPI, have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either Pull-up or Pull-downs.

5.4 FAST PULL-UP/DOWN DURING POWER-UP

During power-up, IO Pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by register [1426].

5.5 GPI STRUCTURE

5.5.1 GPI Structure (for GPI)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1, OE=0
01: Digital In with Schmitt Trigger, smt_en = 1, OE = 0
10: Low Voltage Digital In mode, lv_en = 1, OE = 0
11: Reserved

Note 1: OE cannot be selected by user
Note 2: OE is Matrix output, Digital In is Matrix input

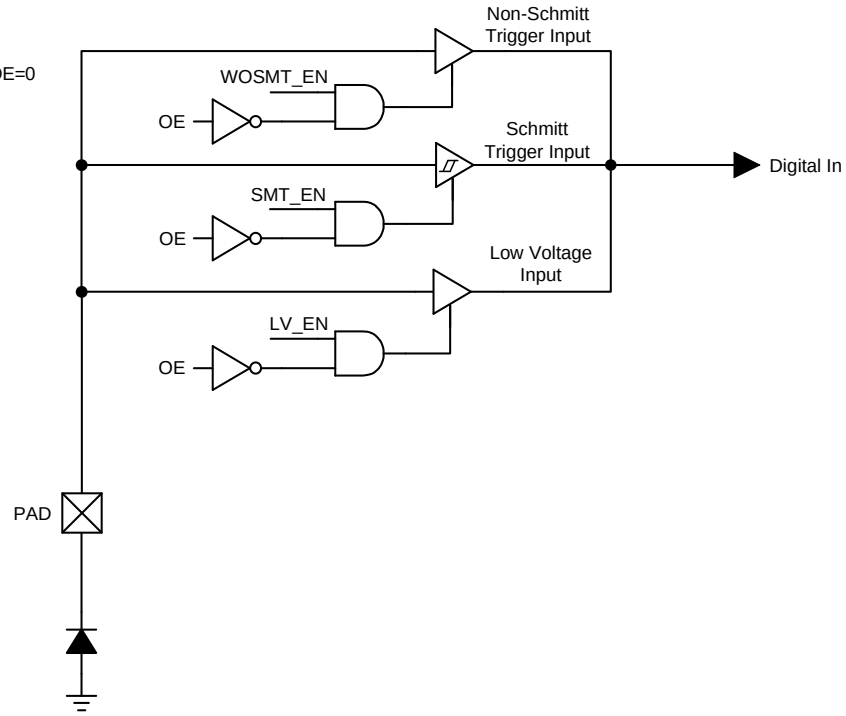


Figure 3: GPI Structure Diagram

5.6 GPIO WITH I²C MODE IO STRUCTURE

5.6.1 GPIO with I²C Mode Structure (for GPIO0 and GPIO1)

GPIO0, GPIO1 Mode [2:0]
00: Digital Input without Schmitt Trigger
01: Digital Input with Schmitt Trigger
10: Low Voltage Digital Input
11: Reserved

Note 1: OE cannot be selected by user and is controlled by register. Digital In is Matrix input.
Note 2: GPIO0 and GPIO1 do not support Push-Pull and PMOS Open-Drain modes.
Note 3: Can be varied over PVT, for reference only.

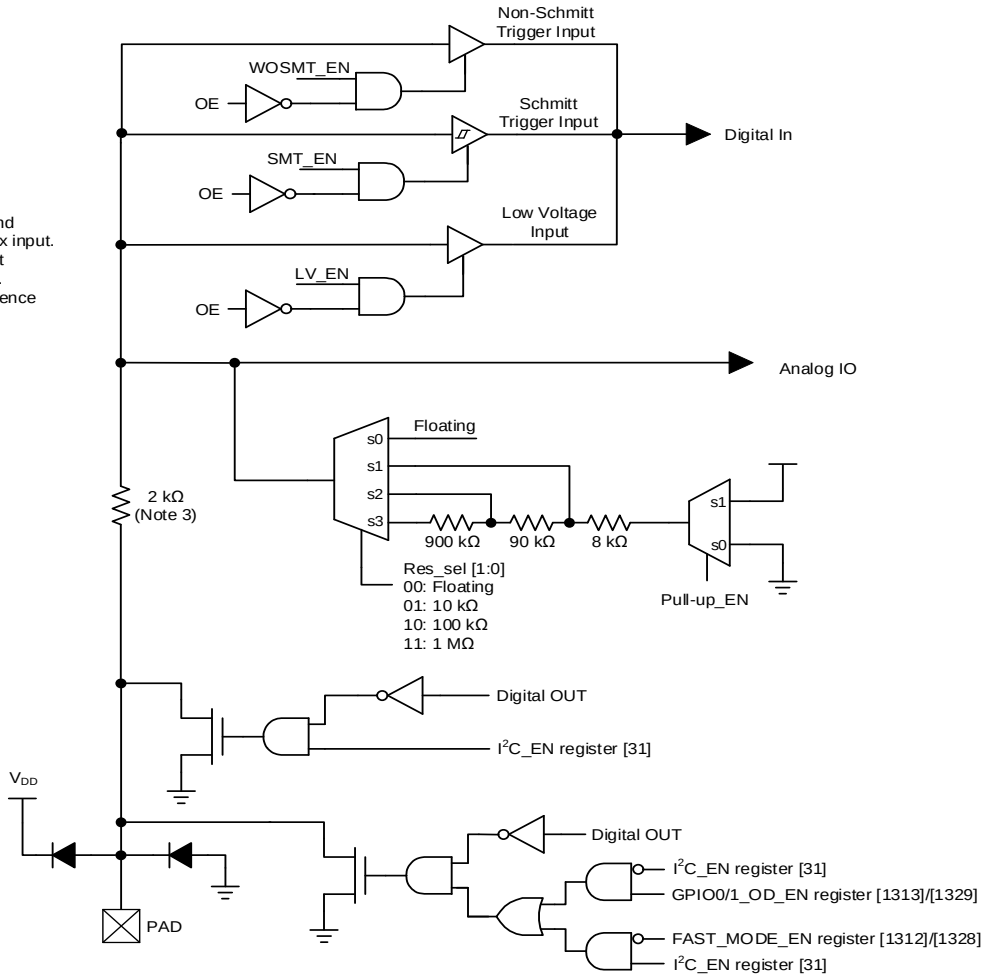


Figure 4: GPIO with I²C Mode IO Structure Diagram

5.7 MATRIX OE IO STRUCTURE

5.7.1 Matrix OE IO Structure (from GPIO0 to GPIO11)

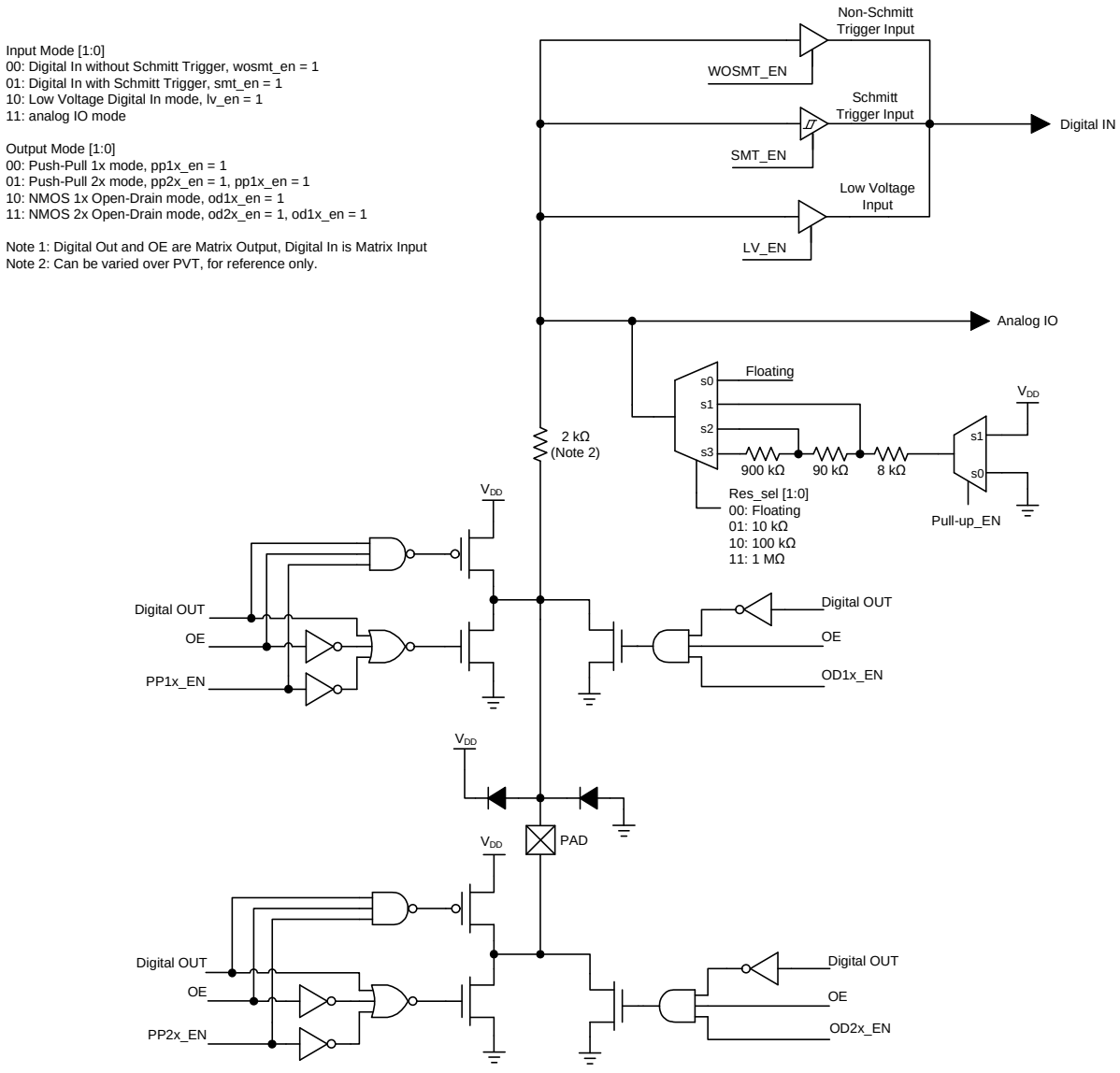


Figure 5: Matrix OE IO Structure Diagram

5.8 IO TYPICAL PERFORMANCE

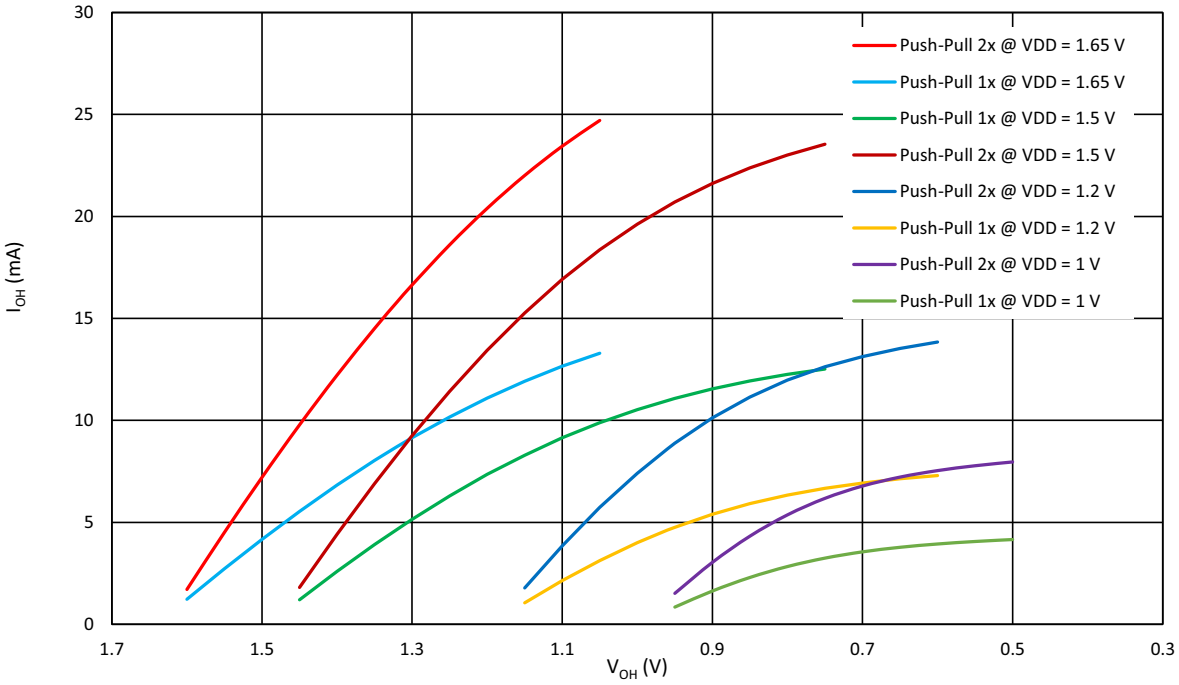


Figure 6: Typical High Level Output Current vs. High Level Output Voltage at T = 25 °C

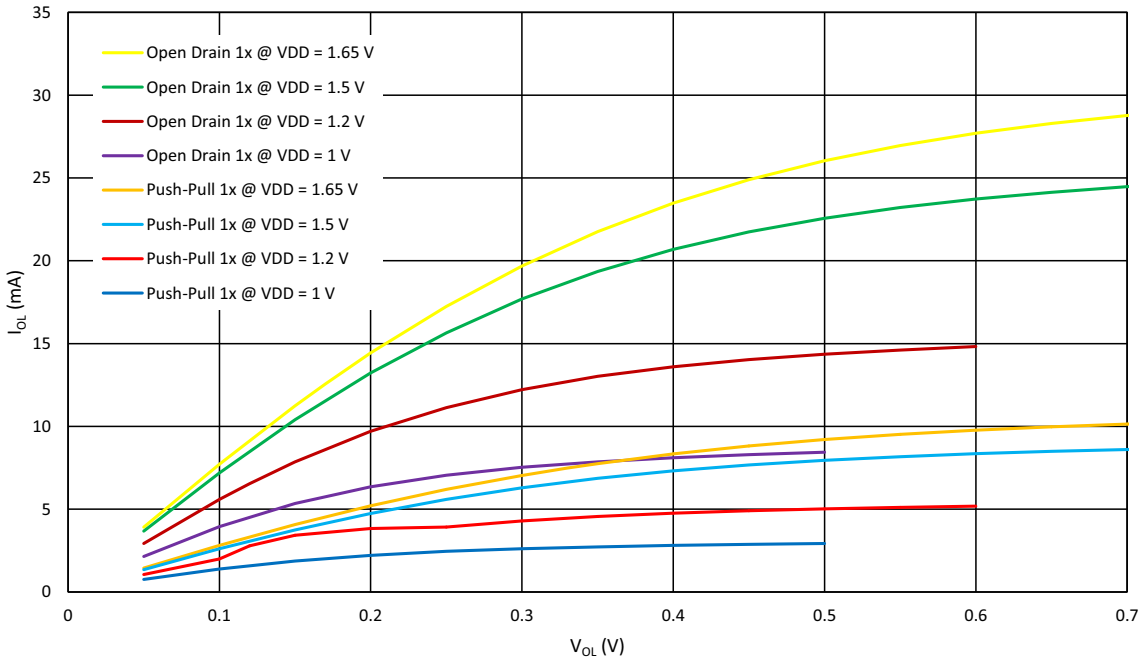


Figure 7: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C, Full Range

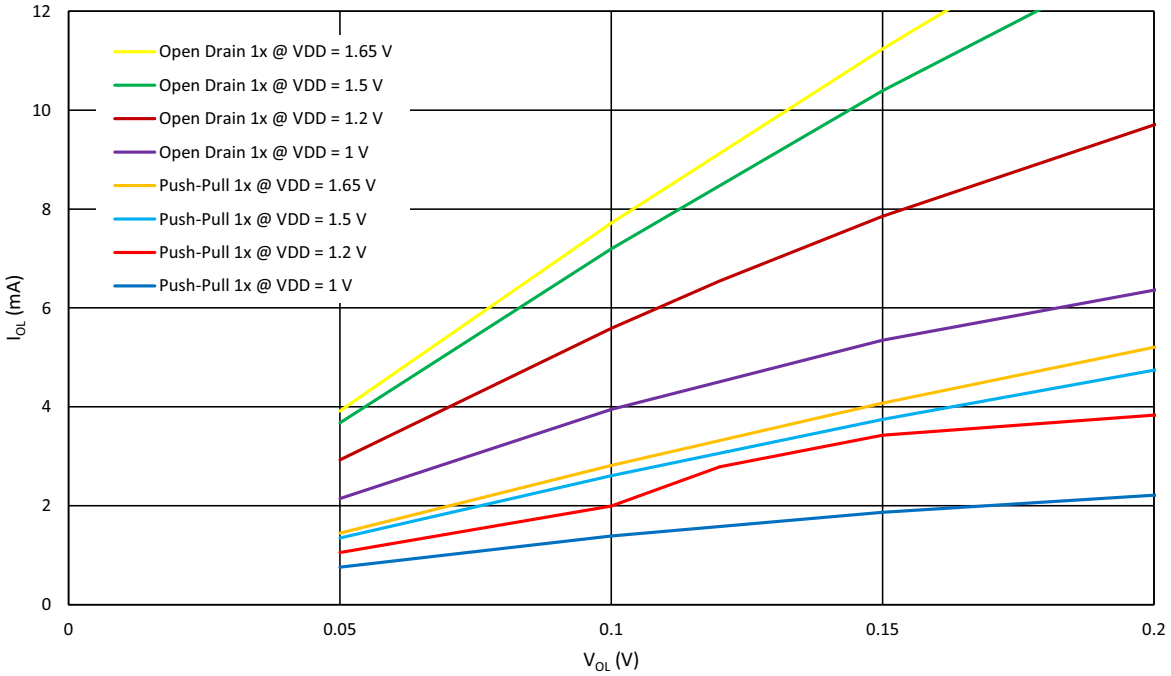


Figure 8: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C

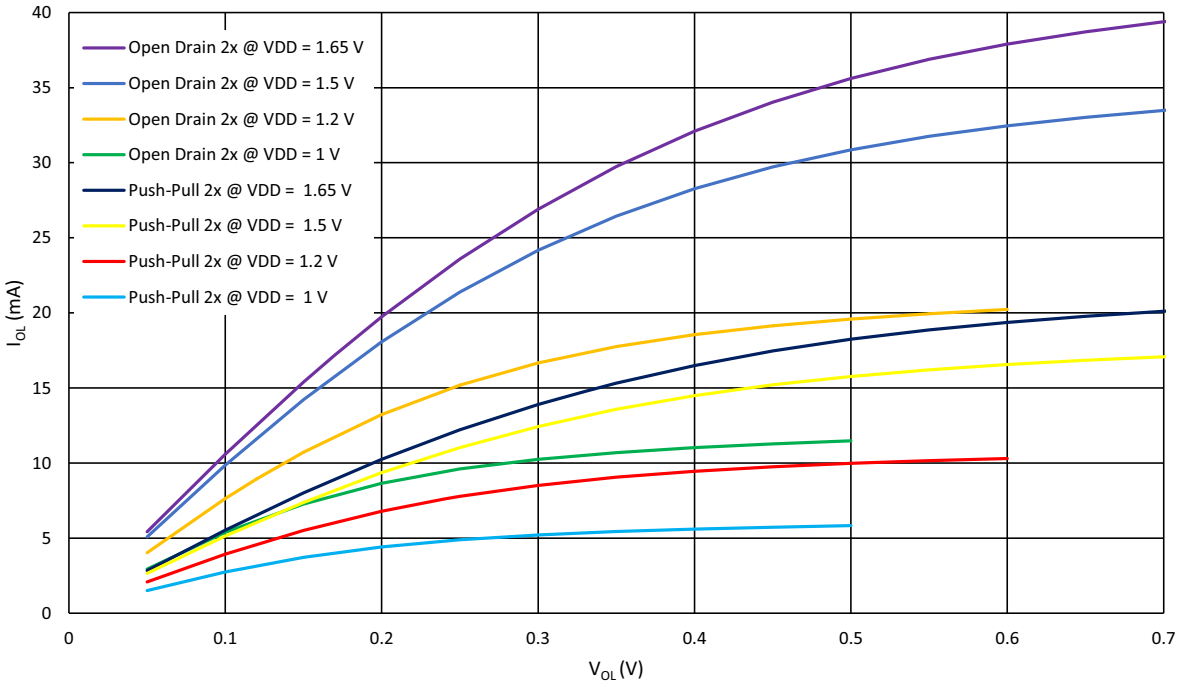


Figure 9: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C, Full Range

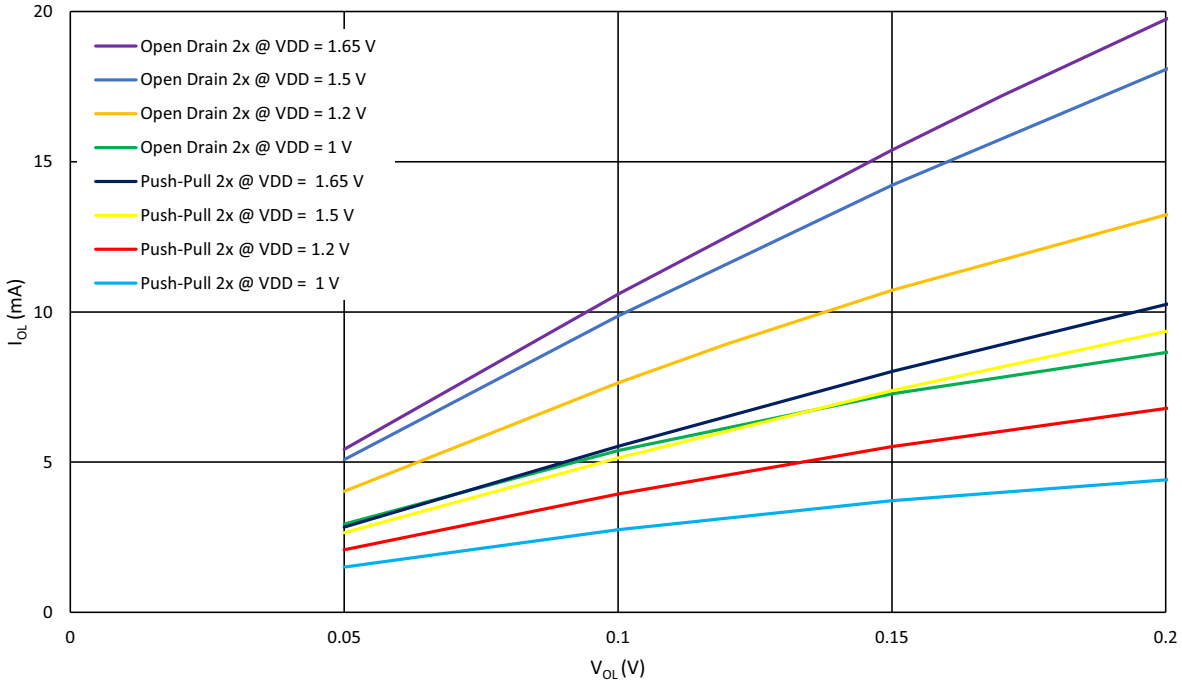


Figure 10: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C

6 Connection Matrix

The Connection Matrix in the SLG47512/13 is used to create an internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one time programmable (OTP) NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG47512/13 has a specific digital bit code assigned to it, that is either set to active “High” or inactive “Low”, based on the design that is created. Once the 2048 register bits within the SLG47512/13 are programmed, a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 98 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG47512/13’s register table, see Section 17.

Matrix Input Signal Functions	N
GND	0
LUT2_0/DFF0 output/ Shift_Reg0 output	1
LUT2_1/DFF1 output/ Shift_Reg1 output	2
LUT2_2/DFF2 output/ Shift_Reg2 output	3
⋮	⋮
POR	62
V_{DD}	63

Matrix Inputs

Matrix Outputs

N	0	1	2	⋯	97
Registers	registers [45:40]	registers [51:46]	registers [57:52]	⋯	registers [627:622]
Function	Matrix OUT: IN0 of LUT2_0 or Clock Input of DFF0 or Clock Input of Shift_Reg0	Matrix OUT: IN1 of LUT2_0 or Data Input of DFF0 or Data Input of Shift_Reg0	Matrix Out: IN0 of LUT2_1 or Clock Input of DFF1 or Clock Input of Shift_Reg1	⋯	Matrix Out: Oscillator1 ENABLE

Figure 11: Connection Matrix

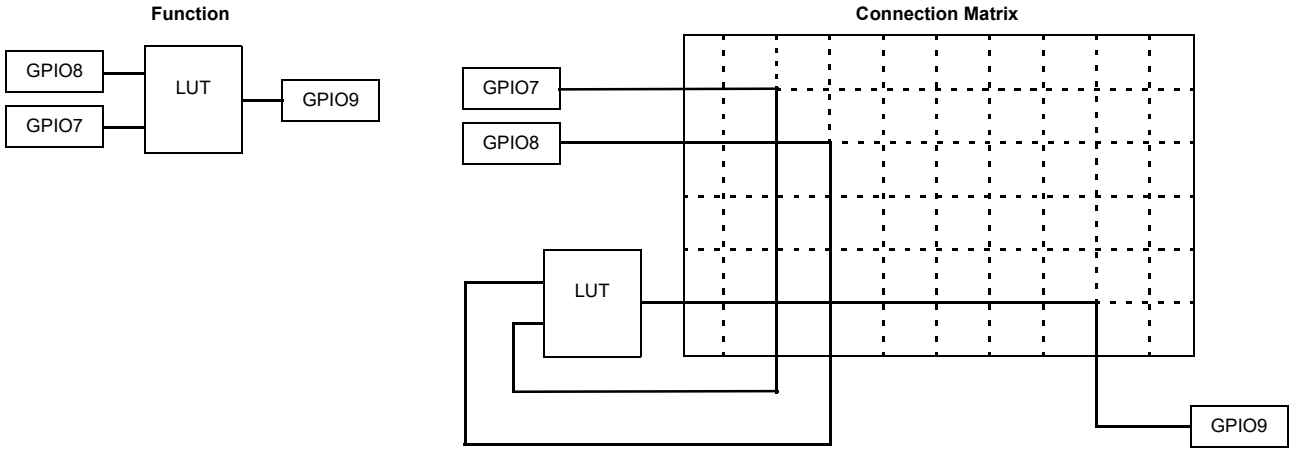


Figure 12: Connection Matrix Usage Example

6.1 MATRIX INPUT TABLE

Table 20: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	LUT2_0/DFF0 output/Shift_Reg0 output	0	0	0	0	0	1
2	LUT2_1/DFF1 output/Shift_Reg1 output	0	0	0	0	1	0
3	LUT2_2/DFF2 output/Shift_Reg2 output	0	0	0	0	1	1
4	LUT2_3/PGen output	0	0	0	1	0	0
5	LUT3_0/DFF3 output/Shift_Reg3 output	0	0	0	1	0	1
6	LUT3_1/DFF4 output/Shift_Reg4 output	0	0	0	1	1	0
7	LUT3_2/DFF5 output/Shift_Reg5 output	0	0	0	1	1	1
8	LUT3_3/DFF6 output/Shift_Reg6 output	0	0	1	0	0	0
9	LUT3_4/DFF7 output/Shift_Reg7 output	0	0	1	0	0	1
10	LUT3_5/DFF8 output/Shift_Reg8 output	0	0	1	0	1	0
11	LUT3_6/DFF9 output/Shift_Reg9 output	0	0	1	0	1	1
12	LUT3_7/DFF10 output/Shift_Reg10 output	0	0	1	1	0	0
13	LUT3_8/DFF11 output/Shift_Reg11 output	0	0	1	1	0	1
14	LUT3_9/DFF12 output/Shift_Reg12 output	0	0	1	1	1	0
15	LUT4_0/DFF13 output/Shift_Reg13 output	0	0	1	1	1	1
16	CNT0 output	0	1	0	0	0	0
17	MLT0_LUT4_1/DFF14_OUT	0	1	0	0	0	1
18	CNT1 output	0	1	0	0	1	0
19	MLT1_LUT3_10/DFF15_OUT	0	1	0	0	1	1
20	CNT2 output	0	1	0	1	0	0
21	MLT2_LUT3_11/DFF16_OUT	0	1	0	1	0	1
22	CNT3 output	0	1	0	1	1	0
23	MLT3_LUT3_12/DFF17_OUT	0	1	0	1	1	1
24	CNT4 output	0	1	1	0	0	0
25	MLT4_LUT3_13/DFF18_OUT	0	1	1	0	0	1
26	CNT5 output	0	1	1	0	1	0
27	MLT5_LUT3_14/DFF19_OUT	0	1	1	0	1	1
28	CNT6 output	0	1	1	1	0	0
29	MLT6_LUT3_15/DFF20_OUT	0	1	1	1	0	1
30	CNT7 output	0	1	1	1	1	0
31	MLT7_LUT3_16/DFF21_OUT	0	1	1	1	1	1
32	GPIO0 digital input or I^2C_virtual_0 Input	1	0	0	0	0	0
33	GPIO1 digital input or I^2C_virtual_1 Input	1	0	0	0	0	1
34	I^2C_virtual_2 Input	1	0	0	0	1	0

Table 20: Matrix Input Table (Continued)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
35	I^2C_virtual_3 Input	1	0	0	0	1	1
36	I^2C_virtual_4 Input	1	0	0	1	0	0
37	I^2C_virtual_5 Input	1	0	0	1	0	1
38	I^2C_virtual_6 Input	1	0	0	1	1	0
39	I^2C_virtual_7 Input	1	0	0	1	1	1
40	Programmable Delay Edge Detect Output	1	0	1	0	0	0
41	Edge Detect Filter Output	1	0	1	0	0	1
42	GPI Digital Input	1	0	1	0	1	0
43	GPIO2 Digital Input	1	0	1	0	1	1
44	GPIO3 Digital Input	1	0	1	1	0	0
45	GPIO4 Digital Input	1	0	1	1	0	1
46	GPIO5 Digital Input	1	0	1	1	1	0
47	GPIO6 Digital Input	1	0	1	1	1	1
48	GPIO7 Digital Input	1	1	0	0	0	0
49	GPIO8 Digital Input	1	1	0	0	0	1
50	GPIO9 Digital Input **(Note 1)**	1	1	0	0	1	0
51	GPIO10 Digital Input **(Note 1)**	1	1	0	0	1	1
52	GPIO11 Digital Input **(Note 1)**	1	1	0	1	0	0
53	GPIO12 Digital Input **(Note 1)**	1	1	0	1	0	1
54	Reserved	1	1	0	1	1	0
55	Reserved	1	1	0	1	1	1
56	Reserved	1	1	1	0	0	0
57	Oscillator0 output 0	1	1	1	0	0	1
58	Oscillator0 output 1	1	1	1	0	1	0
59	Oscillator1 output	1	1	1	0	1	1
60	ACMP0H Output	1	1	1	1	0	0
61	ACMP1H Output	1	1	1	1	0	1
62	POR	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

Note 1 GPIO 9, 10, 11, and 12 are available in 16-pin package only.

6.2 MATRIX OUTPUT TABLE

Table 21: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[45:40]	IN0 of LUT2_0 or Clock Input of DFF0 or Clock Input of Shift_Reg0	0
[51:46]	IN1 of LUT2_0 or Data Input of DFF0 or Data Input of Shift_Reg0	1
[57:52]	IN0 of LUT2_1 or Clock Input of DFF1 or Clock Input of Shift_Reg1	2
[63:58]	IN1 of LUT2_1 or Data Input of DFF1 or Data Input of Shift_Reg1	3
[69:64]	IN0 of LUT2_2 or Clock Input of DFF2 or Clock Input of Shift_Reg2	4
[75:70]	IN1 of LUT2_2 or Data Input of DFF2 or Data Input of Shift_Reg2	5
[81:76]	IN0 of LUT2_3 or Clock Input of PGen	6
[87:82]	IN1 of LUT2_3 or nRST of PGen	7
[93:88]	IN0 of LUT3_0 or Clock Input of DFF3 or Clock Input of Shift_Reg3	8
[99:94]	IN1 of LUT3_0 or Data Input of DFF3 or Data Input of Shift_Reg3	9
[105:100]	IN2 of LUT3_0 or nRST(nSET) of DFF3 or nRST(nSET) of Shift_Reg3	10
[111:106]	IN0 of LUT3_1 or Clock Input of DFF4 or Clock Input of Shift_Reg4	11
[117:112]	IN1 of LUT3_1 or Data Input of DFF4 or Data Input of Shift_Reg4	12
[123:118]	IN2 of LUT3_1 or nRST(nSET) of DFF4 or nRST(nSET) of Shift_Reg4	13
[129:124]	IN0 of LUT3_2 or Clock Input of DFF5 or Clock Input of Shift_Reg5	14
[135:130]	IN1 of LUT3_2 or Data Input of DFF5 or Data Input of Shift_Reg5	15
[141:136]	IN2 of LUT3_2 or nRST(nSET) of DFF5 or nRST(nSET) of Shift_Reg5	16
[147:142]	IN0 of LUT3_3 or Clock Input of DFF6 or Clock Input of Shift_Reg6	17
[153:148]	IN1 of LUT3_3 or Data Input of DFF6 or Data Input of Shift_Reg6	18
[159:154]	IN2 of LUT3_3 or nRST(nSET) of DFF6 or nRST(nSET) of Shift_Reg6	19
[165:160]	IN0 of LUT3_4 or Clock Input of DFF7 or Clock Input of Shift_Reg7	20
[171:166]	IN1 of LUT3_4 or Data Input of DFF7 or Data Input of Shift_Reg7	21
[177:172]	IN2 of LUT3_4 or nRST(nSET) of DFF7 or nRST(nSET) of Shift_Reg7	22
[183:178]	IN0 of LUT3_5 or Clock Input of DFF8 or Clock Input of Shift_Reg8	23
[189:184]	IN1 of LUT3_5 or Data Input of DFF8 or Data Input of Shift_Reg8	24
[195:190]	IN2 of LUT3_5 or nRST(nSET) of DFF8 or nRST(nSET) of Shift_Reg8	25
[201:196]	IN0 of LUT3_6 or Clock Input of DFF9 or Clock Input of Shift_Reg9	26
[207:202]	IN1 of LUT3_6 or Data Input of DFF9 or Data Input of Shift_Reg9	27
[213:208]	IN2 of LUT3_6 or nRST(nSET) of DFF9 or nRST(nSET) of Shift_Reg9	28
[219:214]	IN0 of LUT3_7 or Clock Input of DFF10 or Clock Input of Shift_Reg10	29
[225:220]	IN1 of LUT3_7 or Data Input of DFF10 or Data Input of Shift_Reg10	30
[231:226]	IN2 of LUT3_7 or nRST(nSET) of DFF10 or nRST(nSET) of Shift_Reg10	31
[237:232]	IN0 of LUT3_8 or Clock Input of DFF11 or Clock Input of Shift_Reg11	32
[243:238]	IN1 of LUT3_8 or Data Input of DFF11 or Data Input of Shift_Reg11	33
[249:244]	IN2 of LUT3_8 or nRST(nSET) of DFF11 or nRST(nSET) of Shift_Reg11	34
[255:250]	IN0 of LUT3_9 or Clock Input of DFF12 or Clock Input of Shift_Reg12	35

Table 21: Matrix Output Table (Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[261:256]	IN1 of LUT3_9 or Data Input of DFF12 or Data Input of Shift_Reg12	36
[267:262]	IN2 of LUT3_9 or nRST(nSET) of DFF12 or nRST(nSET) of Shift_Reg12	37
[273:268]	IN0 of LUT4_0 or Clock Input of DFF13 or Clock Input of Shift_Reg13	38
[279:274]	IN1 of LUT4_0 or Data Input of DFF13 or Data Input of Shift_Reg13	39
[285:280]	IN2 of LUT4_0 or nRST(nSET) of DFF13 or nRST(nSET) of Shift_Reg13	40
[291:286]	IN3 of LUT4_0 or Clock Enable of DFF13 or Clock Enable of Shift_Reg13	41
[297:292]	IN0 of MLT0_LUT4_1 or Clock Input of DFF14 or Delay0 Input (or Counter0 nRST Input)	42
[303:298]	IN1 of MLT0_LUT4_1 or nRST (nSET) of DFF14 or Delay0 Input (or Counter0 nRST Input or External Clock Source)	43
[309:304]	IN2 of MLT0_LUT4_1 or Data Input of DFF14 or Delay0 Input (or Counter0 nRST Input)	44
[315:310]	IN3 of MLT0_LUT4_1	45
[321:316]	IN0 of MLT1_LUT3_10 or Clock Input of DFF15 or Delay1 Input (or Counter1 nRST Input)	46
[327:322]	IN1 of MLT1_LUT3_10 or nRST (nSET) of DFF15 or Delay1 Input (or Counter1 nRST Input or External Clock Source)	47
[333:328]	IN2 of MLT1_LUT3_10 or Data Input of DFF15 or Delay1 Input (or Counter1 nRST Input)	48
[339:334]	IN0 of MLT2_LUT3_11 or Clock Input of DFF16 or Delay2 Input (or Counter2 nRST Input)	49
[345:340]	IN1 of MLT2_LUT3_11 or nRST (nSET) of DFF16 or Delay2 Input (or Counter2 nRST Input or External Clock Source)	50
[351:346]	IN2 of MLT2_LUT3_11 or Data Input of DFF16 or Delay2 Input (or Counter2 nRST Input)	51
[357:352]	IN0 of MLT3_LUT3_12 or Clock Input of DFF17 or Delay3 Input (or Counter3 nRST Input)	52
[363:358]	IN1 of MLT3_LUT3_12 or nRST (nSET) of DFF17 or Delay3 Input (or Counter3 nRST Input or External Clock Source)	53
[369:364]	IN2 of MLT3_LUT3_12 or Data Input of DFF17 or Delay3 Input (or Counter3 nRST Input)	54
[375:370]	IN0 of MLT4_LUT3_13 or Clock Input of DFF18 or Delay4 Input (or Counter4 nRST Input)	55
[381:376]	IN1 of MLT4_LUT3_13 or nRST (nSET) of DFF18 or Delay4 Input (or Counter4 nRST Input or External Clock Source)	56
[387:382]	IN2 of MLT4_LUT3_13 or Data Input of DFF18 or Delay4 Input (or Counter4 nRST Input)	57
[393:388]	IN0 of MLT5_LUT3_14 or Clock Input of DFF19 or Delay5 Input (or Counter5 nRST Input)	58
[399:394]	IN1 of MLT5_LUT3_14 or nRST (nSET) of DFF19 or Delay5 Input (or Counter5 nRST Input or External Clock Source)	59
[405:400]	IN2 of MLT5_LUT3_14 or Data Input of DFF19 or Delay5 Input (or Counter5 nRST Input)	60

Table 21: Matrix Output Table (Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[411:406]	IN0 of MLT6_LUT3_15 or Clock Input of DFF20 or Delay6 Input (or Counter6 nRST Input)	61
[417:412]	IN1 of MLT6_LUT3_15 or nRST (nSET) of DFF20 or Delay6 Input (or Counter6 nRST Input or External Clock Source)	62
[423:418]	IN2 of MLT6_LUT3_15 or Data Input of DFF20 or Delay6 Input (or Counter6 nRST Input)	63
[429:424]	IN0 of MLT7_LUT3_16 or Clock Input of DFF21 or Delay7 Input (or Counter7 nRST Input)	64
[435:430]	IN1 of MLT7_LUT3_16 or nRST (nSET) of DFF21 or Delay7 Input (or Counter7 nRST Input or External Clock Source)	65
[441:436]	IN2 of MLT7_LUT3_16 or Data Input of DFF21 or Delay7 Input (or Counter7 nRST Input)	66
[447:442]	GPIO0 Digital Output	67
[453:448]	GPIO1 Digital Output	68
[459:454]	GPIO2 Digital Output OE	69
[465:460]	GPIO2 Digital Output	70
[471:466]	GPIO3 Digital Output OE	71
[477:472]	GPIO3 Digital Output	72
[483:478]	GPIO4 Digital Output OE	73
[489:484]	GPIO4 Digital Output	74
[495:490]	GPIO5 Digital Output OE	75
[501:496]	GPIO5 Digital Output	76
[507:502]	GPIO6 Digital Output OE	77
[513:508]	GPIO6 Digital Output	78
[519:514]	GPIO7 Digital Output OE	79
[525:520]	GPIO7 Digital Output	80
[531:526]	GPIO8 Digital Output OE	81
[537:532]	GPIO8 Digital Output	82
[543:538]	GPIO9 Digital Output OE **(Note 2)**	83
[549:544]	GPIO9 Digital Output **(Note 2)**	84
[555:550]	GPIO10 Digital Output OE **(Note 2)**	85
[561:556]	GPIO10 Digital Output **(Note 2)**	86
[567:562]	GPIO11 Digital Output OE **(Note 2)**	87
[573:568]	GPIO11 Digital Output **(Note 2)**	88
[579:574]	GPIO12 Digital Output OE **(Note 2)**	89
[585:580]	GPIO12 Digital Output **(Note 2)**	90
[591:586]	Filter/Edge Detect Input	91
[597:592]	Programmable Delay/Edge Detect Input	92
[603:598]	PWR UP of ACMP0_H	93

Table 21: Matrix Output Table (Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[609:604]	PWR UP of ACMP1_H	94
[615:610]	Temp sensor, Vref Out_0 Power Up	95
[621:616]	Oscillator0 ENABLE	96
[627:622]	Oscillator1 ENABLE	97
Note 1 For each Address, the two most significant bits are unused. **Note 2** GPIO 9, 10, 11, and 12 are available in 16-pin package only.		

6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at byte 0x1.

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs (GPIO0 Digital or I^2C_virtual_0 Input), and (GPIO1 Digital or I^2C_virtual_1 Input). If the virtual input mode is selected, an I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). The I^2C disable/enable register bit [31] selects whether the Connection Matrix input comes from the Pin input or from the virtual register:

- Select SCL & Virtual Input 0 or GPIO0
- Select SDA & Virtual Input 1 or GPIO1

See Table 22 for Connection Matrix Virtual Inputs.

Table 22: Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I^2C_virtual_0 Input	[8]
33	I^2C_virtual_1 Input	[9]
34	I^2C_virtual_2 Input	[10]
35	I^2C_virtual_3 Input	[11]
36	I^2C_virtual_4 Input	[12]
37	I^2C_virtual_5 Input	[13]
38	I^2C_virtual_6 Input	[14]
39	I^2C_virtual_7 Input	[15]

7 Combination Function Macrocells

The SLG47512/13 has 15 combination function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as 2-bit LUT or as D Flip-Flop, or as Shift Register
- Ten macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input, or as Shift Register
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)
- One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input, or as Shift Register

Inputs/Outputs for the 15 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-BIT LUT OR D FLIP-FLOP OR SHIFT REGISTER MACROCELLS

There are three macrocells that can serve as 2-bit LUT or as DFF/LATCH, or as Shift Register. It is also possible to define the active level (Q or nQ) for the macrocell's output by registers [748], [753], [758]. DFF/Shift Register or LUT are selected by registers [744], [749], [754]. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

When used to implement Shift Register, the two input signals from the connection matrix go to the data (D_in), clock (CLK) inputs for the Shift Register, with the output going back to the connection matrix. The input data (D_in) writes into LSB. The Shift Register length (up to 4 bits/memory cells) is selected by registers [746:745], [751:750], [756:755], when these registers = 0 DFF/LATCH function is selected.

When used to implement DFF/LATCH function, the two input signals from the connection matrix go to the data (D_in), clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix. LATCH or DFF configuration is selected by registers [747], [752], [757].

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

It's possible to read/write the Shift Register content via I^2C (bytes 4Fh and 50h). See section 15.4.10 for more information.

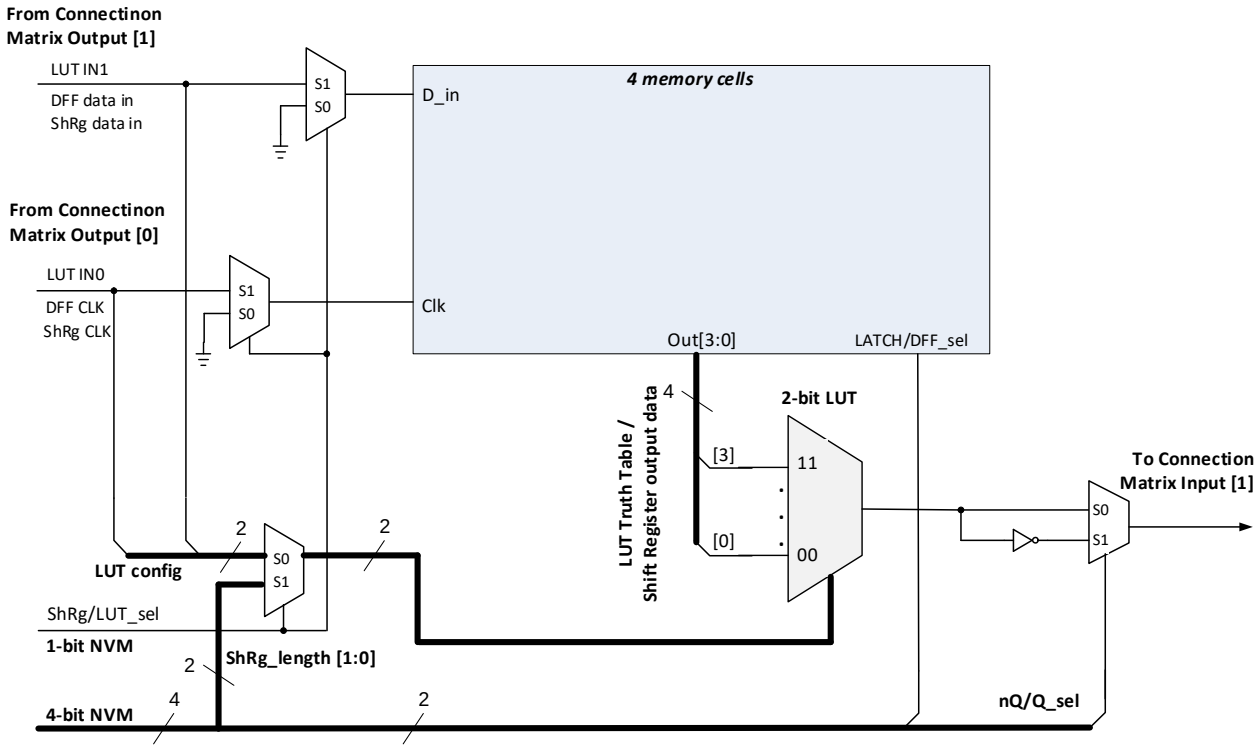


Figure 13: 2-bit LUT0 or DFF0 or Shift Register0

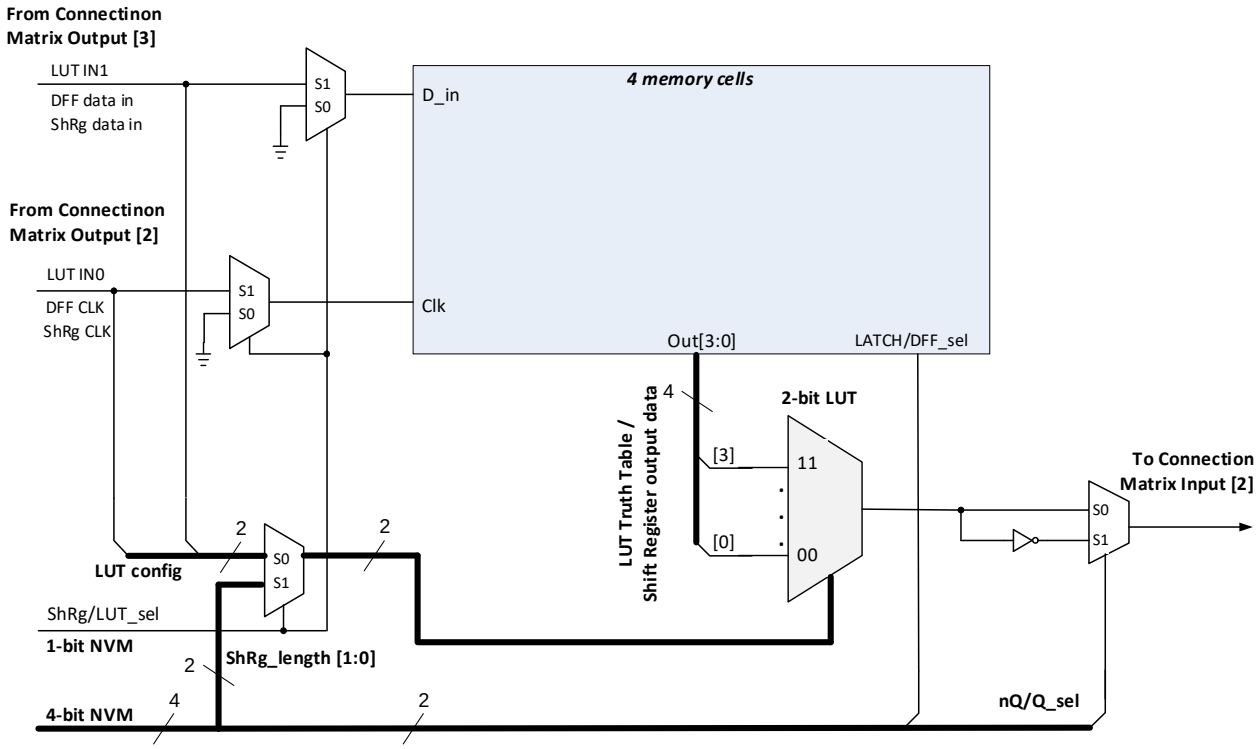


Figure 14: 2-bit LUT1 or DFF1 or Shift Register1

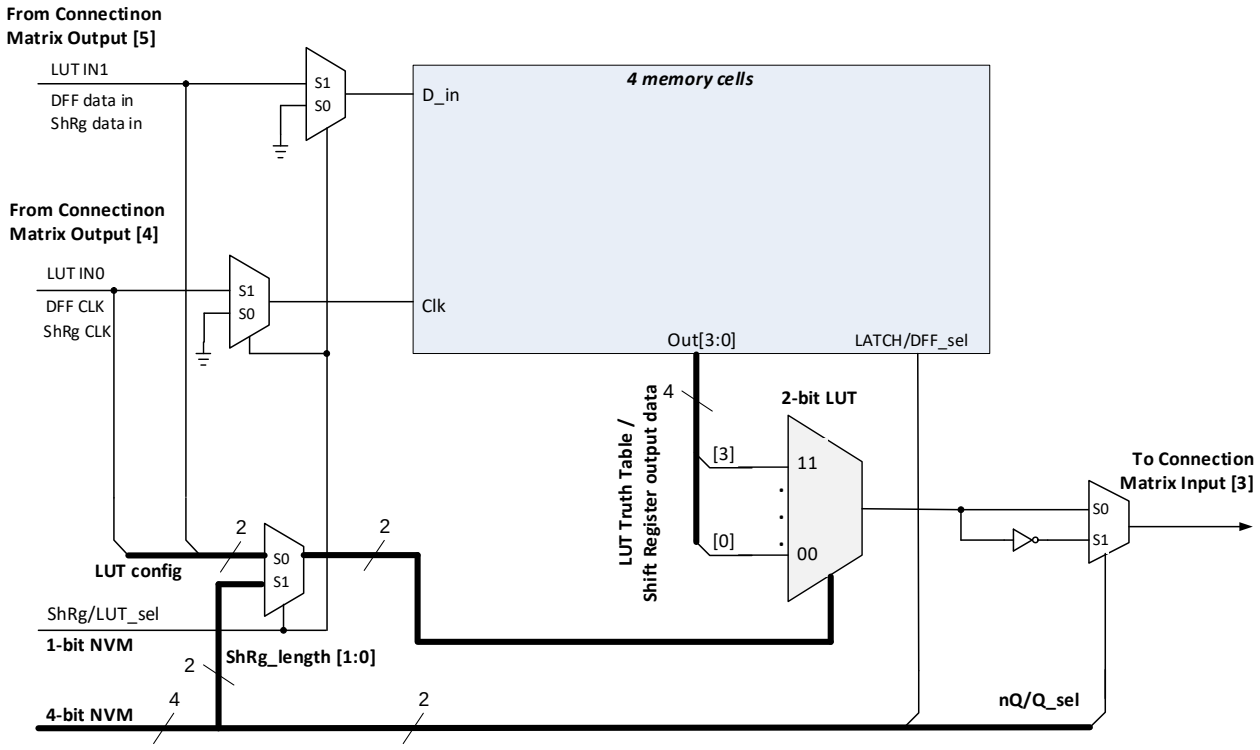
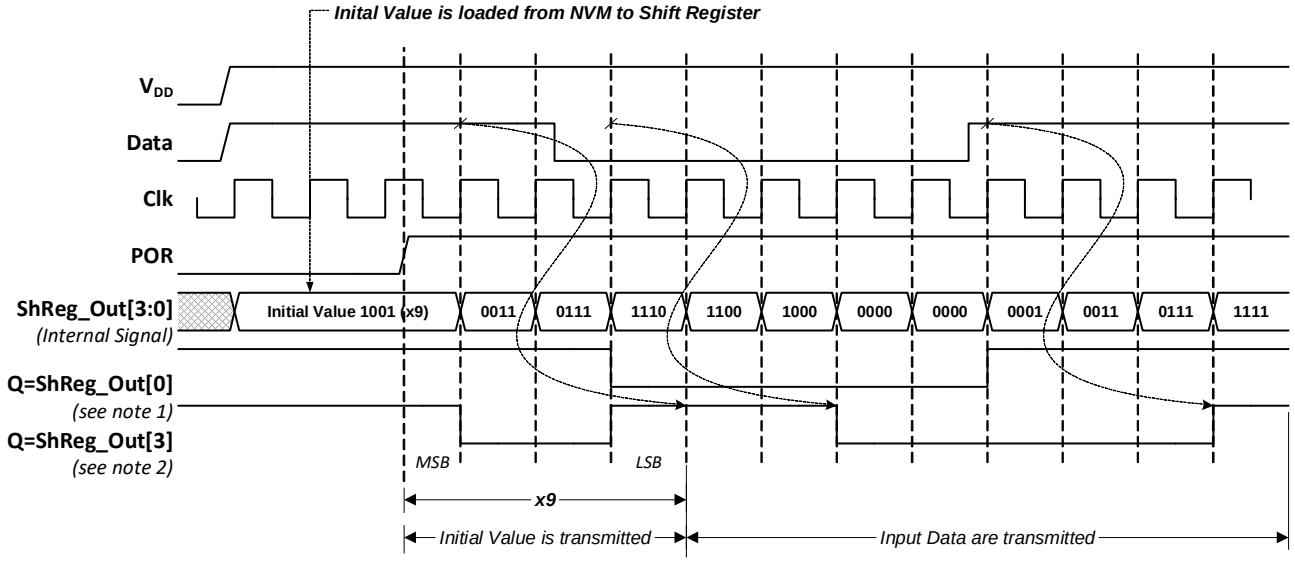
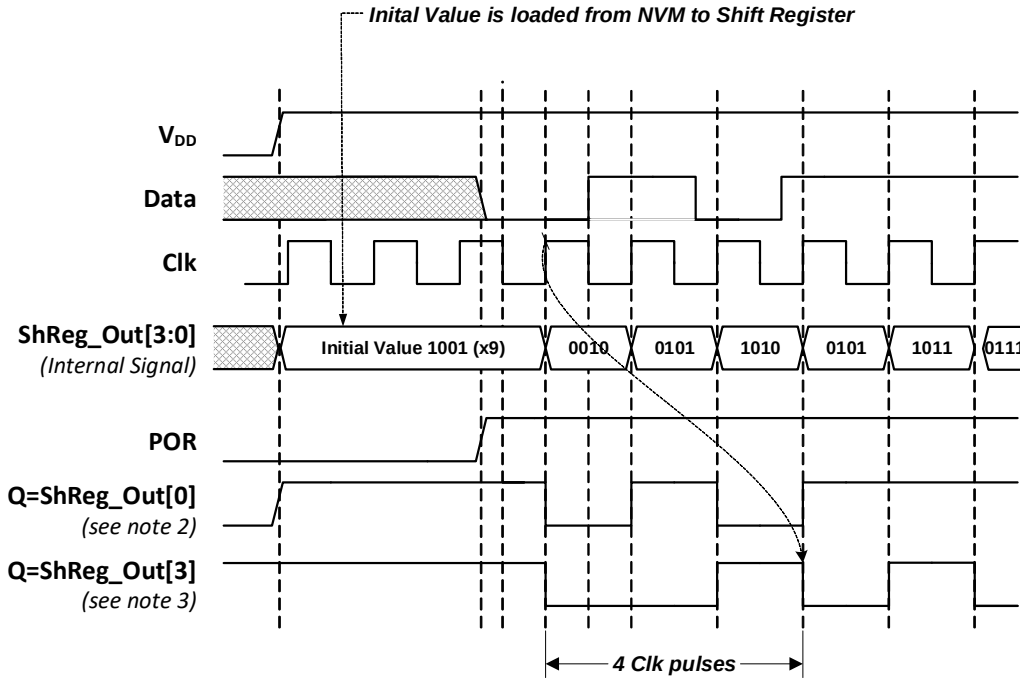


Figure 15: 2-bit LUT2 or DFF2 or Shift Register2



***Note1** : Macrocell is configured as DFF*
***Note2** : Macrocell is configured as 4-bit Shift Register*

Figure 16: DFF0 to DFF2 and Shift Register0 to Shift Register2 Operation



Note1 *: DFF Setting "Initial Value: 1"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 4-bits ShReg*

Figure 17: DFF0 to DFF2 and Shift Register0 to Shift Register2 Operation with DFF Initial Value = 1

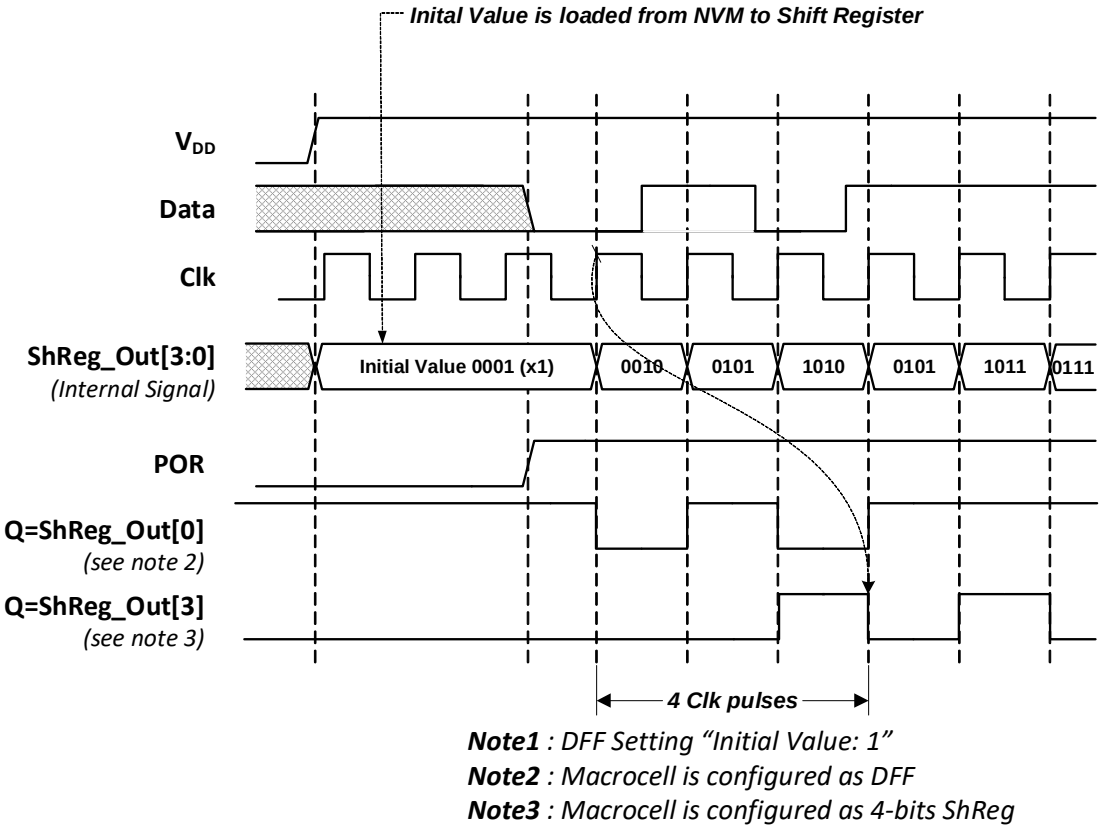


Figure 18: DFF0 to DFF2 and Shift Register0 to Shift Register2 Operation with Initial Value = b0001

7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

This Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by registers [635:632]

2-Bit LUT1 is defined by registers [639:636]

2-Bit LUT2 is defined by registers [643:640]

Table 23: 2-bit LUT2_0 to 2-bit LUT2_2 Truth Table

IN1	IN0	OUT LUT0	OUT LUT1	OUT LUT2	
0	0	register [632]	register [636]	register [640]	LSB
0	1	register [633]	register [637]	register [641]	
1	0	register [634]	register [638]	register [642]	
1	1	register [635]	register [639]	register [643]	MSB

Table 24 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 24: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.2 2-BIT LUT OR PROGRAMMABLE PATTERN GENERATOR

The SLG47512/13 has one combination function macrocell that can serve as a logic or a timing function. This macrocell can serve as a Look Up Table (LUT), or a Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

It is possible to define the RST level for the PGen macrocell. There are both high level reset (RST) and a low level reset (nRST) options available, which are selected by register [760]. When operating as the Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

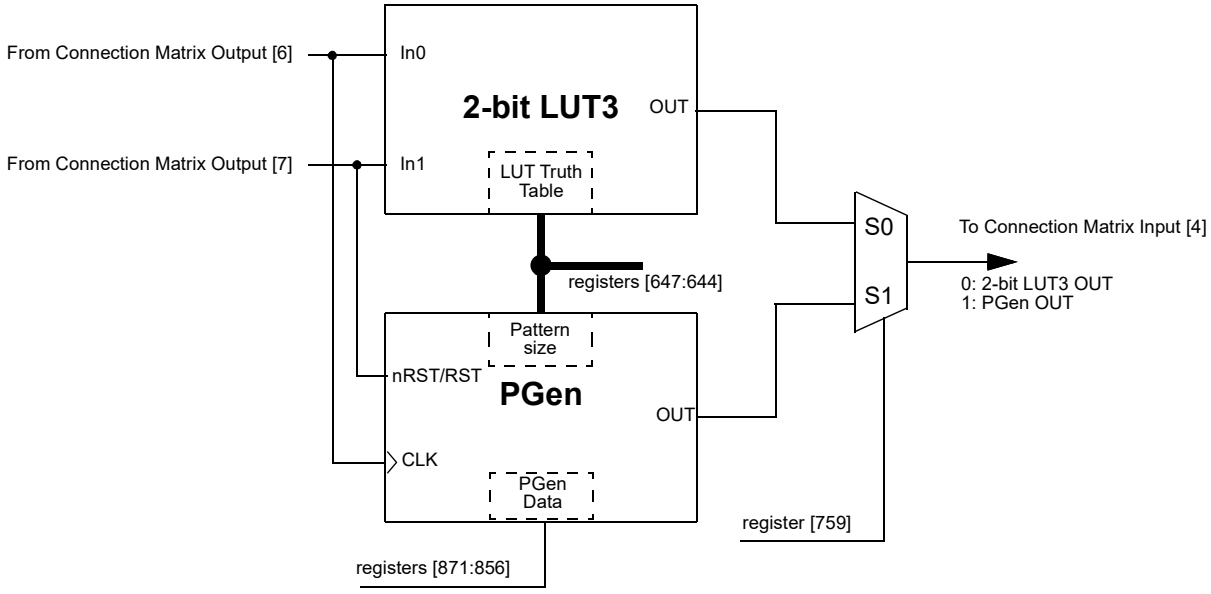


Figure 19: 2-bit LUT3 or PGen

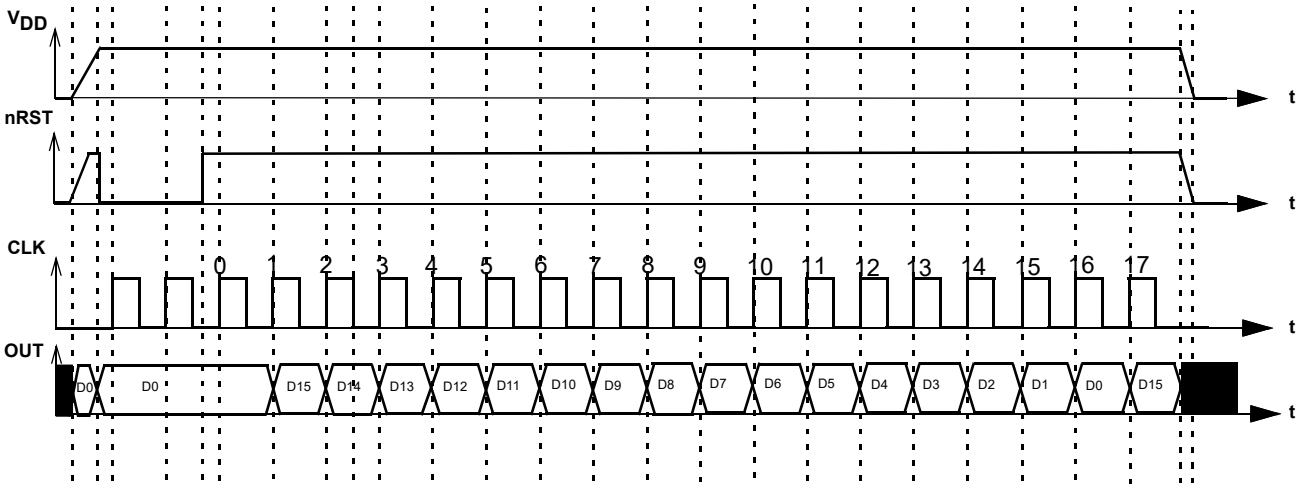


Figure 20: PGen Timing Diagram

Table 25: 2-bit LUT2_3 Truth Table

IN1	IN0	OUT	
0	0	register [647]	LSB
0	1	register [646]	
1	0	register [645]	
1	1	register [644]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT2_3 is defined by registers [647:644]

Table 26 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 26: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET OR SHIFT REGISTER MACROCELLS

There are ten macrocells that can serve as 3-bit LUT or as DFF/LATCH, or as Shift Register. It is also possible to define the active level (Q or nQ) for the macrocell's output by registers [766], [774], [782], [790], [798], [806], [814], [822], [830], [838]. DFF/Shift Register or LUT are selected by registers [761], [769], [777], [785], [793], [801], [809], [817], [825], [833]. When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used to implement Shift Register, the three input signals from the connection matrix go to the data (D_in), clock (CLK), and Set/Reset (nSET/nRST) inputs for the Shift Register, with the output going back to the connection matrix. It is possible to define the active level for the Set/Reset input of Shift Register macrocell which is selected by registers [768], [776], [784], [792], [800], [808], [816], [824], [832], [840]. The input data (D_in) writes into LSB. The Shift Register length (up to 8 bits/memory cells) is selected by registers [764:762], [772:770], [780:778], [788:786], [796:794], [804:802]. [812:810], [820:818], [828:826], [836:834], [845:842], when these registers = 0 DFF/LATCH function is selected.

When used to implement D Flip-Flop/LATCH function, the three input signals from the connection matrix go to the data (D_in), clock (CLK), and Set/Reset (nSET/nRST) inputs for the Flip-Flop/LATCH, with the output going back to the connection matrix. It is possible to define the active level for the Set/Reset input (nSET/nRST_sel which is selected by register [767], [775], [783], [791], [799], [807], [815], [823], [831], [839]) of DFF/LATCH macrocell. LATCH or DFF configuration is selected by registers [765], [773], [781], [789], [797], [805], [813], [821], [829], [837].

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

It's possible to read/write the Shift Register content via I^2C (bytes 51h, 52h, 53h, 54h, 55h, 56h, 57h, 58h, 59h and 5Ah). See section 15.4.10 for more information.

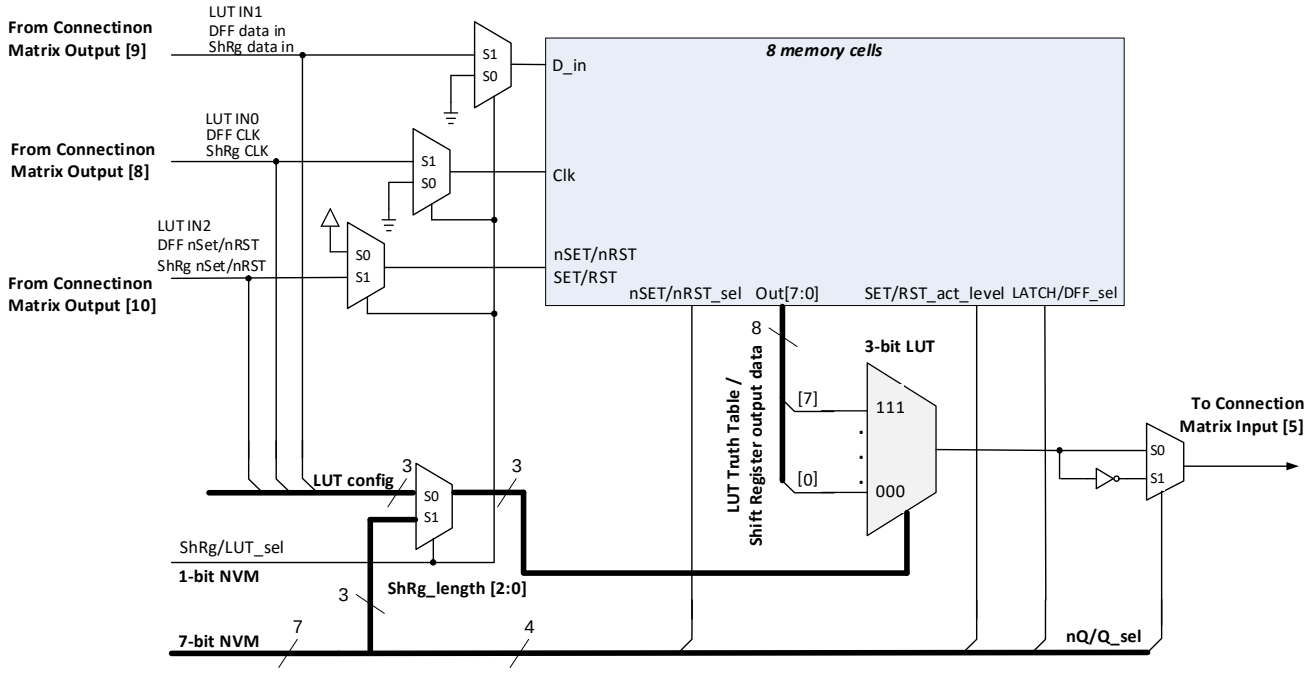


Figure 21: 3-bit LUT0 or DFF3 or Shift Register 3

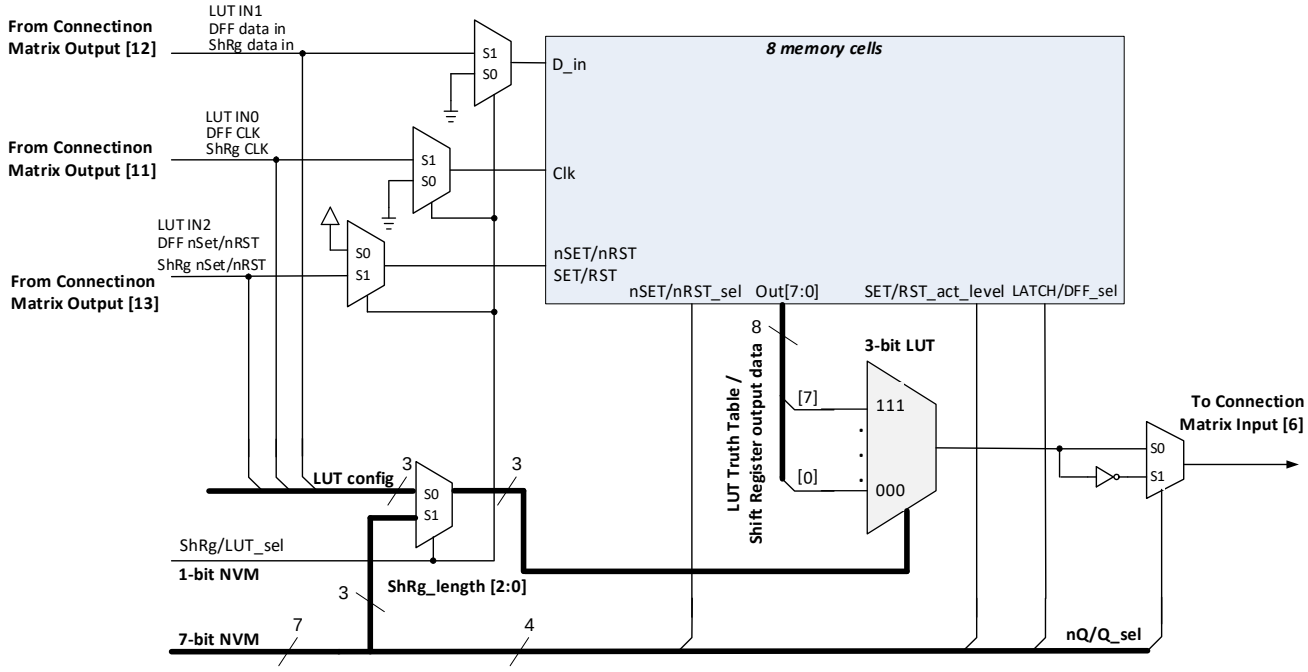


Figure 22: 3-bit LUT1 or DFF4 or Shift Register 4

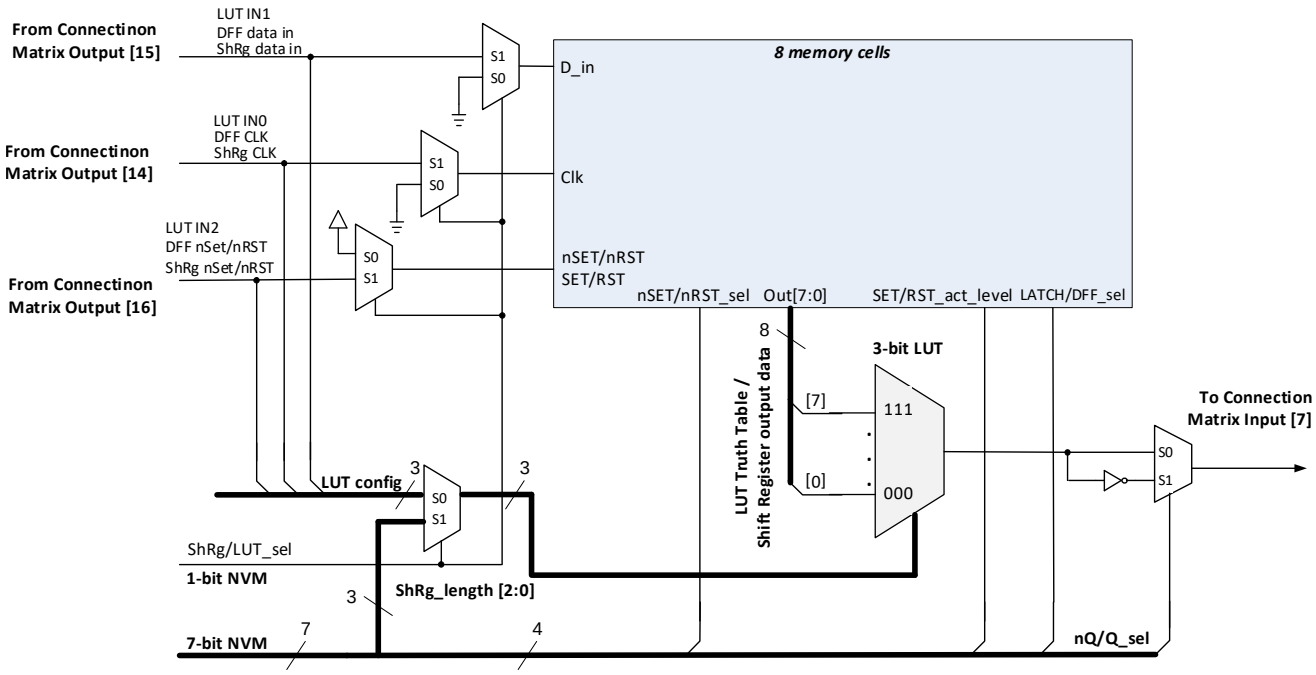


Figure 23: 3-bit LUT2 or DFF5 or Shift Register 5

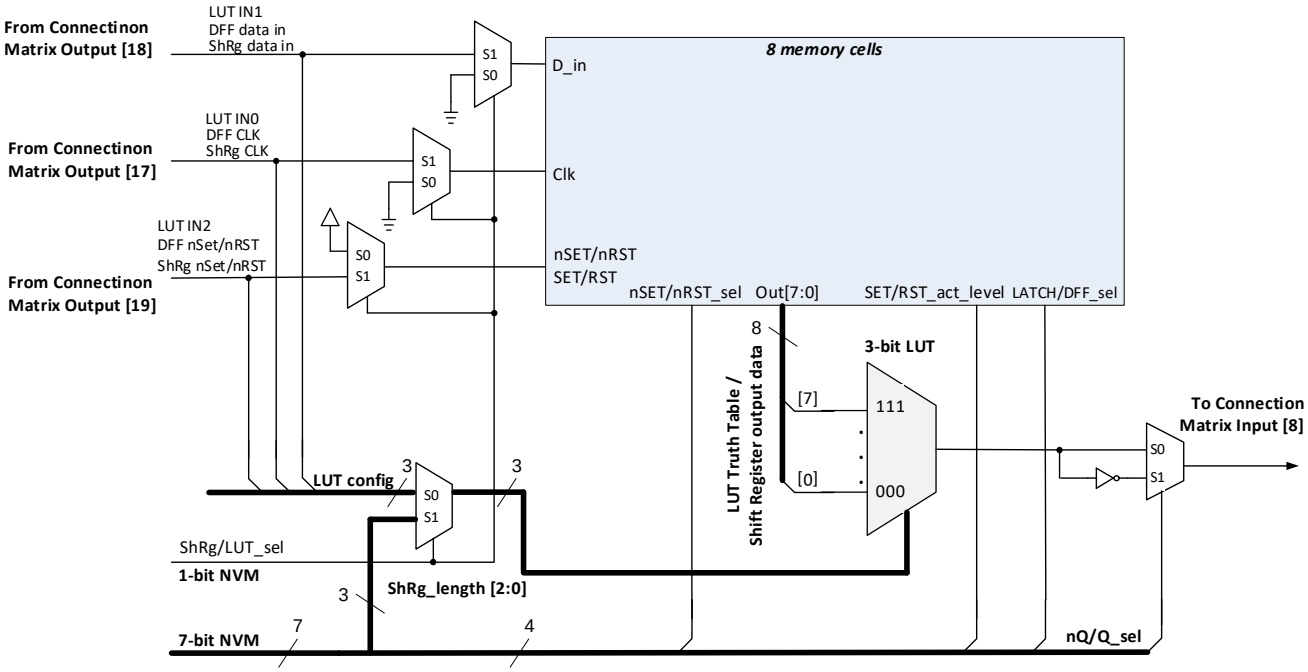


Figure 24: 3-bit LUT3 or DFF6 or Shift Register 6

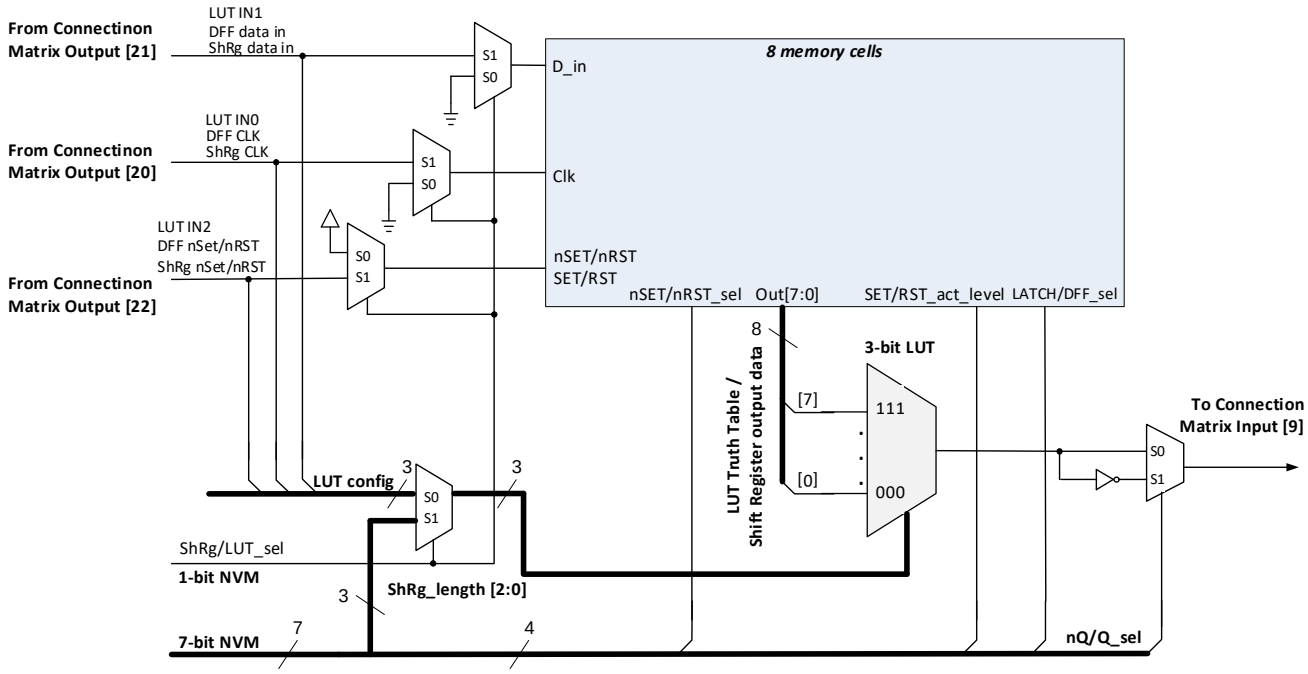


Figure 25: 3-bit LUT4 or DFF7 or Shift Register 7

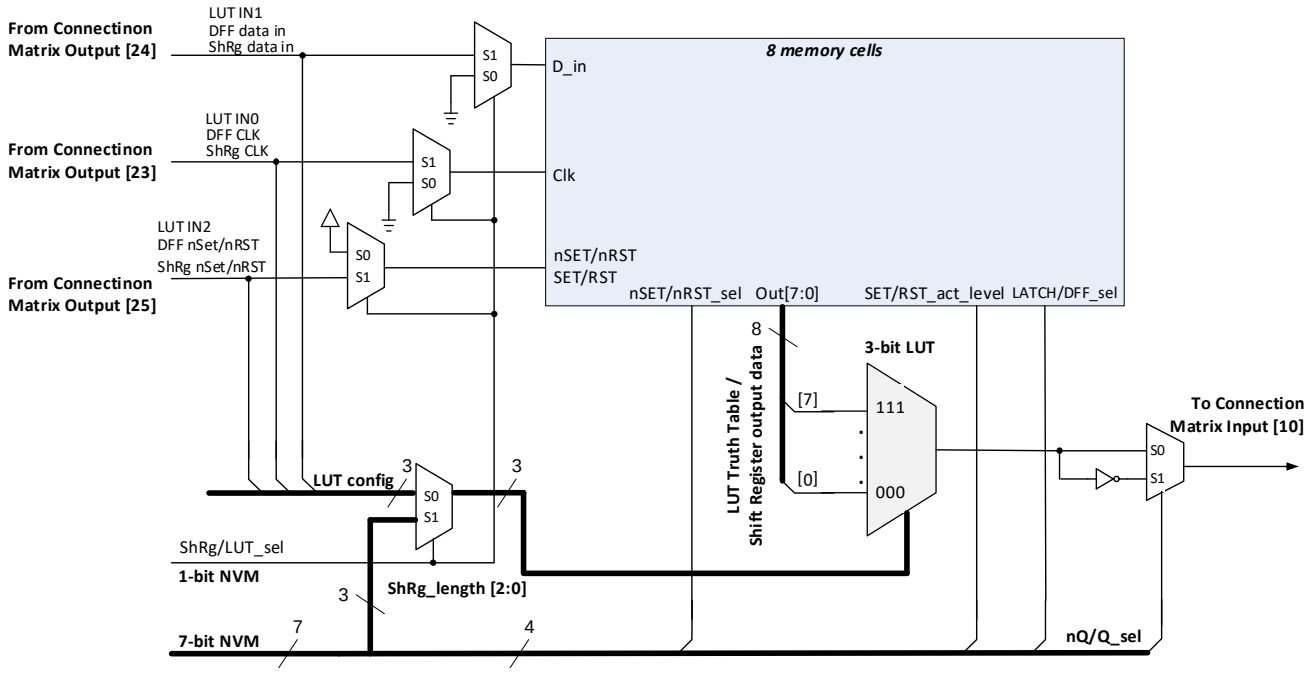


Figure 26: 3-bit LUT5 or DFF8 or Shift Register 8

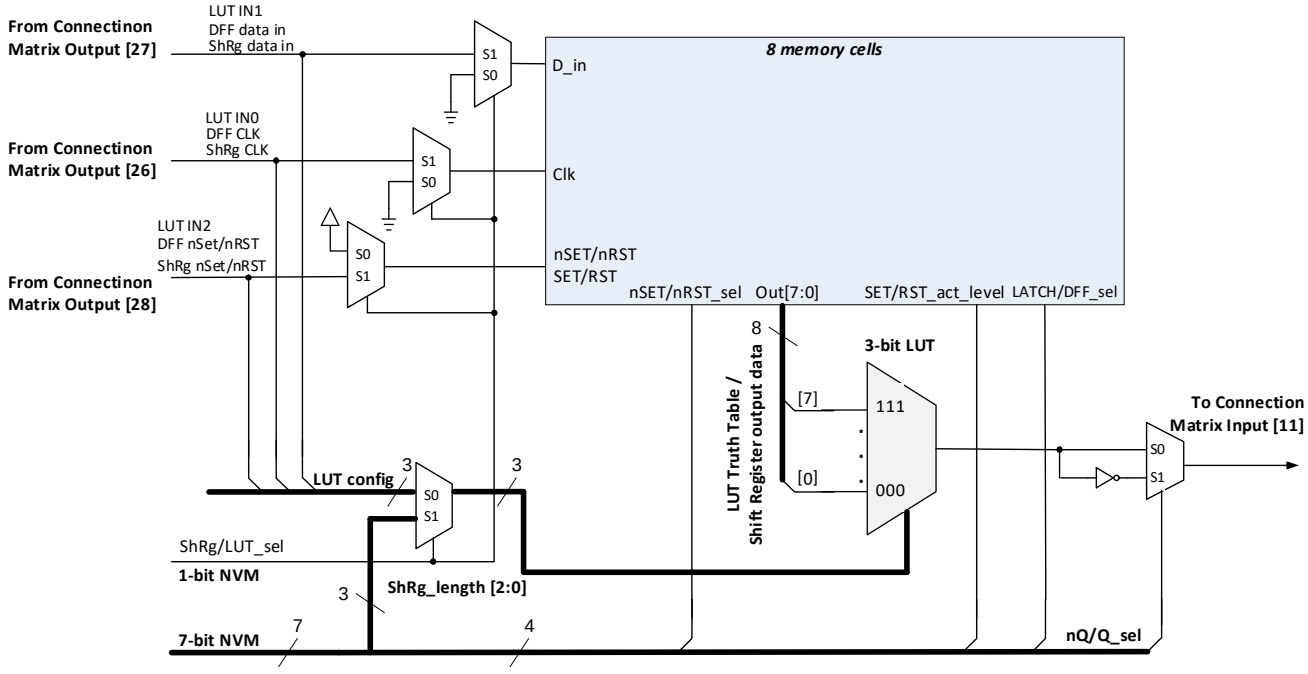


Figure 27: 3-bit LUT6 or DFF9 or Shift Register 9

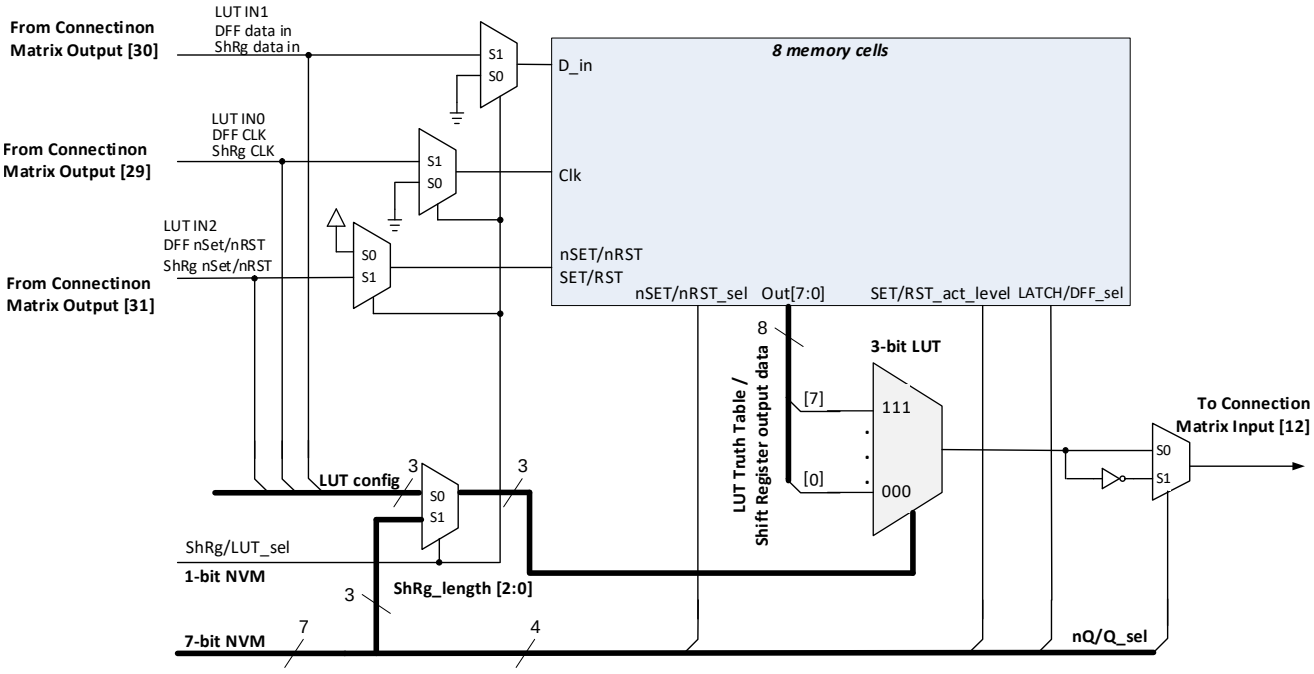


Figure 28: 3-bit LUT7 or DFF10 or Shift Register 10

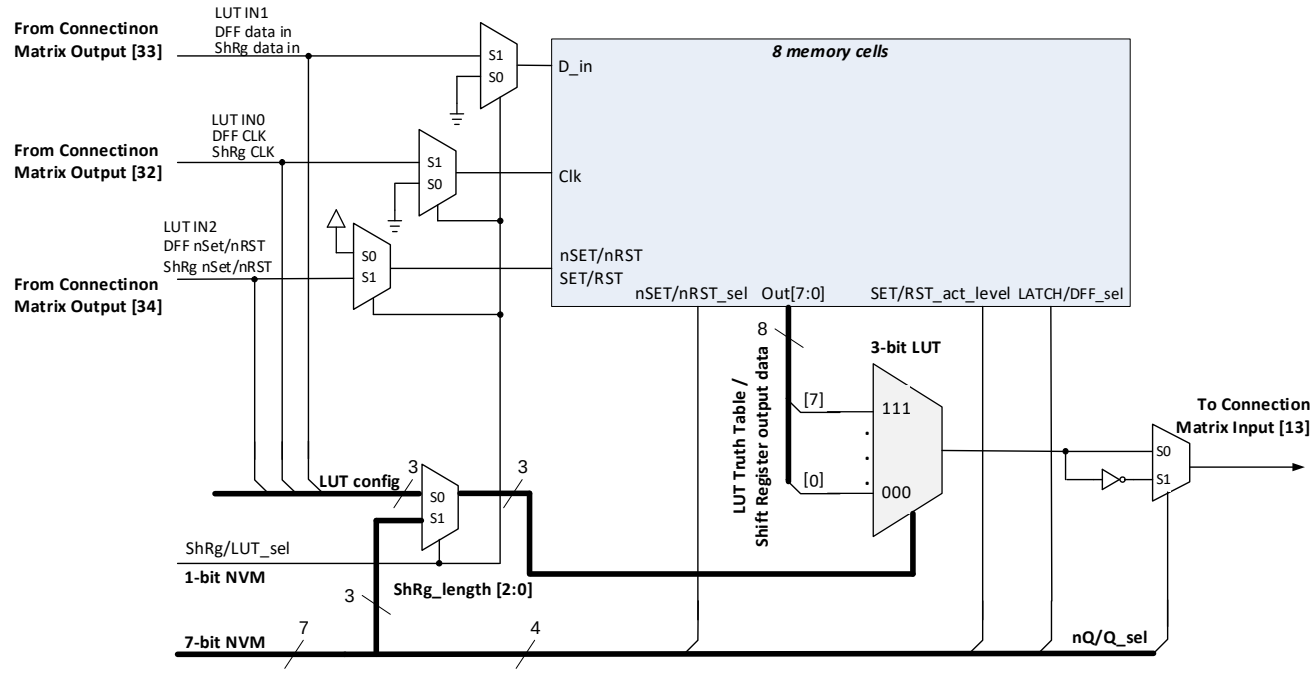


Figure 29: 3-bit LUT8 or DFF11 or Shift Register 11

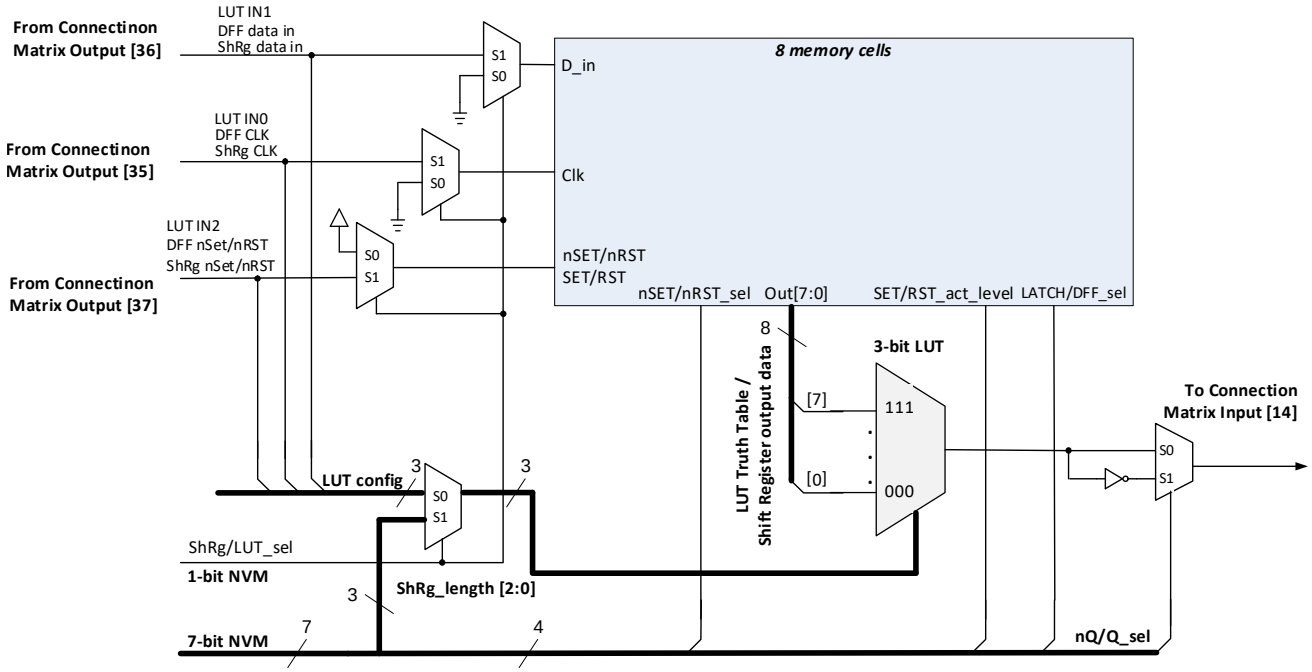
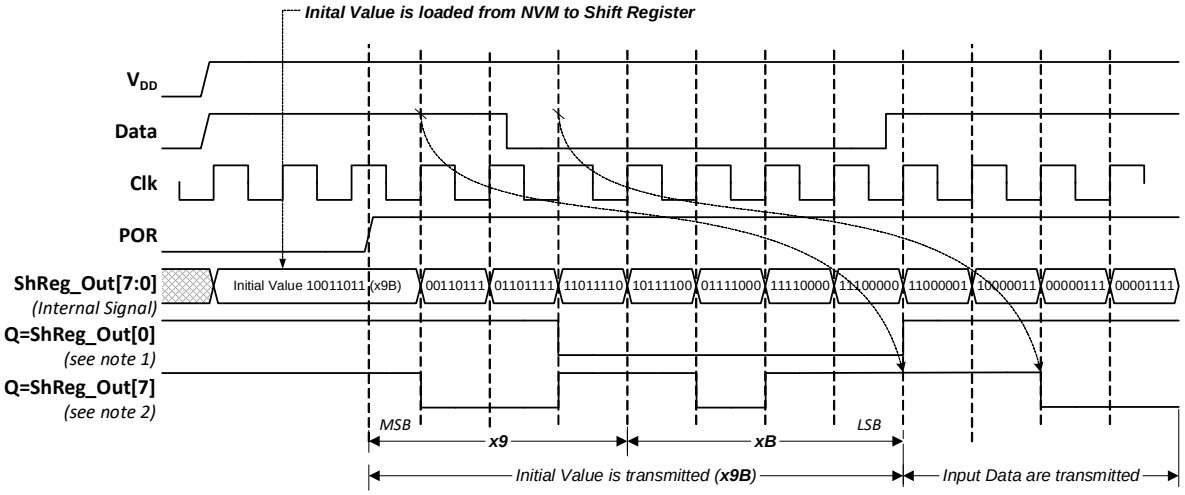
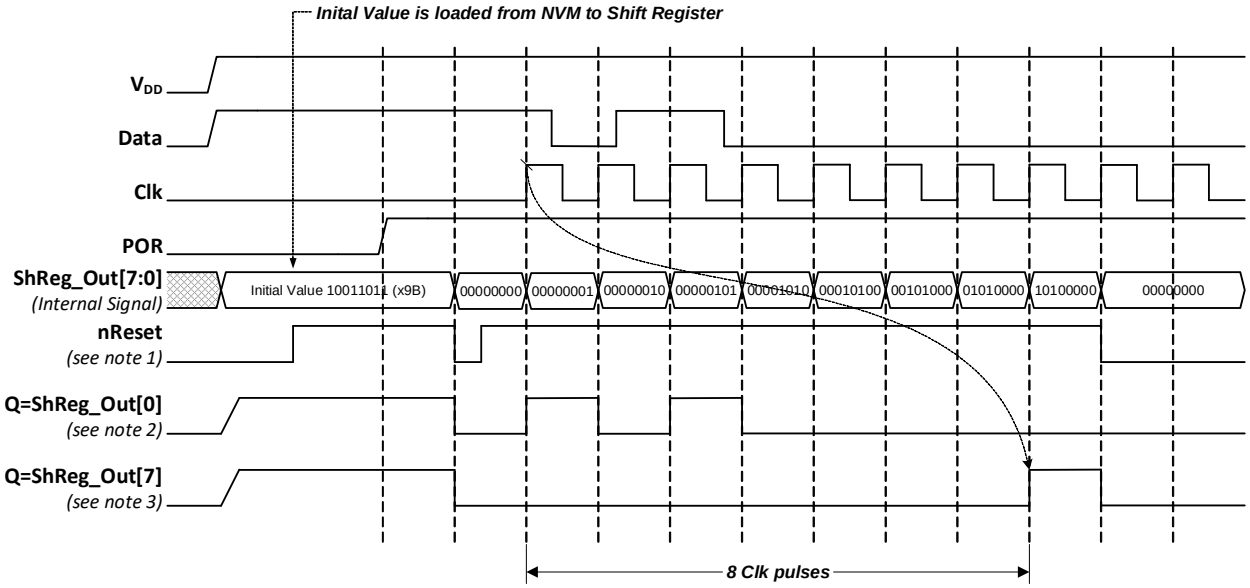


Figure 30: 3-bit LUT9 or DFF12 or Shift Register 12



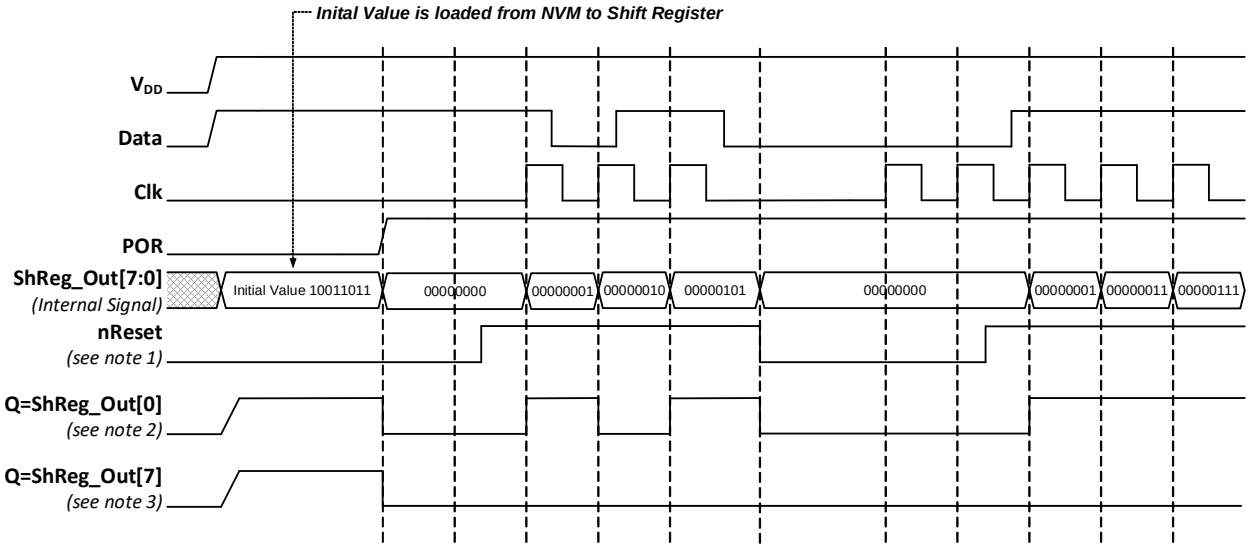
***Note1** : Macrocell is configured as DFF*
***Note2** : Macrocell is configured as 8-bit Shift Register*

Figure 31: DFF3 to DFF12 and Shift Register 3 to Shift Register 12 Operation



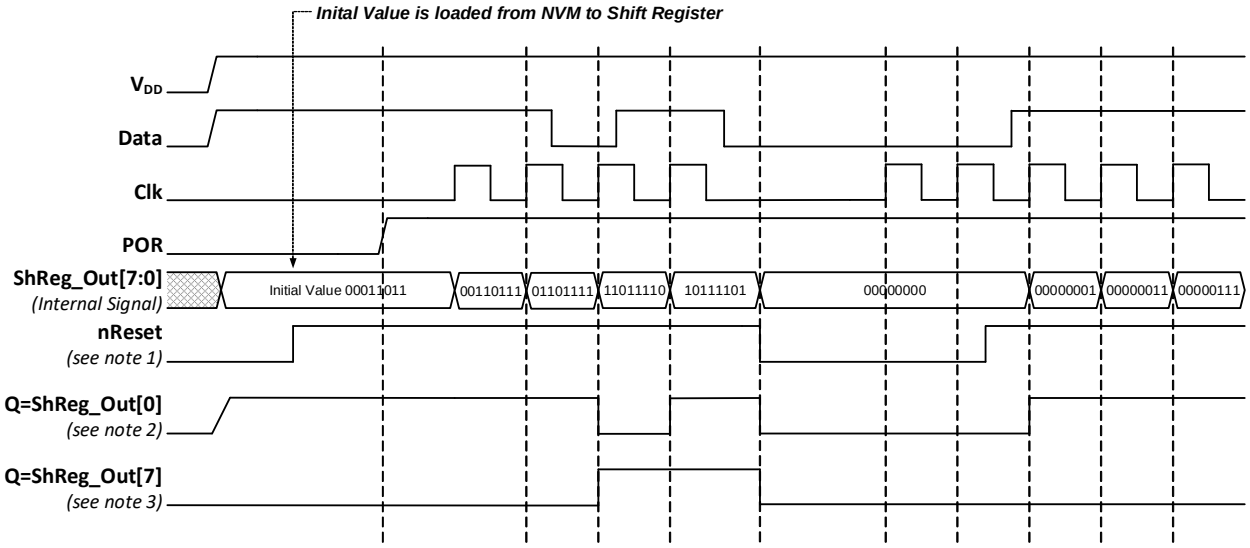
Note1 *: DFF Setting "Initial Value: 1"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 32: DFF3 to DFF12 and Shift Register 3 to Shift Register 12 Operation, nReset, Initial Value: b10011011



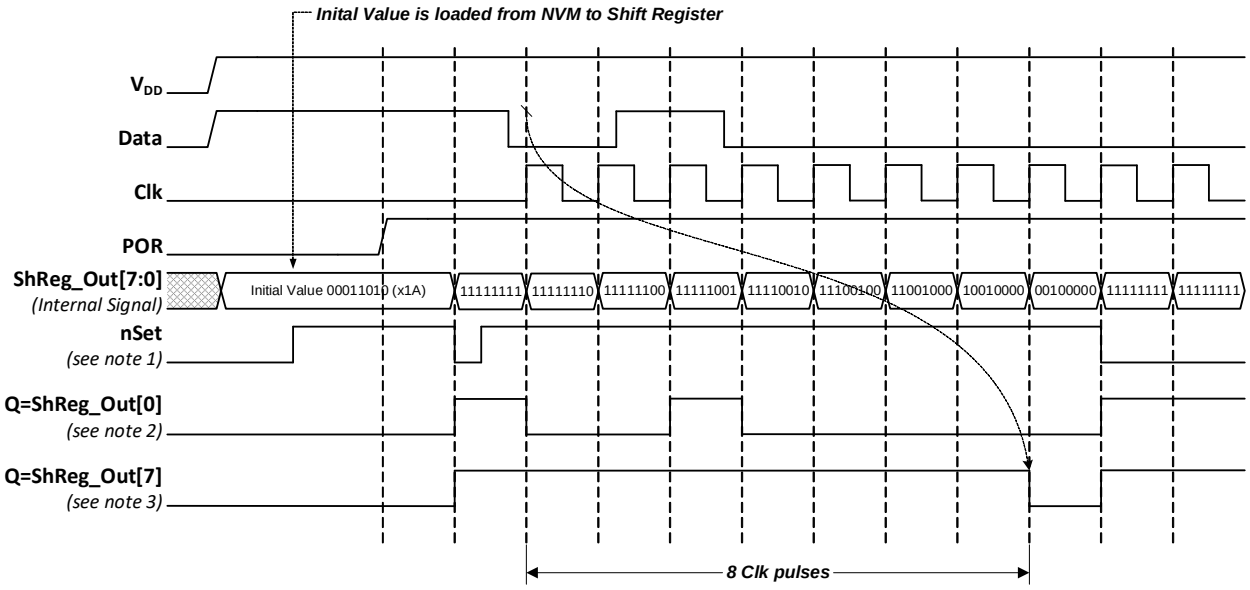
Note1 *: DFF Setting "Initial Value: 1"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 33: DFF3 to DFF12 and Shift Register3 to Shift Register12 Operation, nReset, Initial Value: b10011011, Case2



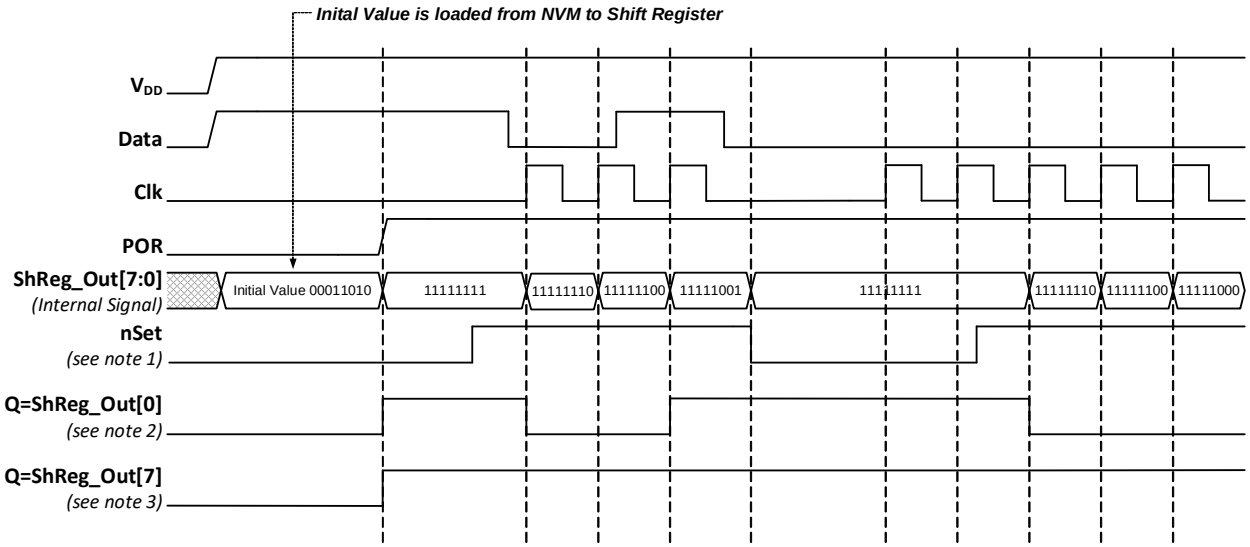
Note1 *: DFF Setting "Initial Value: 1"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 34: DFF3 to DFF12 and Shift Register 3 to Shift Register 12 Operation, nReset, Initial Value: b00011011



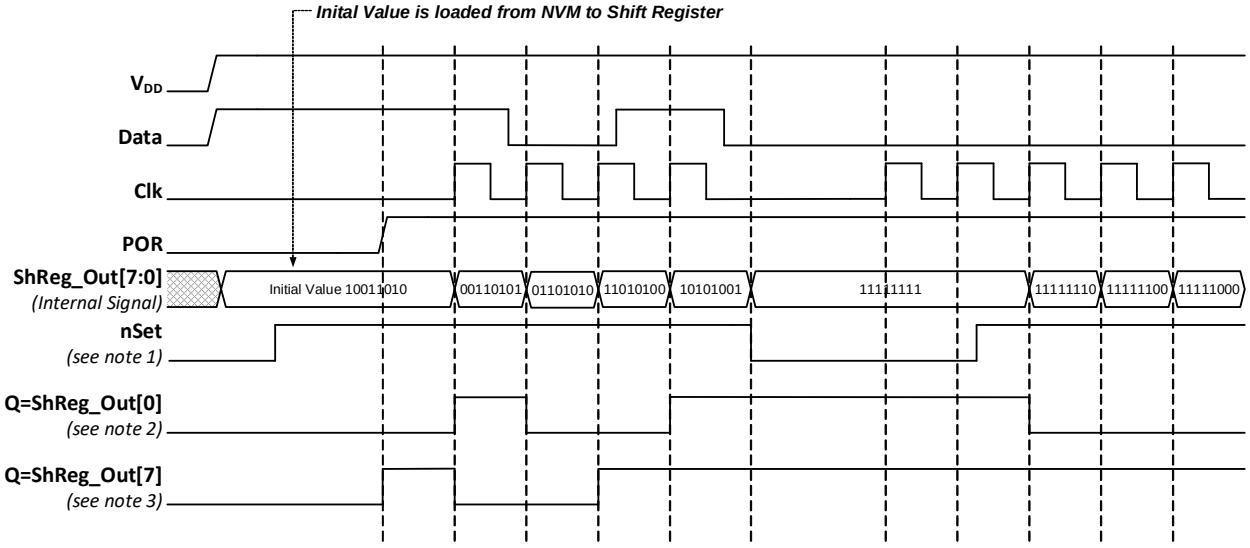
Note1 *: DFF Setting "Initial Value: 0"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 35: DFF3 to DFF12 and Shift Register 3 to Shift Register 12 Operation, nSet, Initial Value: b00011010



Note1 *: DFF Setting "Initial Value: 0"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 36: DFF3 to DFF12 and Shift Register 3 to Shift Register 12 Operation, nSet, Initial Value: b00011010, Case 2



Note1 *: DFF Setting "Initial Value: 0"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 8-bits*

Figure 37: DFF3 to DFF12 and Shift Register 3 to Shift Register 12 Operation, nSet, Initial Value: b10011010

7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

3-Bit LUT3_0 is defined by registers [655:648]

3-Bit LUT3_1 is defined by registers [663:656]

3-Bit LUT3_2 is defined by registers [671:664]

3-Bit LUT3_3 is defined by registers [679:672]

3-Bit LUT3_4 is defined by registers [687:680]

3-Bit LUT3_5 is defined by registers [695:688]

3-Bit LUT3_6 is defined by registers [703:696]

3-Bit LUT3_7 is defined by registers [711:704]

3-Bit LUT3_8 is defined by registers [719:712]

3-Bit LUT3_9 is defined by registers [727:720]

Table 27: 3-bit LUT3_0 to 3-bit LUT3_9 Truth Table

IN2	IN1	IN0	OUT LUT3_0	OUT LUT3_1	OUT LUT3_2	OUT LUT3_3	OUT LUT3_4	OUT LUT3_5	OUT LUT3_6	OUT LUT3_7	OUT LUT3_8	OUT LUT3_9	
0	0	0	register [648]	register [656]	register [664]	register [672]	register [680]	register [688]	register [696]	register [704]	register [712]	register [720]	LSB
0	0	1	register [649]	register [657]	register [665]	register [673]	register [681]	register [689]	register [697]	register [705]	register [713]	register [721]	
0	1	0	register [650]	register [658]	register [666]	register [674]	register [682]	register [690]	register [698]	register [706]	register [714]	register [722]	
0	1	1	register [651]	register [659]	register [667]	register [675]	register [683]	register [691]	register [699]	register [707]	register [715]	register [723]	
1	0	0	register [652]	register [660]	register [668]	register [676]	register [684]	register [692]	register [700]	register [708]	register [716]	register [724]	
1	0	1	register [653]	register [661]	register [669]	register [677]	register [685]	register [693]	register [701]	register [709]	register [717]	register [725]	
1	1	0	register [654]	register [662]	register [670]	register [678]	register [686]	register [694]	register [702]	register [710]	register [718]	register [726]	
1	1	1	register [655]	register [663]	register [671]	register [679]	register [687]	register [695]	register [703]	register [711]	register [719]	register [727]	MSB

Table 28 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 28: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0

Table 28: 3-bit LUT Standard Digital Functions (Continued)

Function	MSB							LSB
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.4 4-BIT LUT OR D FLIP-FLOP WITH SET/RESET OR SHIFT REGISTER MACROCELL

There is one macrocell that can serve as 4-bit LUT or as DFF/LATCH, or as Shift Register. It is also possible to define the active level (Q or nQ) for the macrocell's output by register [847]. DFF/Shift Register or LUT are selected by register [841]. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used to implement Shift Register, the four input signals from the connection matrix go to the data (D_in), clock (CLK), clock enable (CLK_enable), and Set/Reset (nSET/nRST) inputs for the Shift Register, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of Shift Register macrocell which is selected by register [849]. The input data (D_in) writes into LSB. The Shift Register length (up to 16 bits/memory cells) is selected by register [845:842]. Register [845:842] = 0 means that DFF/LATCH function is selected.

When used to implement D Flip-Flop function, the four input signals from the connection matrix go to the data (D_in), clock (CLK), clock enable (CLK_enable), and Set/Reset (nSET/nRST) inputs for the Flip-Flop, with the output going back to the connection matrix. Macrocell in LATCH configuration have three input signals: data (D_in), clock (CLK), and Set/Reset (nSET/nRST). It is possible to define the active level for the reset/set input (nSET/nRST_sel which are selected by register [848]) of DFF/LATCH macrocell. LATCH or DFF configuration is selected by register [846].

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change. When clock enable (CLK_enable) is low, macrocell doesn't react to any pulses at clock (CLK) input.

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

It's possible to read/write the Shift Register content via I^2C (bytes 5Bh and 5Ch). See section 15.4.10 for more information.

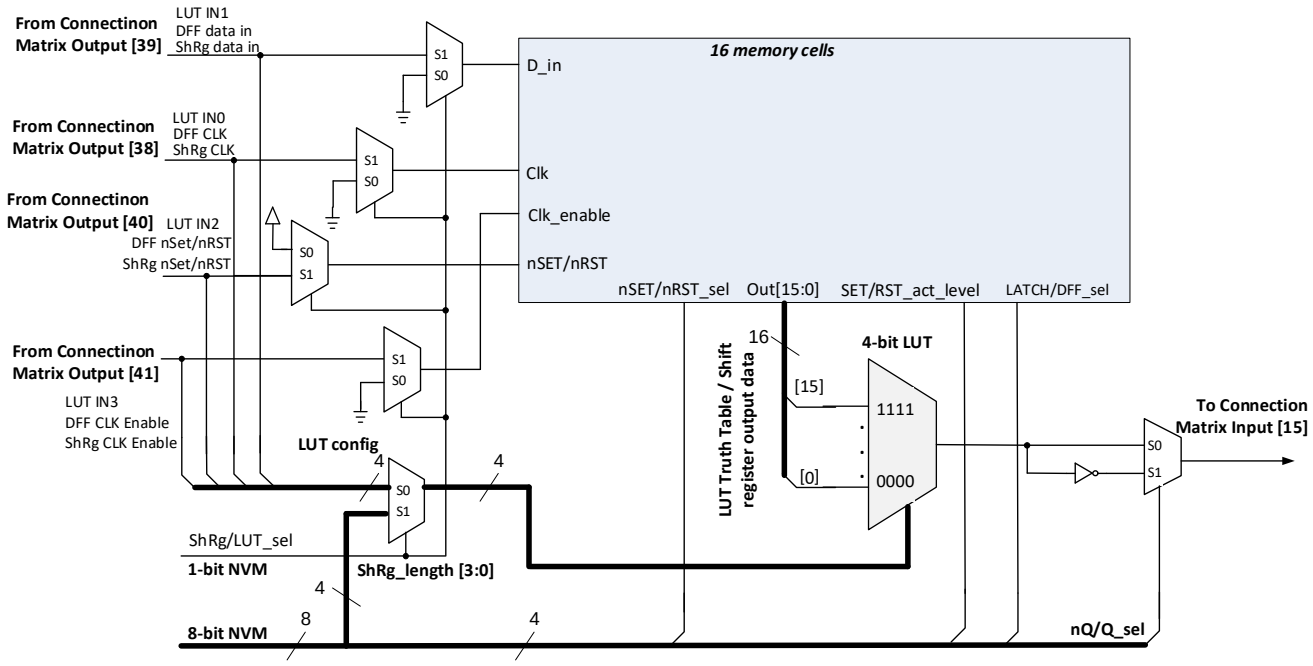
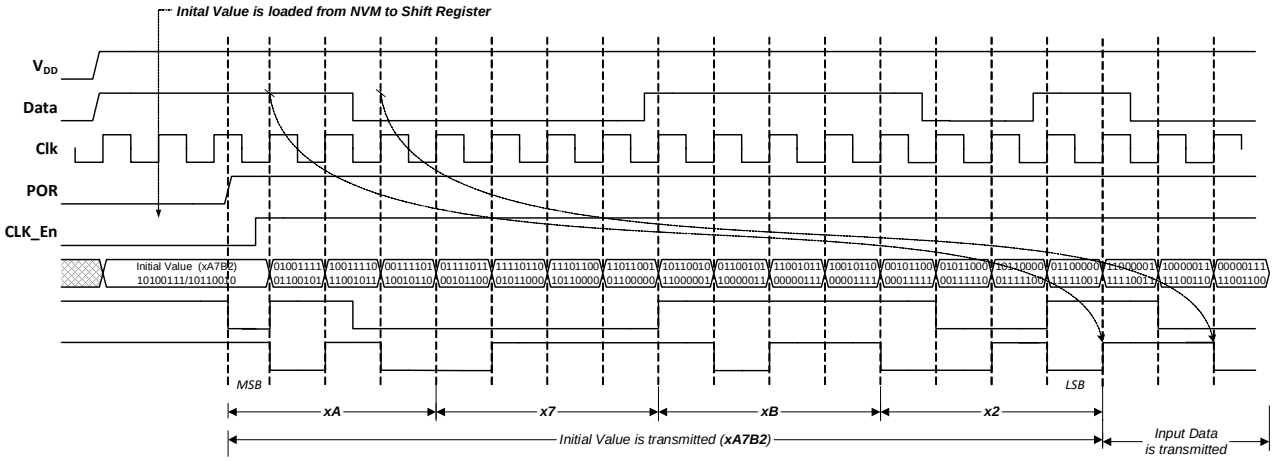
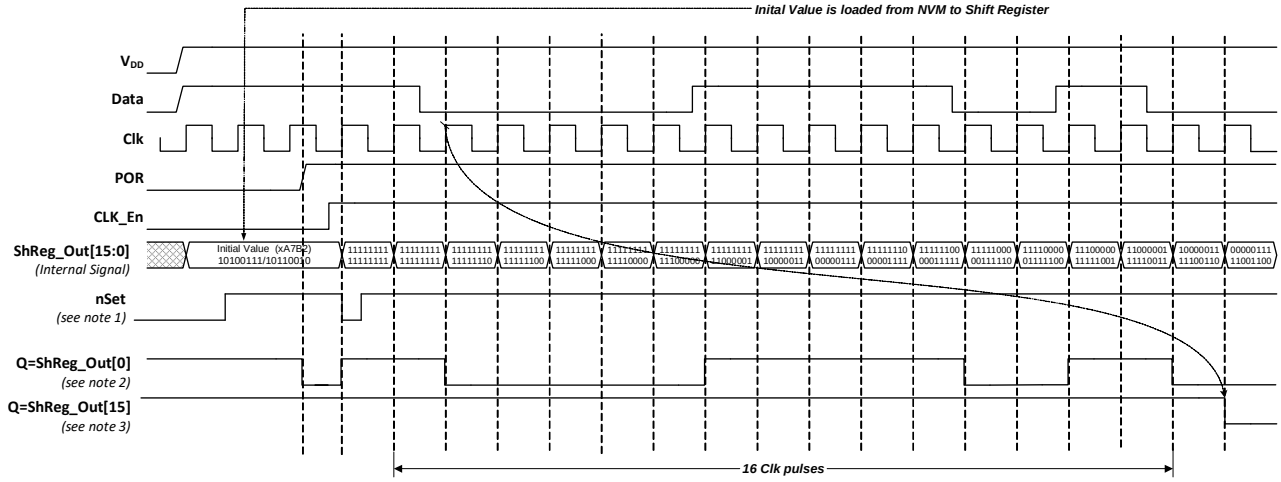


Figure 38: 4-bit LUT0 or DFF13 or Shift Register 13



Note1 *: Macrocell is configured as DFF*
Note2 *: Macrocell is configured as 16-bit Shift Register*

Figure 39: DFF13 and Shift Register 13 Operation



Note1 *: DFF Setting "Initial Value: 0"*
Note2 *: Macrocell is configured as DFF*
Note3 *: Macrocell is configured as 16-bits ShReg*

Figure 40: DFF13 and Shift Register 13 Operation, nSet, Initial Value: xA7B2

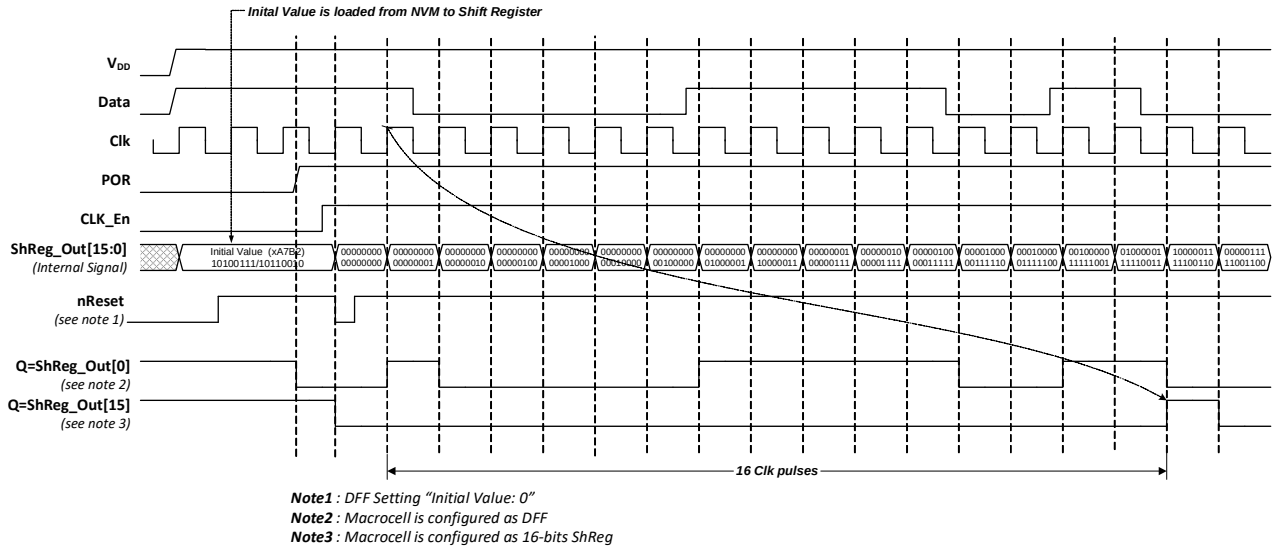


Figure 41: DFF13 and Shift Register 13 Operation, nReset, Initial Value: xA7B2

7.4.1 4-Bit LUT Macrocell Used as 4-Bit LUT

Table 29: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [728]	LSB
0	0	0	1	register [729]	
0	0	1	0	register [730]	
0	0	1	1	register [731]	
0	1	0	0	register [732]	
0	1	0	1	register [733]	
0	1	1	0	register [734]	
0	1	1	1	register [735]	
1	0	0	0	register [736]	
1	0	0	1	register [737]	
1	0	1	0	register [738]	
1	0	1	1	register [739]	
1	1	0	0	register [740]	
1	1	0	1	register [741]	
1	1	1	0	register [742]	
1	1	1	1	register [743]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by registers [743:728]

Table 30: 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

8 Multi-Function Macrocells

The SLG47512/13 has 8 Multi-Function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 42.

See the list below for the functions that can be implemented in these macrocells:

- Seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays
- One macrocell that can serve as a 4-bit LUT/D Flip-Flop and as 16-Bit Counter/Delay/FSM

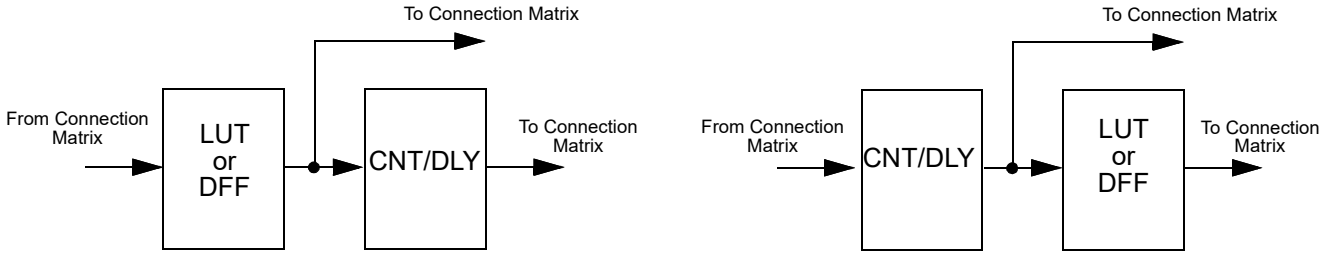


Figure 42: Possible Connections Inside Multi-Function Macrocell

Inputs/Outputs for the 8 Multi-Function function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 3-BIT LUT OR DFF/LATCH WITH 8-BIT COUNTER/DELAY MACROCELLS

There are seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Set/Reset (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

LATCH: when CLK is High, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is Low).

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which define its initial value after GPAK is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to sections 7.1 and 8.3.

Note: After two DFF – counters initialize with counter data = 0 after POR.
Initial state = 1 – counters initialize with counter data = 0 after POR.
Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

CNT6 and CNT7 current count value can be read via I^2C. However, it is possible to change the counter data (value counter starts operating from) for any macrocell using I^2C write commands. In this mode, it is possible to load count data immediately (after two DFF) or after counter ends counting. See Section 15.4.8 for further details.

8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

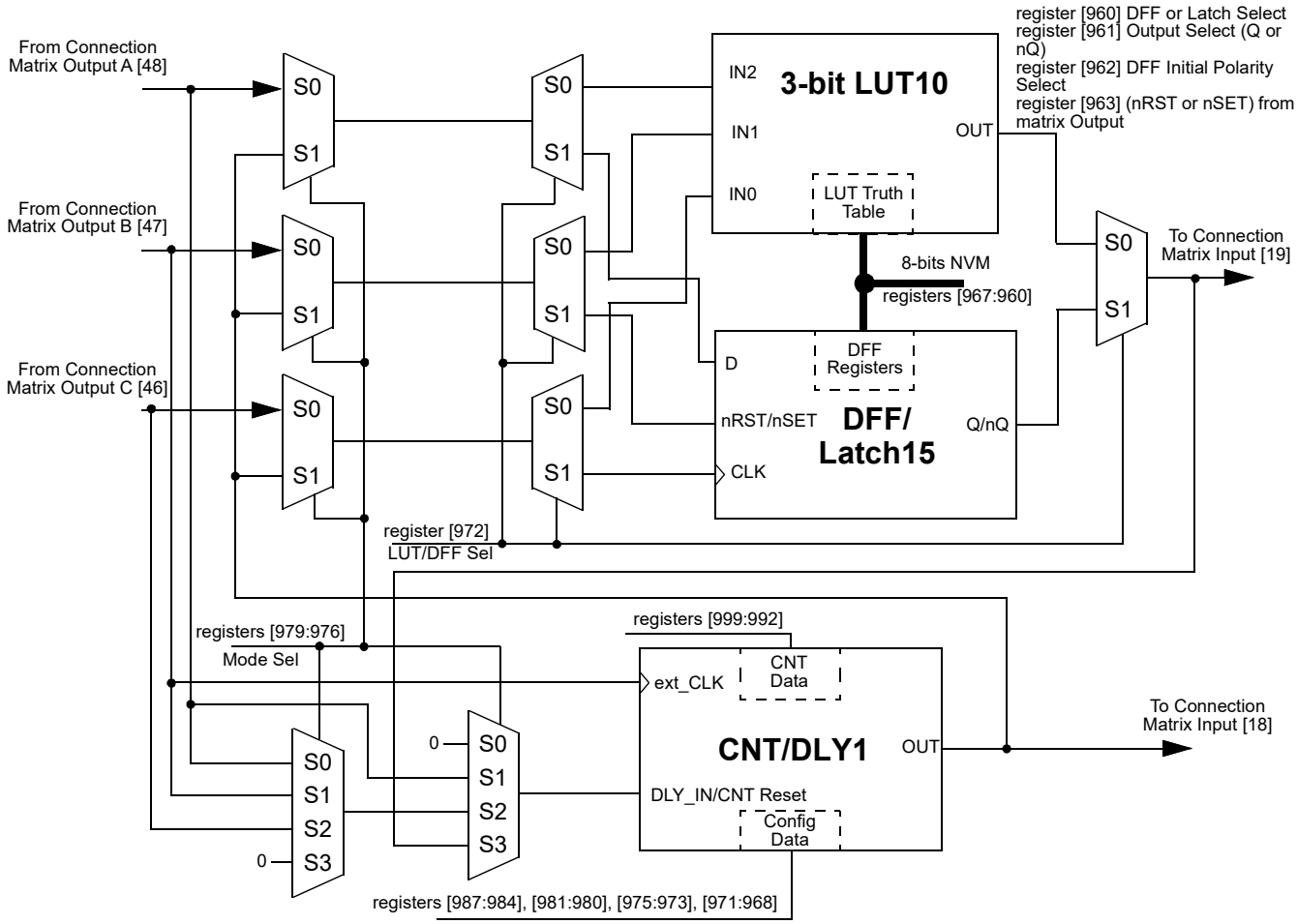


Figure 43: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF15, CNT/DLY1)

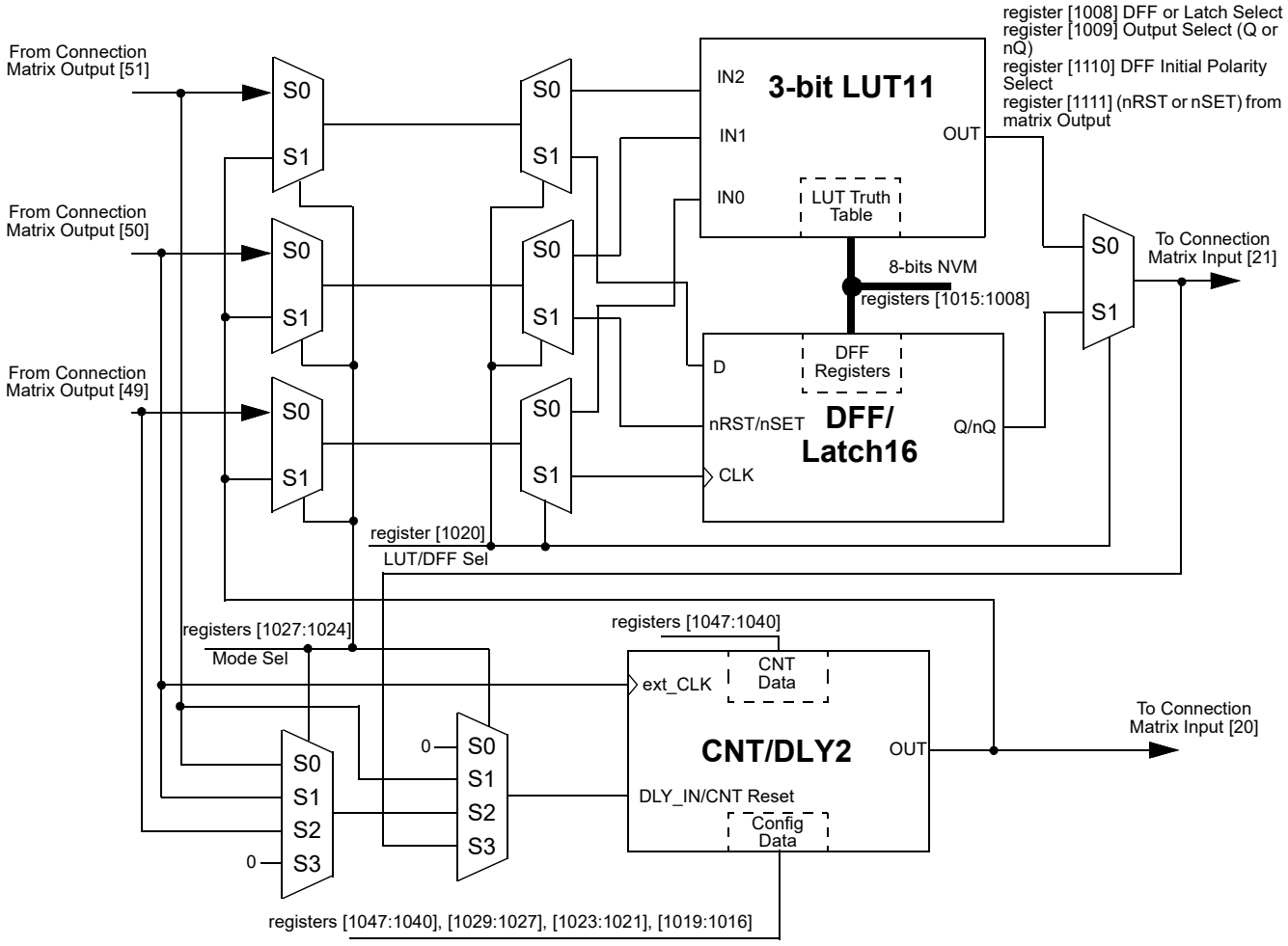


Figure 44: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF16, CNT/DLY2)

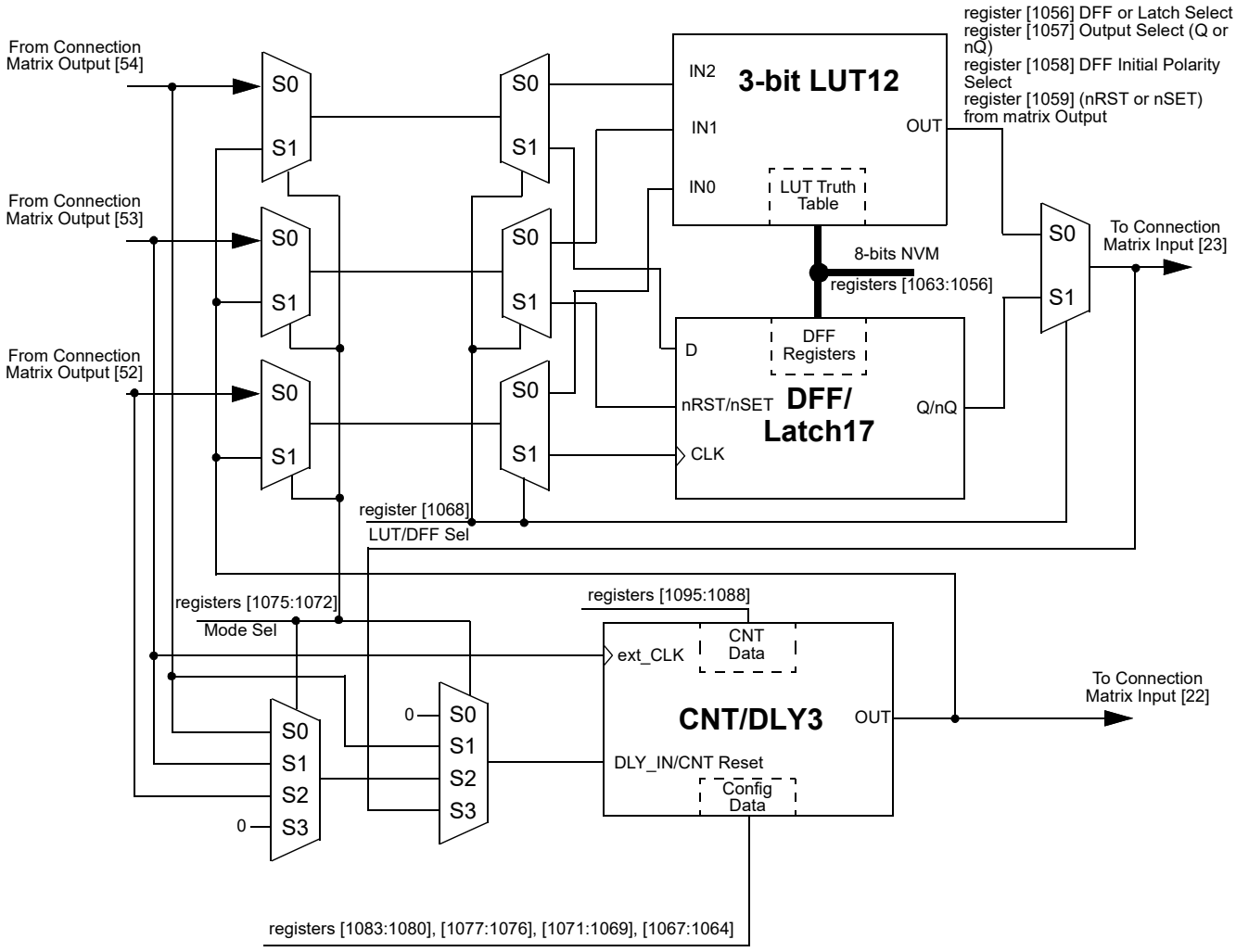


Figure 45: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF17, CNT/DLY3)

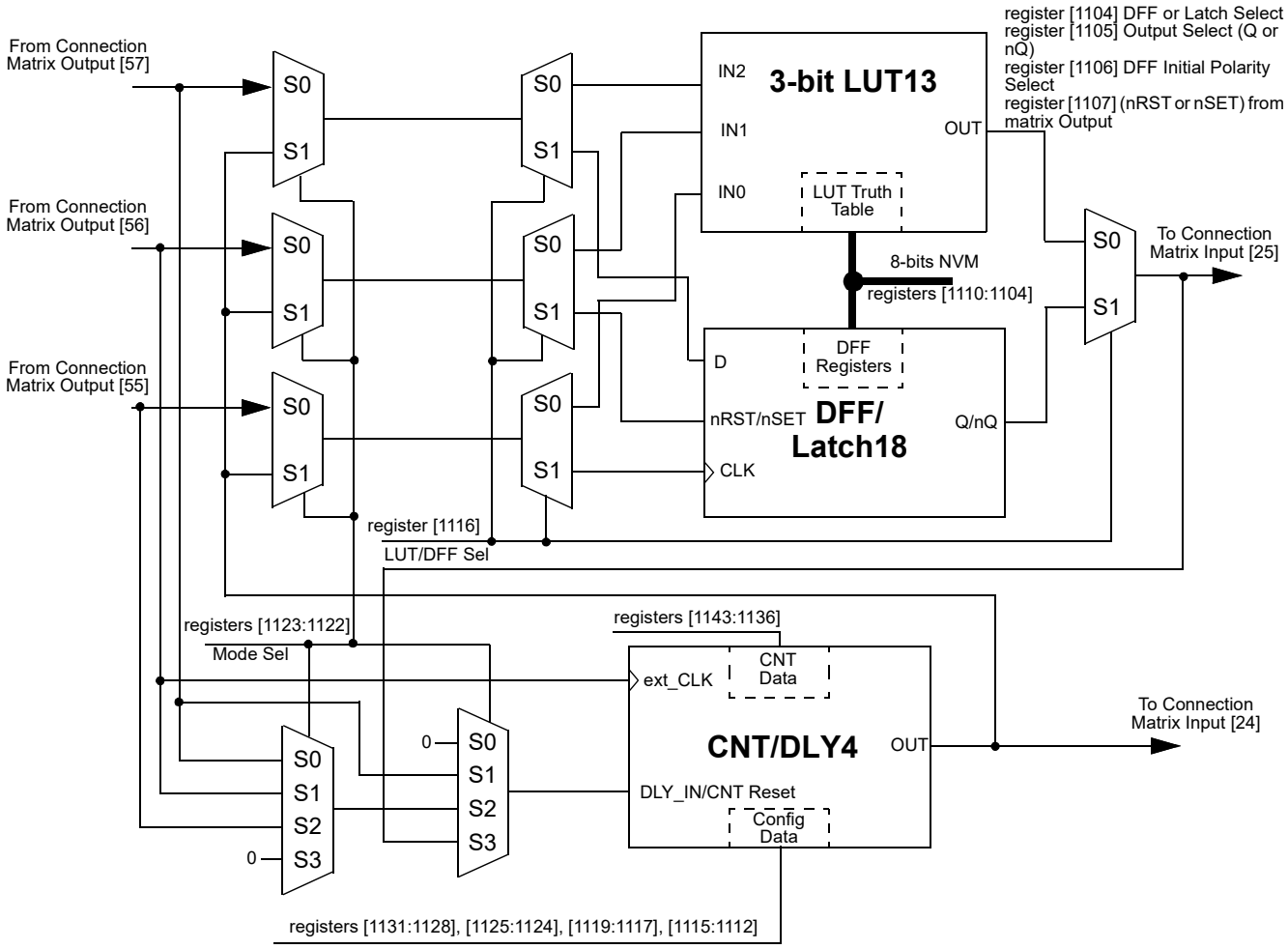


Figure 46: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT13/DFF18, CNT/DLY4)

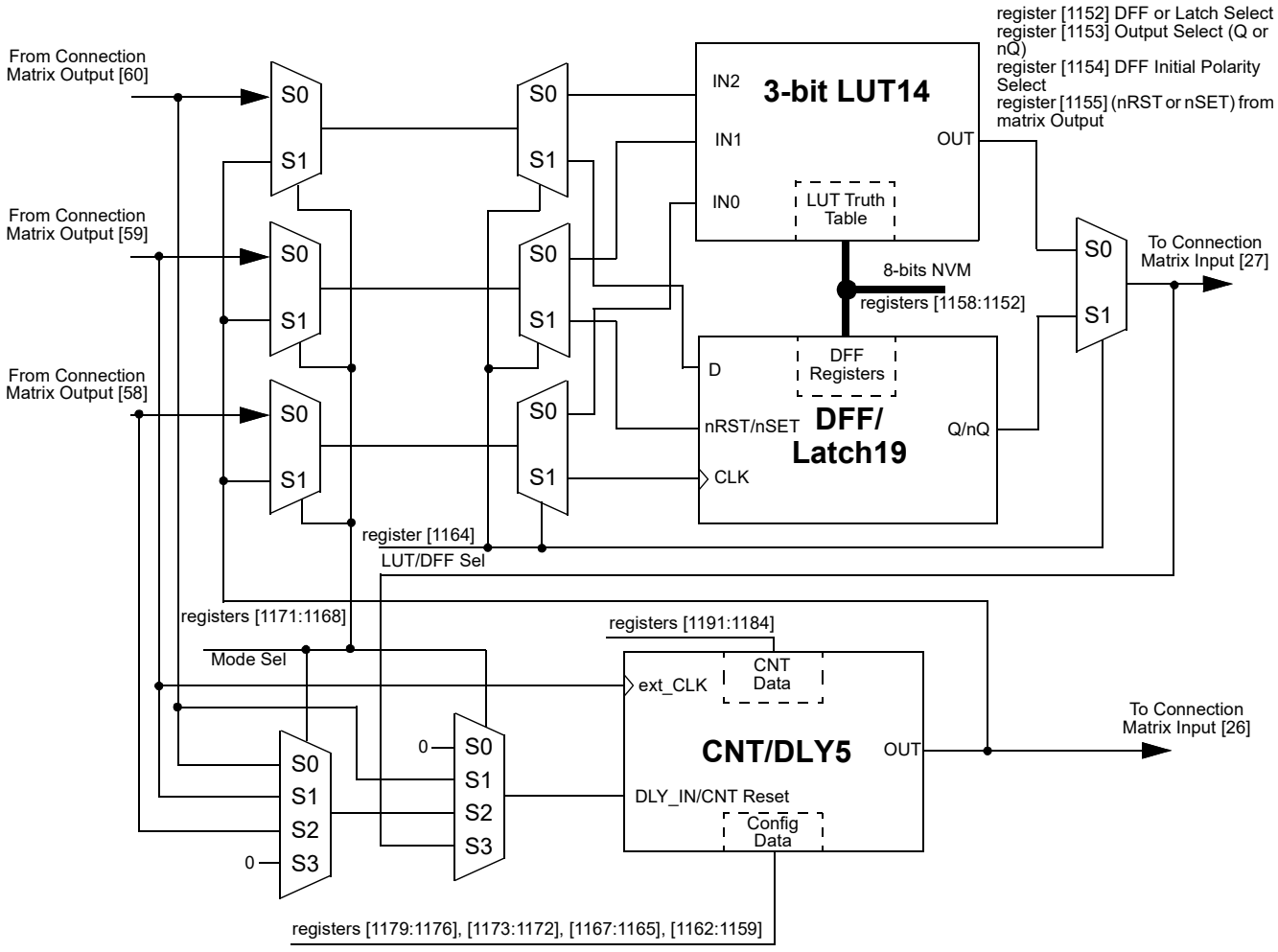


Figure 47: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT14/DFF19, CNT/DLY5)

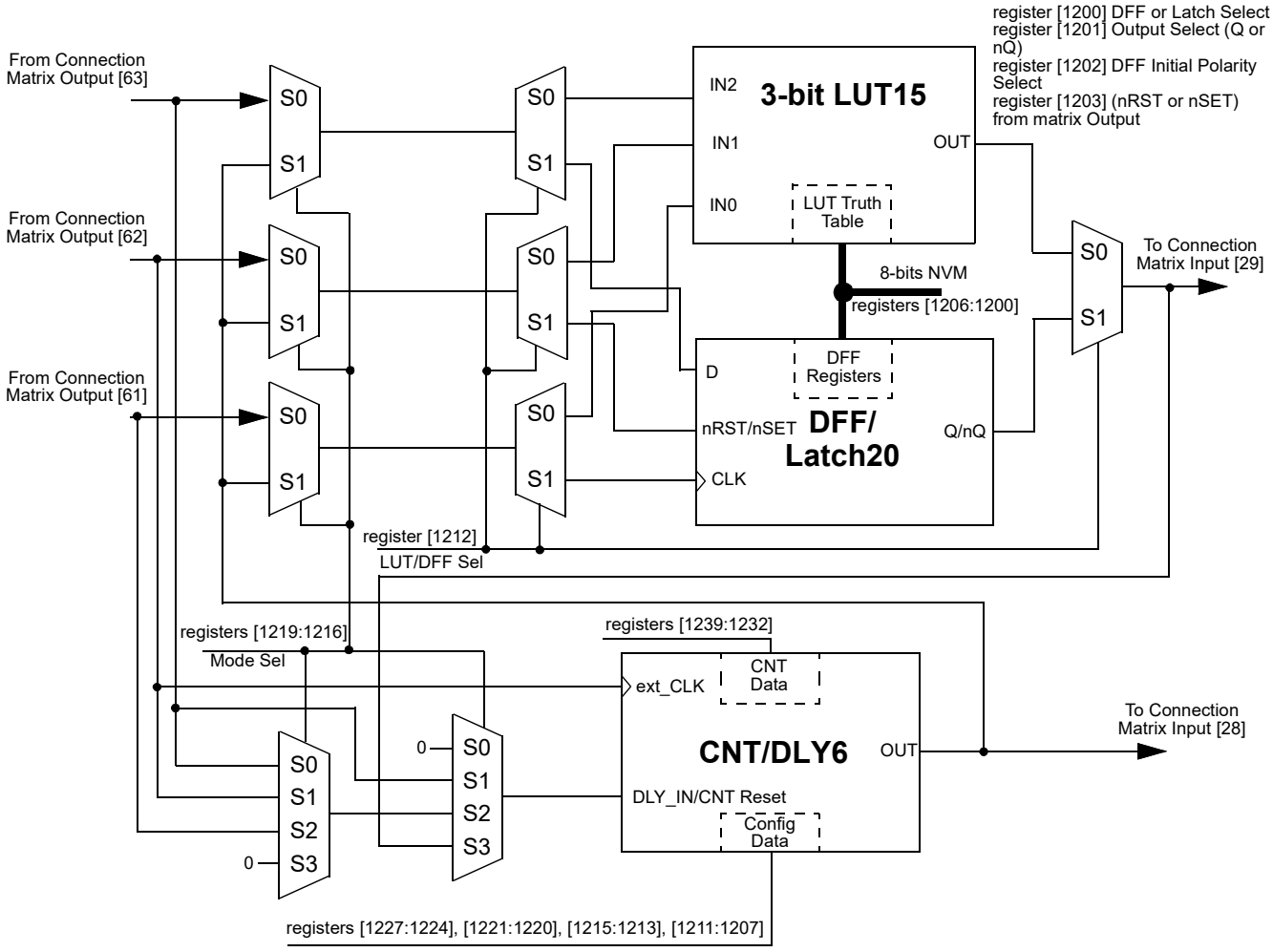


Figure 48: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT15/DFF20, CNT/DLY6)

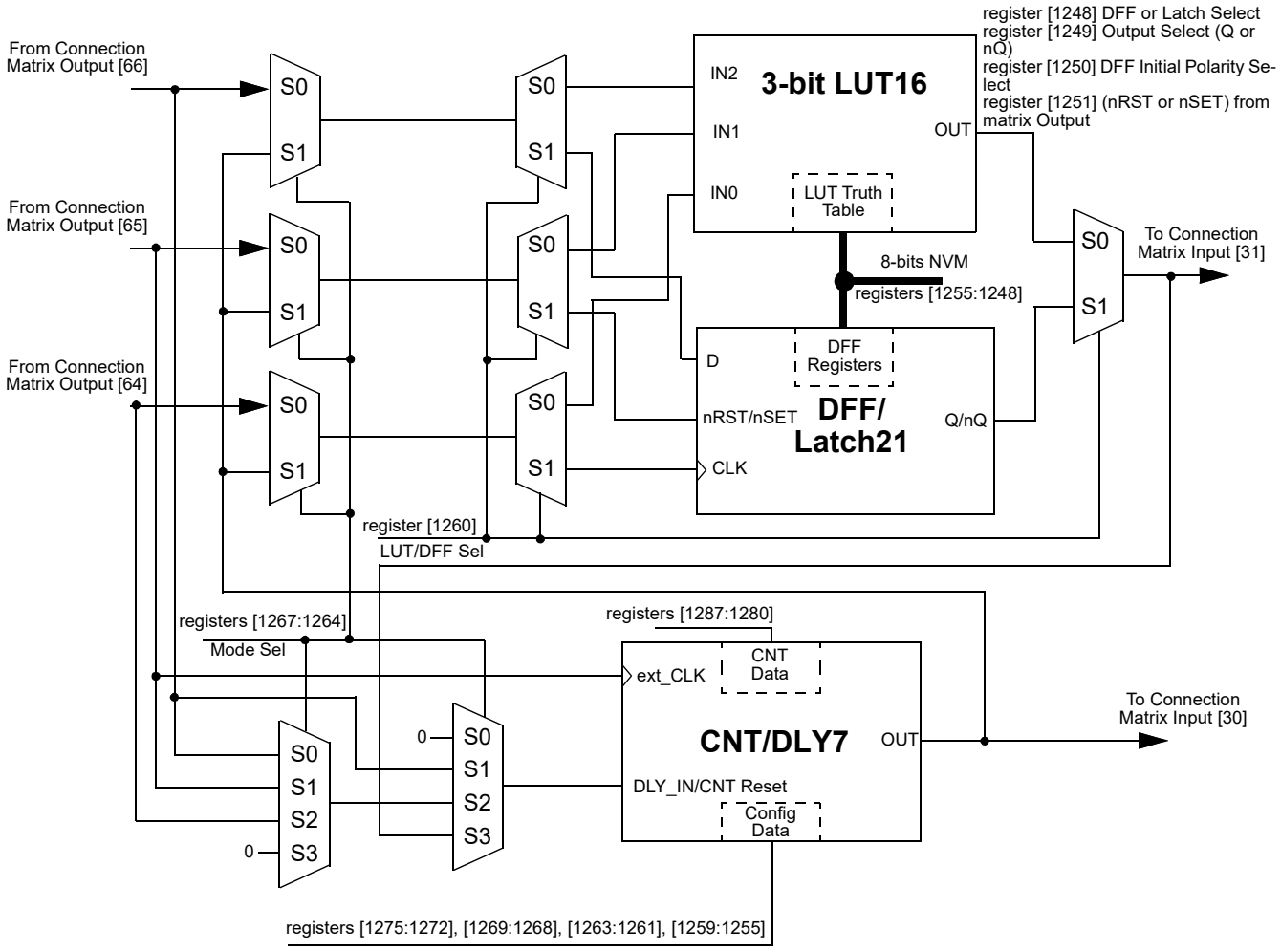


Figure 49: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT16/DFF21, CNT/DLY7)

As shown in Figures 22-28 there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

8.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 31: 3-bit LUT10 to 3-bit LUT16 Truth Table

IN2	IN1	IN0	OUT LUT3_10	OUT LUT3_11	OUT LUT3_12	OUT LUT3_13	OUT LUT3_14	OUT LUT3_15	OUT LUT3_16	
0	0	0	register [960]	register [1008]	register [1056]	register [1104]	register [1152]	register [1200]	register [1248]	LSB
0	0	1	register [961]	register [1009]	register [1057]	register [1105]	register [1153]	register [1201]	register [1249]	
0	1	0	register [962]	register [1010]	register [1058]	register [1106]	register [1154]	register [1202]	register [1250]	
0	1	1	register [963]	register [1011]	register [1059]	register [1107]	register [1155]	register [1203]	register [1251]	
1	0	0	register [964]	register [1012]	register [1060]	register [1108]	register [1156]	register [1204]	register [1252]	
1	0	1	register [965]	register [1013]	register [1061]	register [1109]	register [1157]	register [1205]	register [1253]	
1	1	0	register [966]	register [1014]	register [1062]	register [1110]	register [1158]	register [1206]	register [1254]	
1	1	1	register [967]	register [1015]	register [1063]	register [1111]	register [1159]	register [1207]	register [1255]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

3-Bit LUT10 is defined by registers [967:960]

3-Bit LUT11 is defined by registers [1015:1008]

3-Bit LUT12 is defined by registers [1063:1056]

3-Bit LUT13 is defined by registers [1111:1104]

3-Bit LUT14 is defined by registers [1159:1152]

3-Bit LUT15 is defined by registers [1207:1200]

3-Bit LUT16 is defined by registers [1255:1248]

8.2 4-BIT LUT OR DFF/LATCH WITH 16-BIT COUNTER/DELAY MACROCELL

There is one macrocell that can serve as either 4-bit LUT or as 16-bit Counter/Delay. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 16-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the counter/delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality. FSM has an option to reset its counted value either to 0 or to user defined data.

The behavior of FSM macrocell is described below:

- FSM output Q goes to 1 if counter value reaches 0;
- FSM Set Selection Mode sets the initial counter value to counter data;
- RST Selection Mode sets the initial counter value to 0;
- Counter value reaches maximum and overloads, after that counting starts from 0. Otherwise, in case of counting down from maximum to 0, after overloading counter starts from 65535;

Mode signal synchronization (available for thee inputs) adds two extra clocks to avoid metastability issue.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

This macrocell can also operate in a frequency detection or edge detection mode.

This macrocell can have its active count value read via I^2C. See Section 15.4.8 for further details.

Note: After two DFF – counters initialize with counter data = 0 after POR.
Initial state = 1 – counters initialize with counter data = 0 after POR.
Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

8.2.1 4-Bit LUT or DFF/LATCH with 16-Bit CNT/DLY Block Diagram

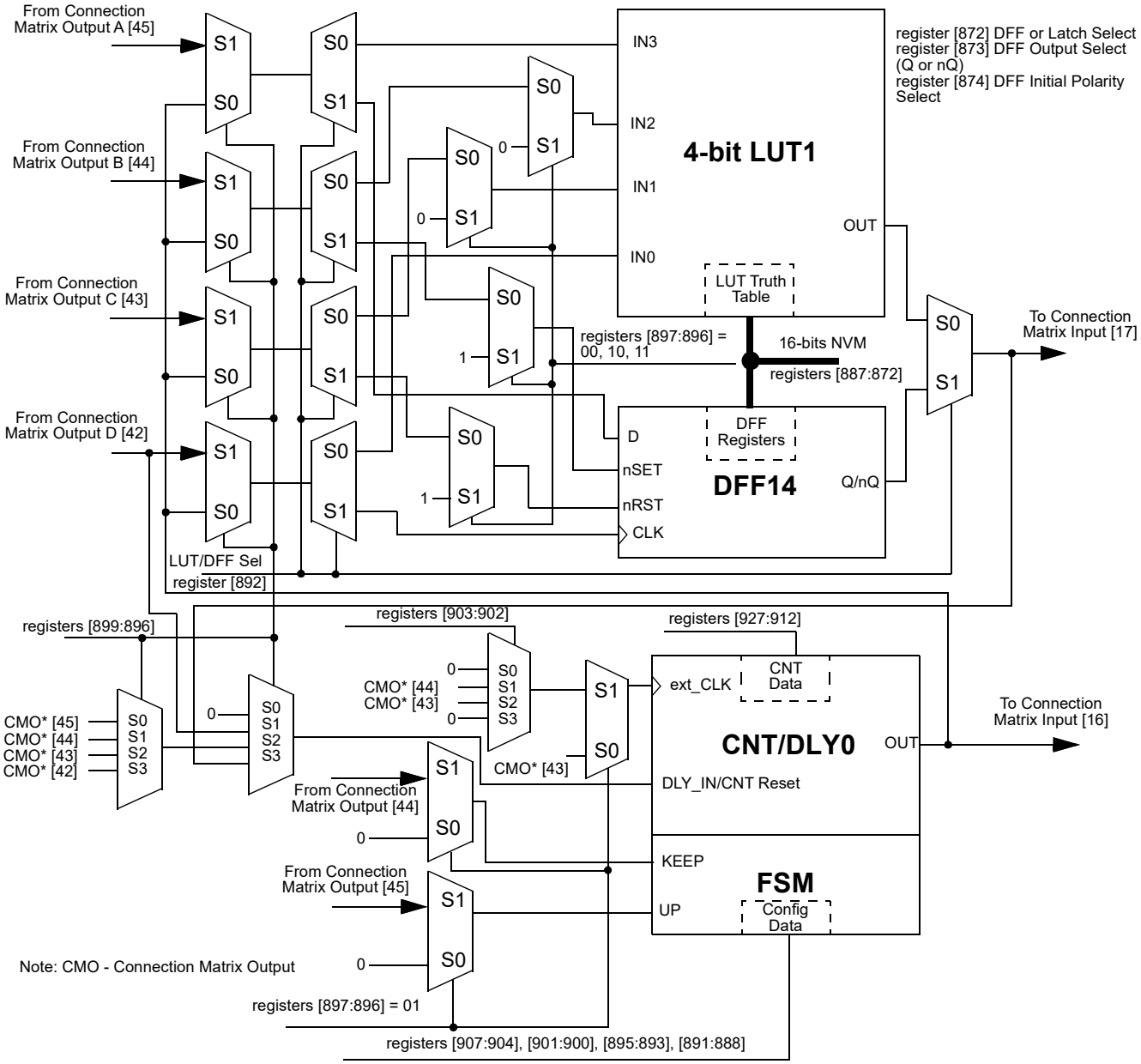


Figure 50: 4-bit LUT1 or CNT/DLY0

8.2.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 32: 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [872]	LSB
0	0	0	1	register [873]	
0	0	1	0	register [874]	
0	0	1	1	register [875]	
0	1	0	0	register [876]	
0	1	0	1	register [877]	
0	1	1	0	register [878]	
0	1	1	1	register [879]	
1	0	0	0	register [880]	
1	0	0	1	register [881]	
1	0	1	0	register [882]	
1	0	1	1	register [883]	
1	1	0	0	register [884]	
1	1	0	1	register [885]	
1	1	1	0	register [886]	
1	1	1	1	register [887]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT1 is defined by registers [887:872]

Table 33: 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

8.3 CNT/DLY TIMING DIAGRAMS

8.3.1 Delay Mode CNT/DLY0 to CNT/DLY7

Delay macrocell can automatically start/stop oscillator (Figure 51).

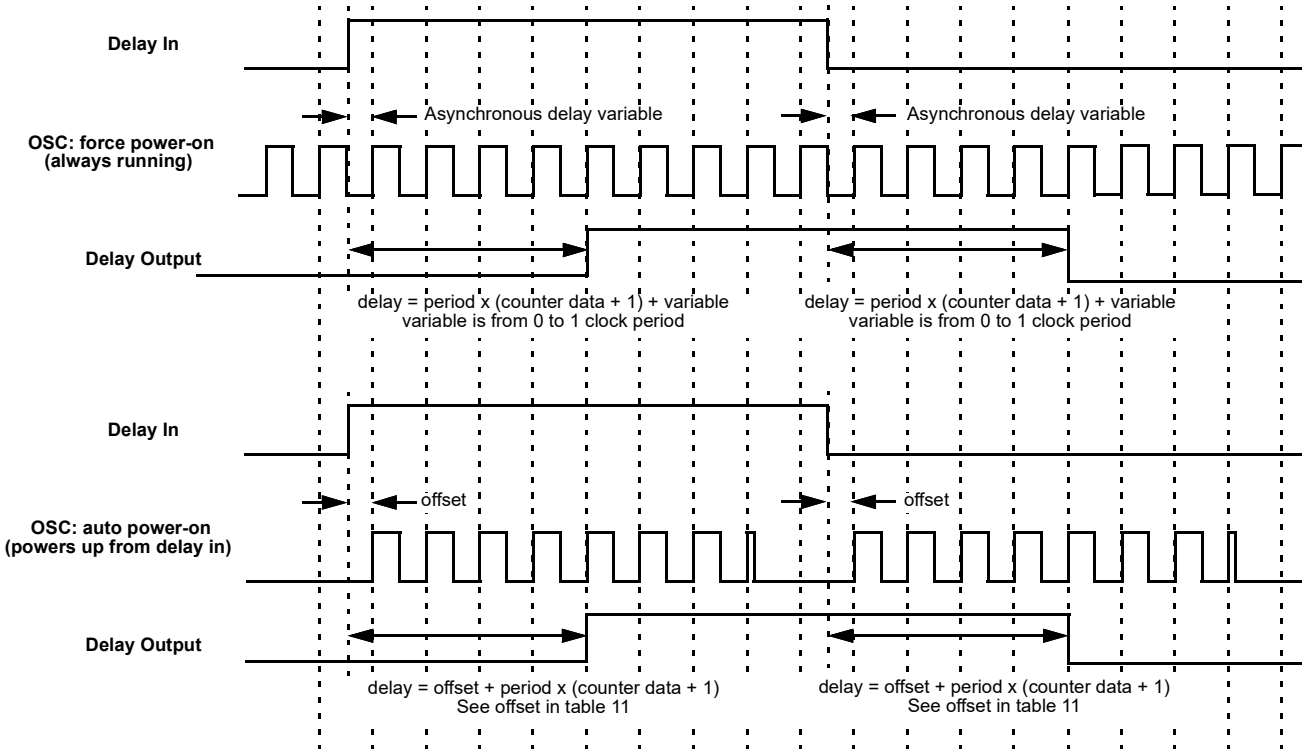


Figure 51: Delay Macrocell Behavior with Different Oscillators Options (Edge Select: Both, Counter Data: 3)

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

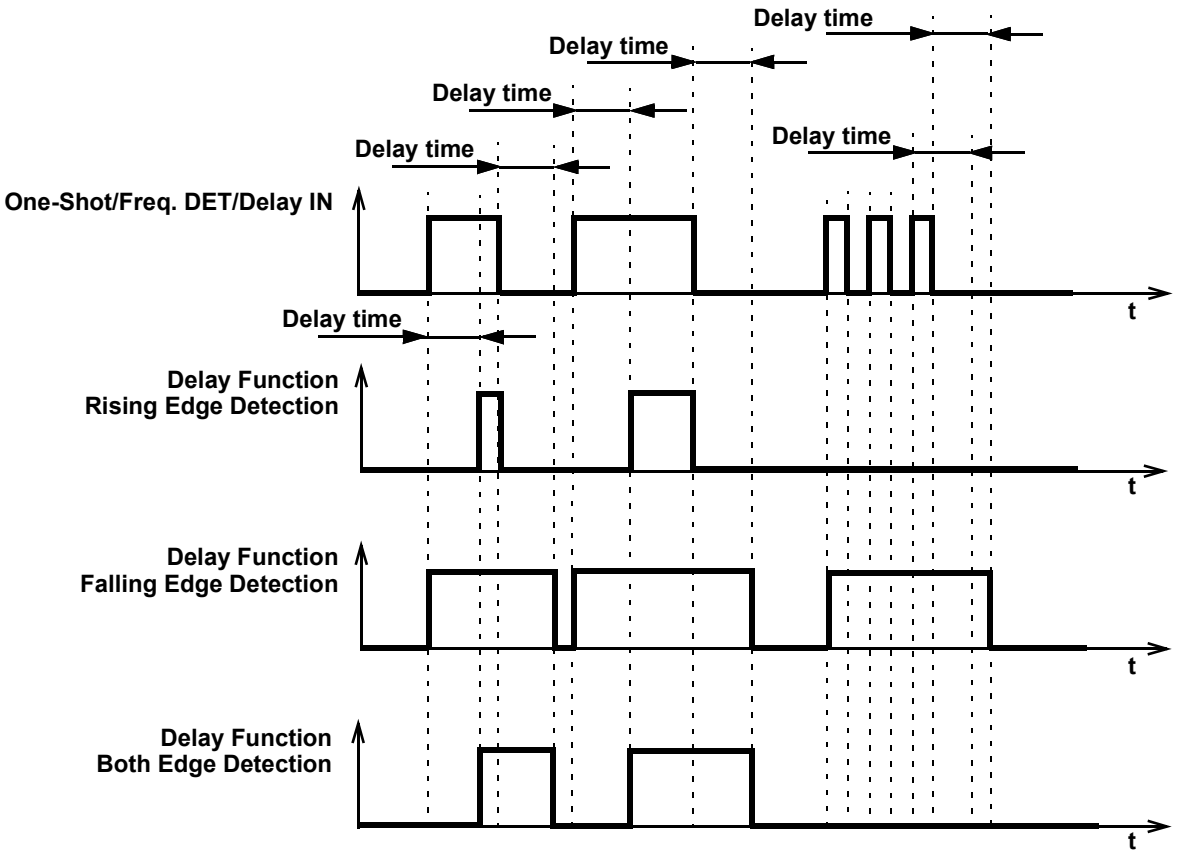


Figure 52: Delay Mode Timing Diagram (Rising, Falling, and Both Edge Detection)

8.3.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY7

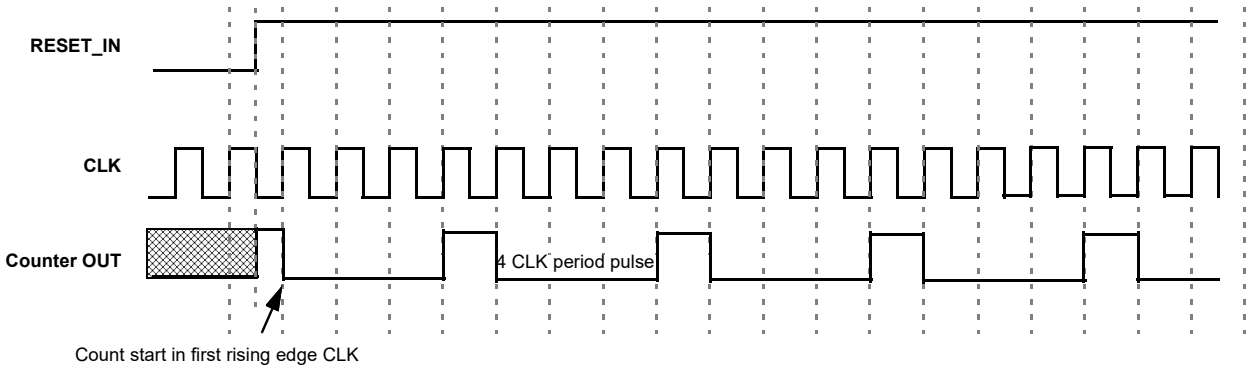


Figure 53: Counter Mode Timing Diagram without Two DFFs Synced Up

.

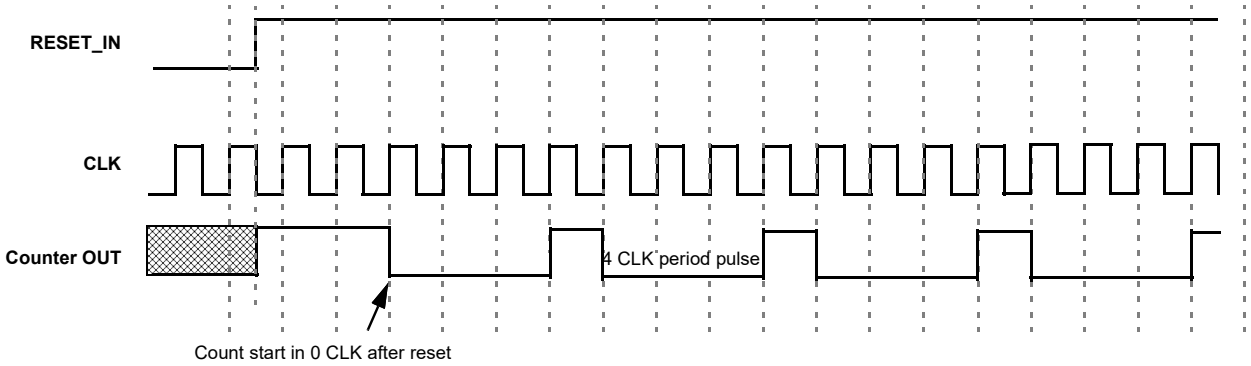


Figure 54: Counter Mode Timing Diagram with Two DFFs Synced Up

8.3.3 One-Shot Mode CNT/DLY0 to CNT/DLY7

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width is determined by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

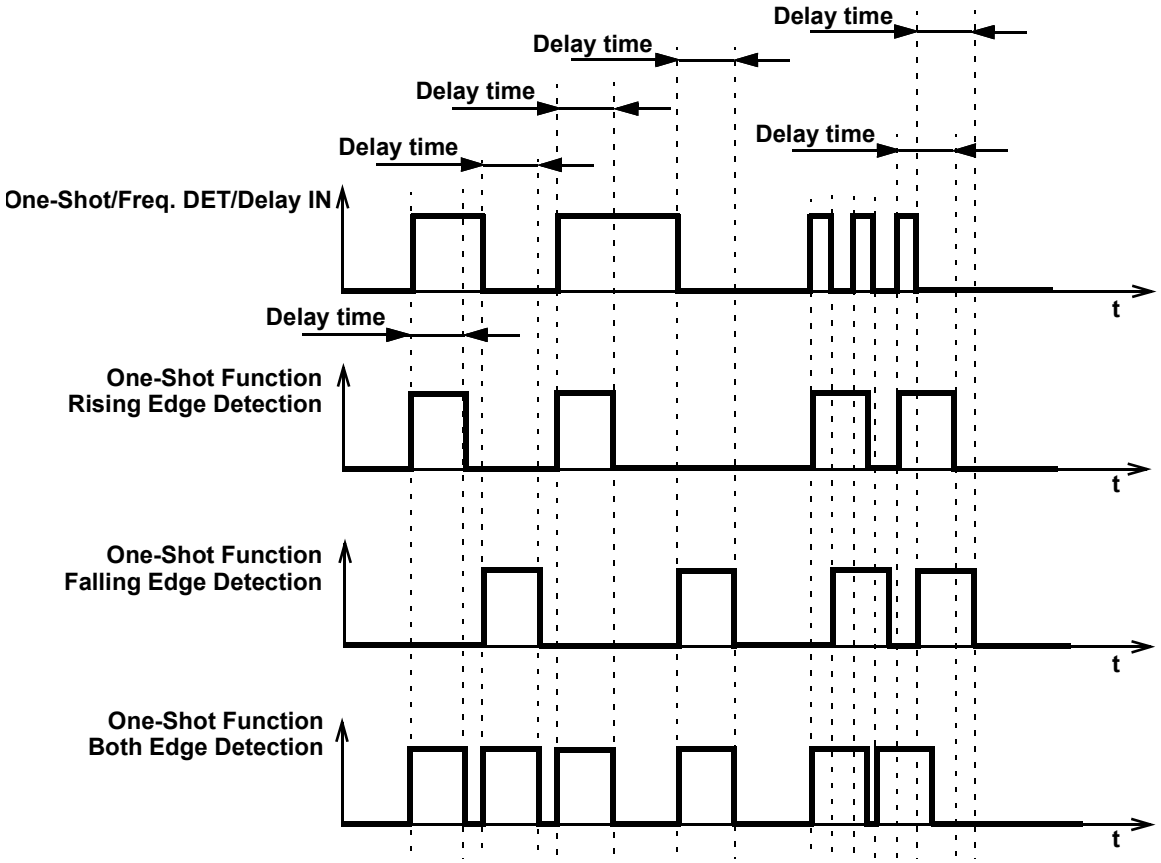


Figure 55: One-Shot Function Timing Diagram

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

8.3.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY7

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

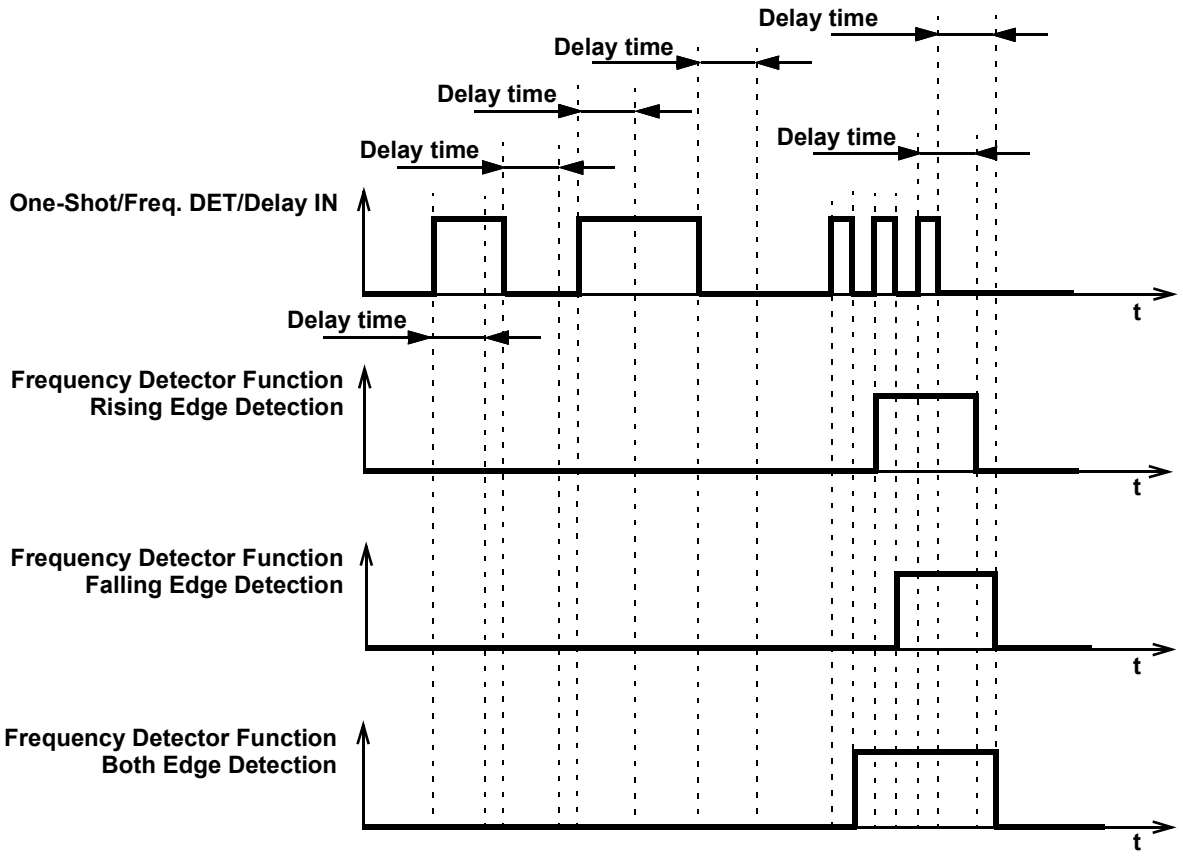


Figure 56: Frequency Detection Mode Timing Diagram

8.3.5 Edge Detection Mode CNT/DLY1 to CNT/DLY7

The macrocell generates high level short pulse when detecting the respective edge. See Table 11.

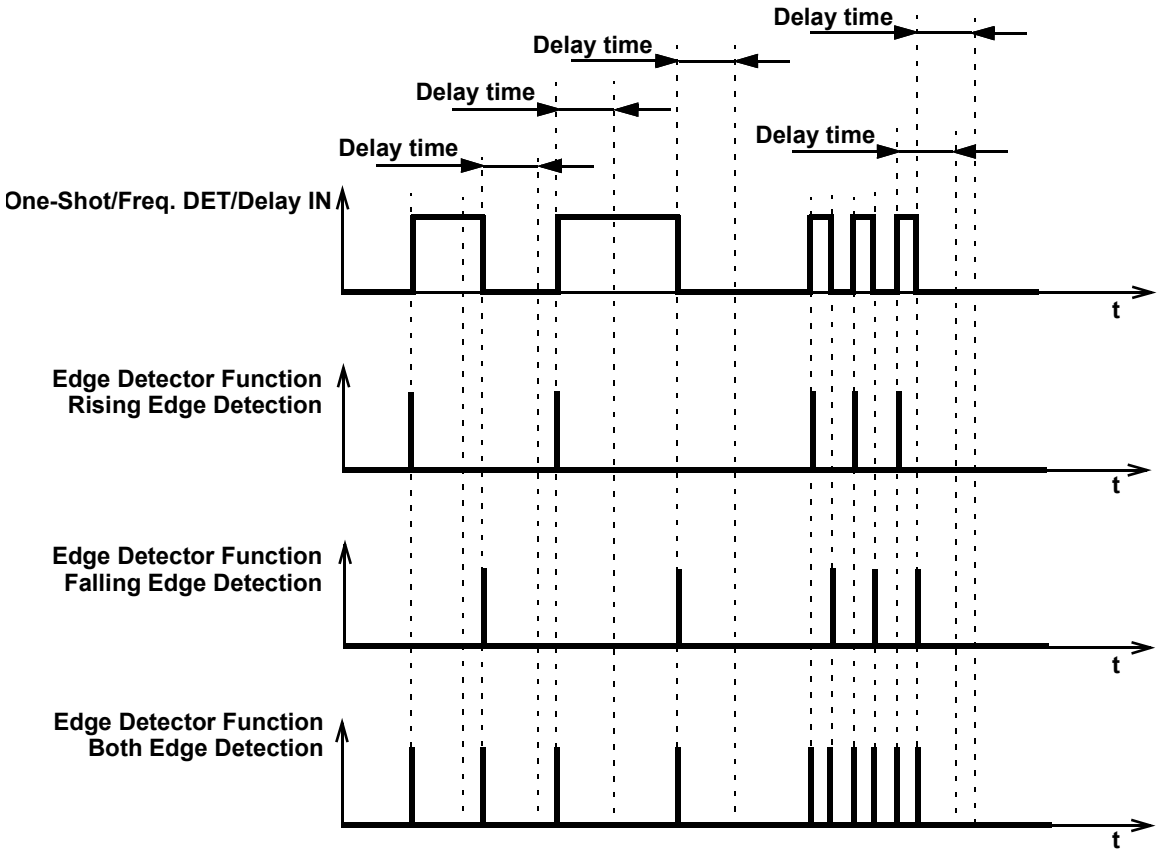


Figure 57: Edge Detection Mode Timing Diagram

8.3.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY7

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 58.

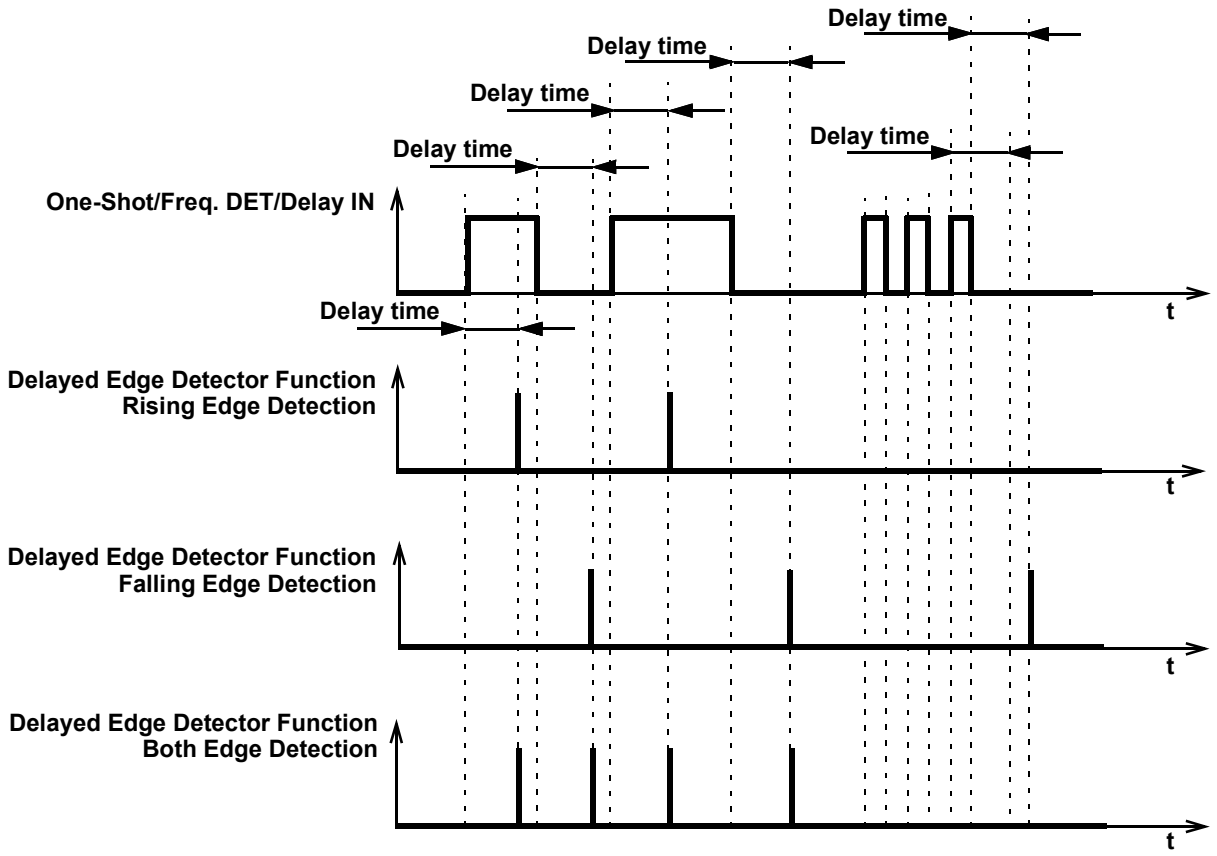


Figure 58: Delayed Edge Detection Mode Timing Diagram

8.3.7 Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. Compared to Counter mode, in Delay/One-Shot/Frequency Detect modes the counter value is shifted for two rising edges of the clock signal. See Figure 59:

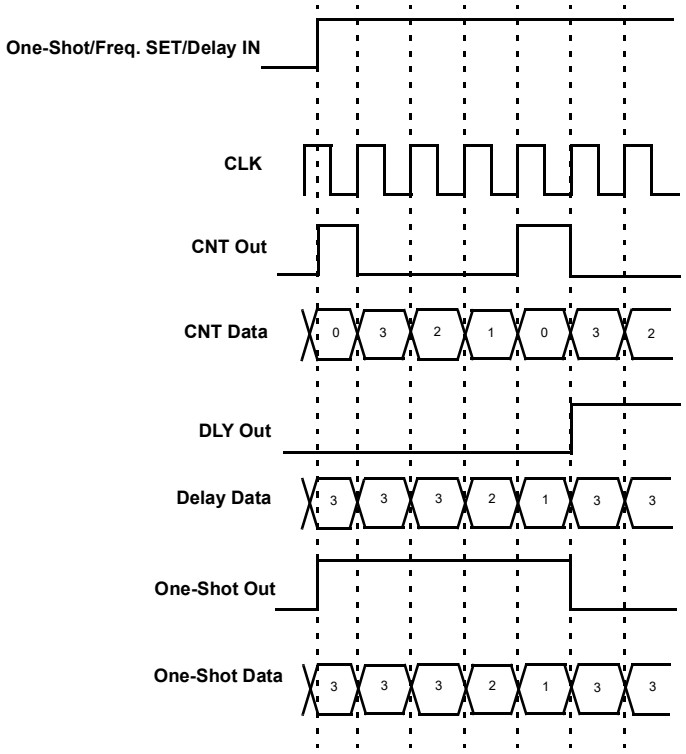


Figure 59: Counter Value, Counter Data = 3

8.4 FSM TIMING DIAGRAMS

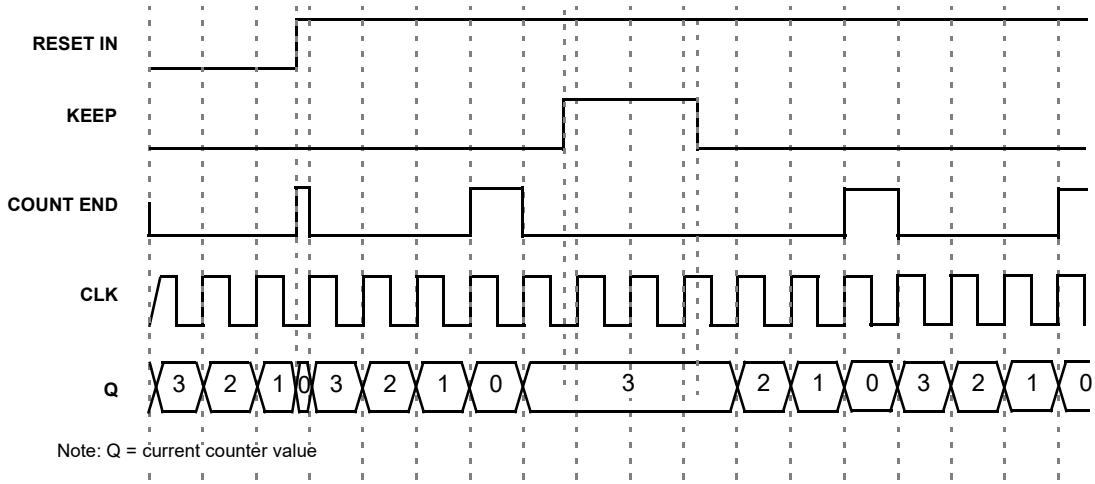


Figure 60: CNT/FSM Mode Timing Diagram (Reset Rising Edge Mode, OSC is Forced On, UP=0) for CNT Data = 3

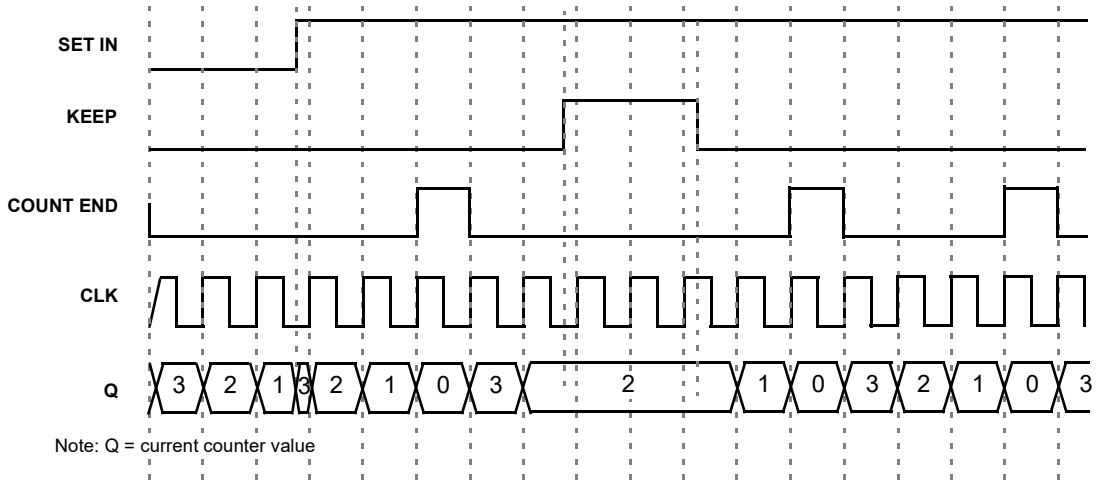


Figure 61: CNT/FSM Mode Timing Diagram (Set Rising Edge Mode, OSC is Forced On, UP = 0) for CNT Data = 3

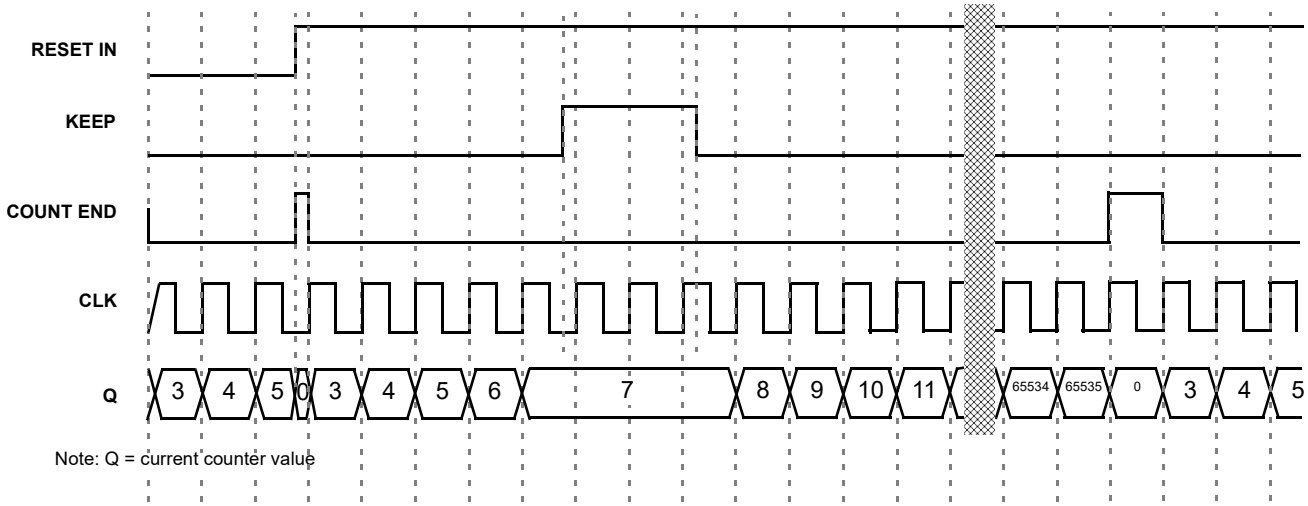


Figure 62: CNT/FSM Mode Timing Diagram (Reset Rising Edge Mode, OSC is Forced On, UP = 1) for CNT Data = 3

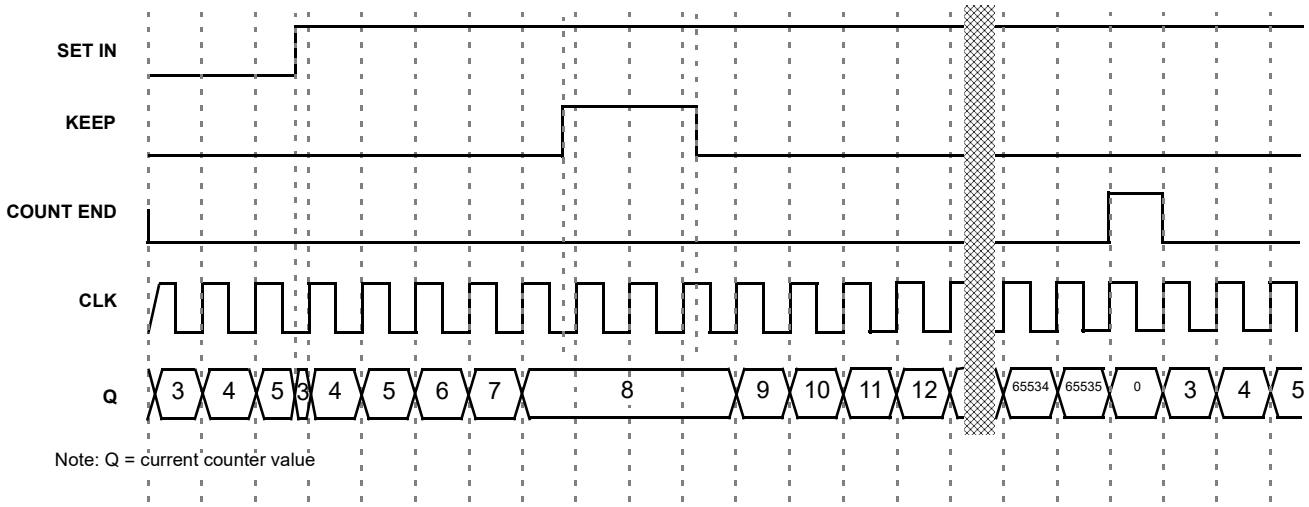


Figure 63: CNT/FSM Mode Timing Diagram (Set Rising Edge Mode, OSC is Forced On, UP = 1) for CNT Data = 3

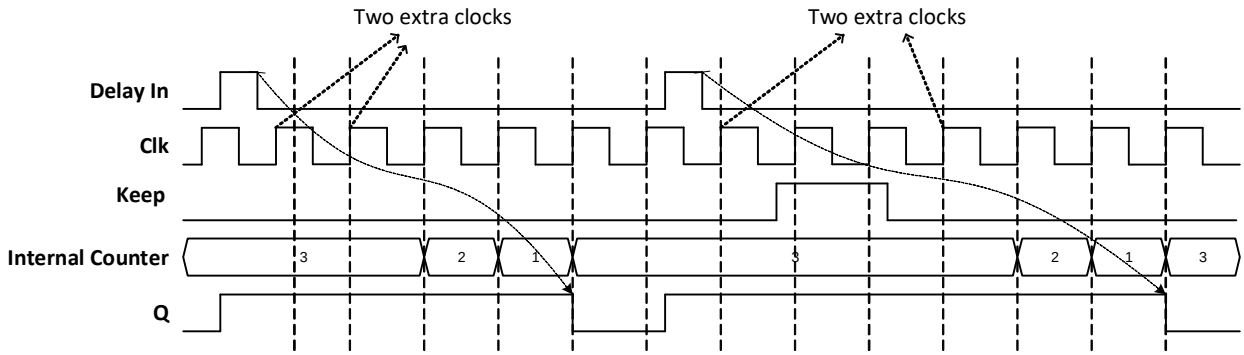


Figure 64: DLY/FSM Mode, Falling Edge Delay, OSC is Forced On, DFFs Synced Up, UP = 0, CNT Data = 3

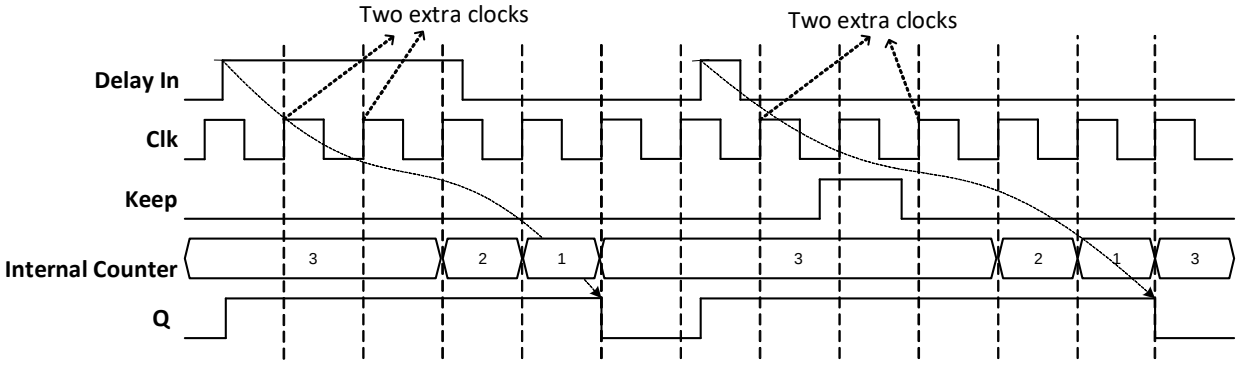


Figure 65: One Shot/FSM Mode, Rising Edge, OSC is Forced On, DFFs Synced Up, UP = 0, CNT Data = 3

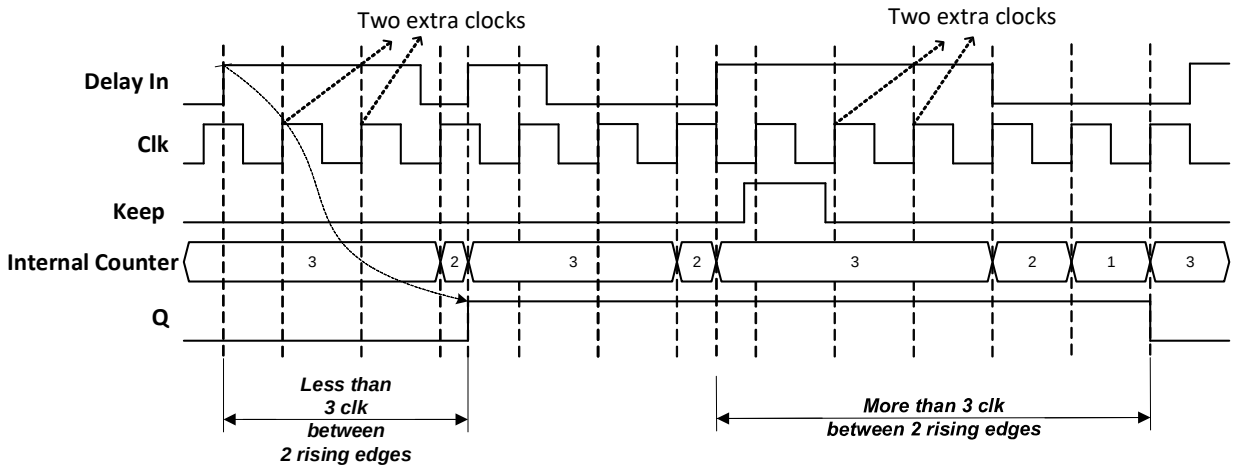


Figure 66: Freq. Detector/FSM Mode, Rising Edge, OSC is Forced On, DFFs Synced Up, UP = 0, CNT Data = 3

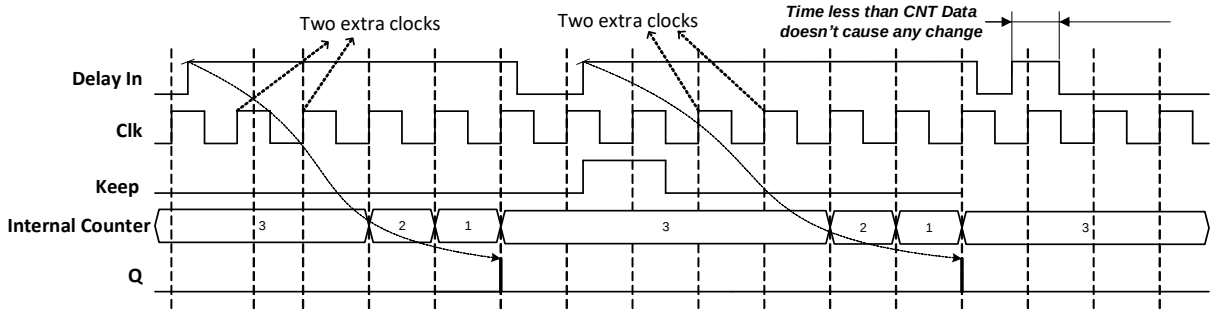


Figure 67: Delayed Edge Detector/FSM Mode, Rising Edge, OSC is Forced On, DFFs Synced Up, UP = 0, CNT Data = 3

8.5 WAKE AND SLEEP CONTROLLER

SLG47512/13 has a Wake and Sleep function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [953:952] = 11 and register [948] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

Note 1: BG/Analog_Good time is long and should be considered in wake and sleep timing in case it dynamically powers on/off.

Note 2: Wake time should be long enough to make sure ACMP and Vref have enough time to get a sample before going to sleep.

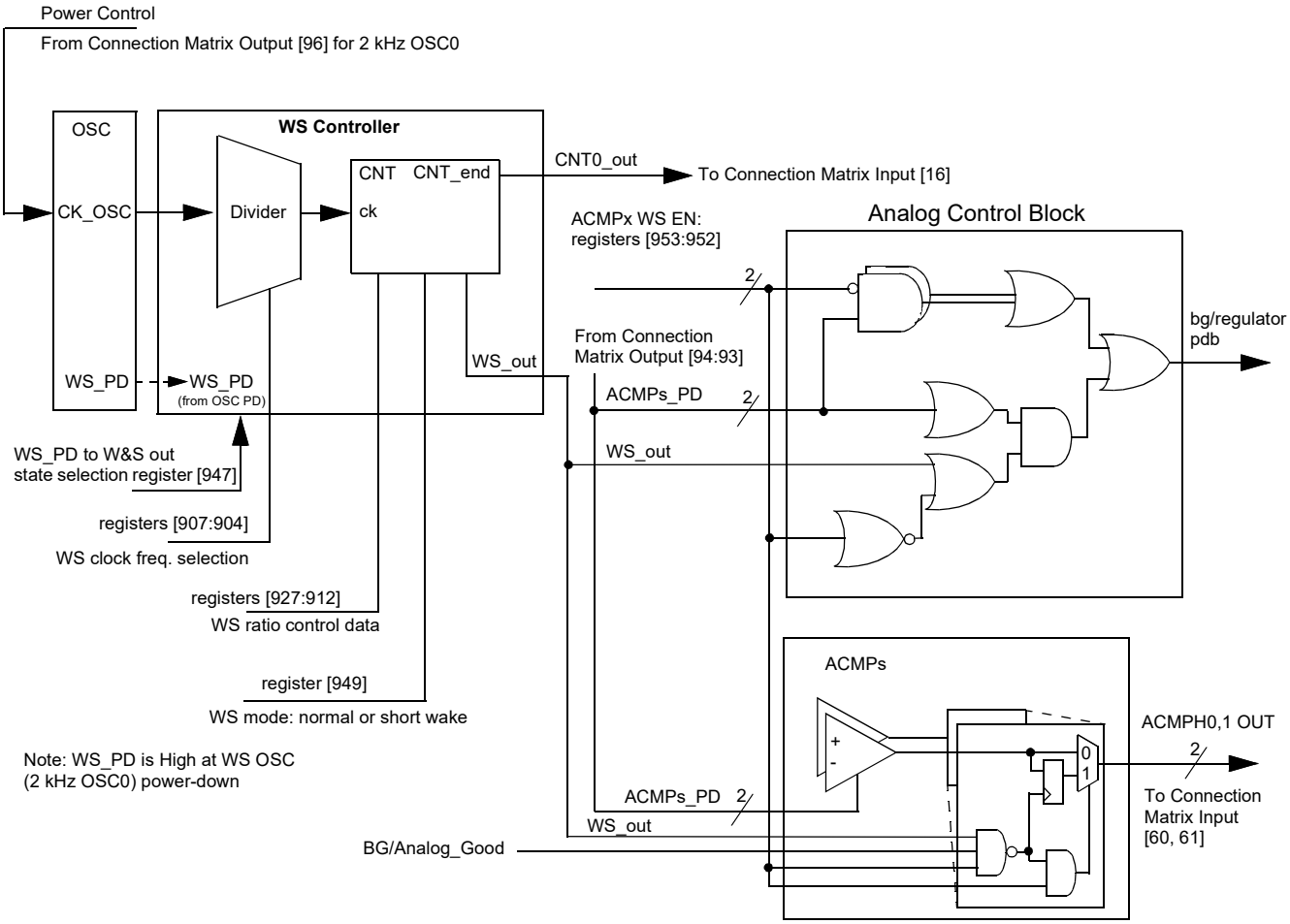
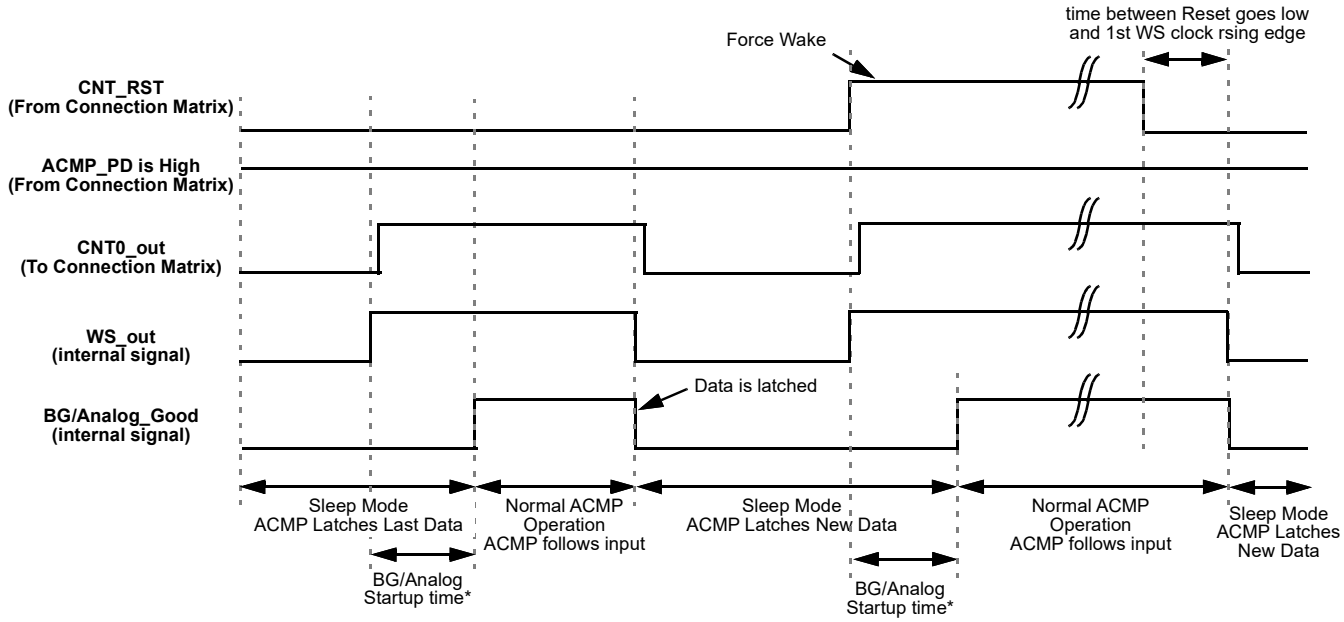
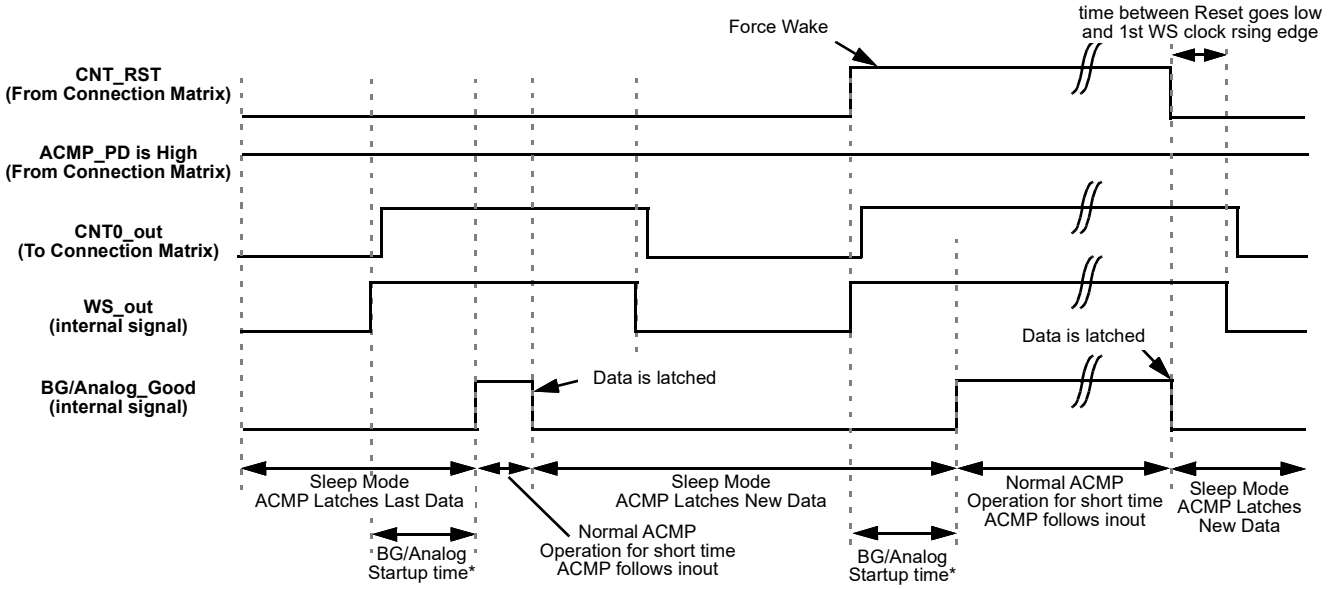


Figure 68: Wake/Sleep Controller



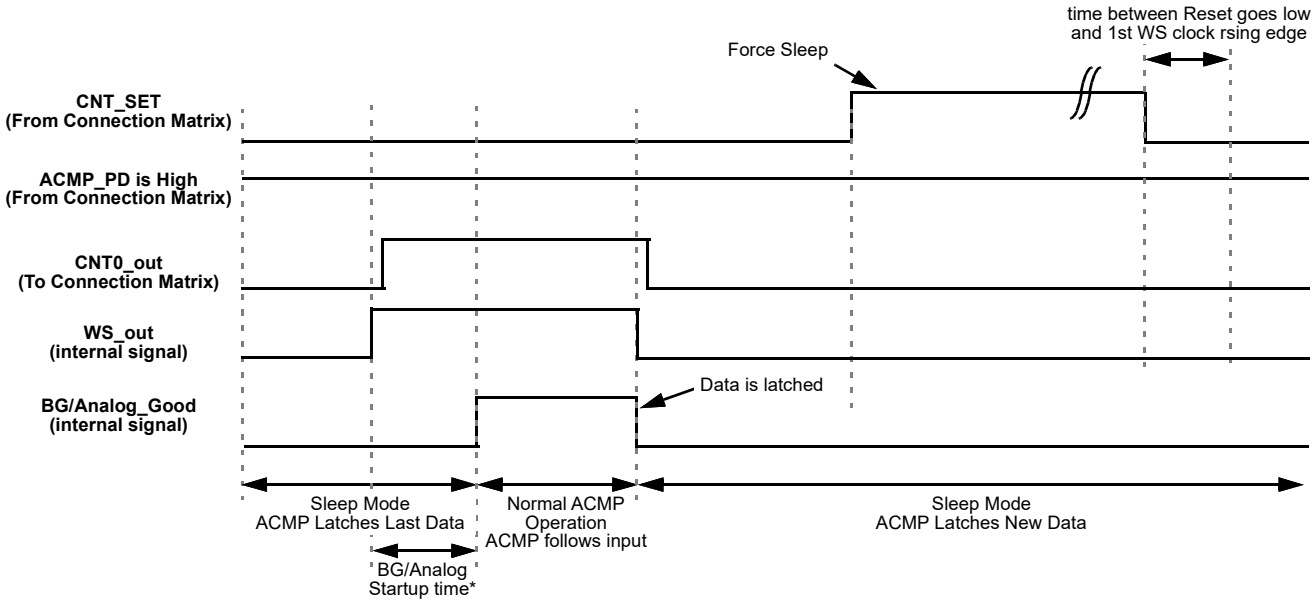
Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 69: Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used



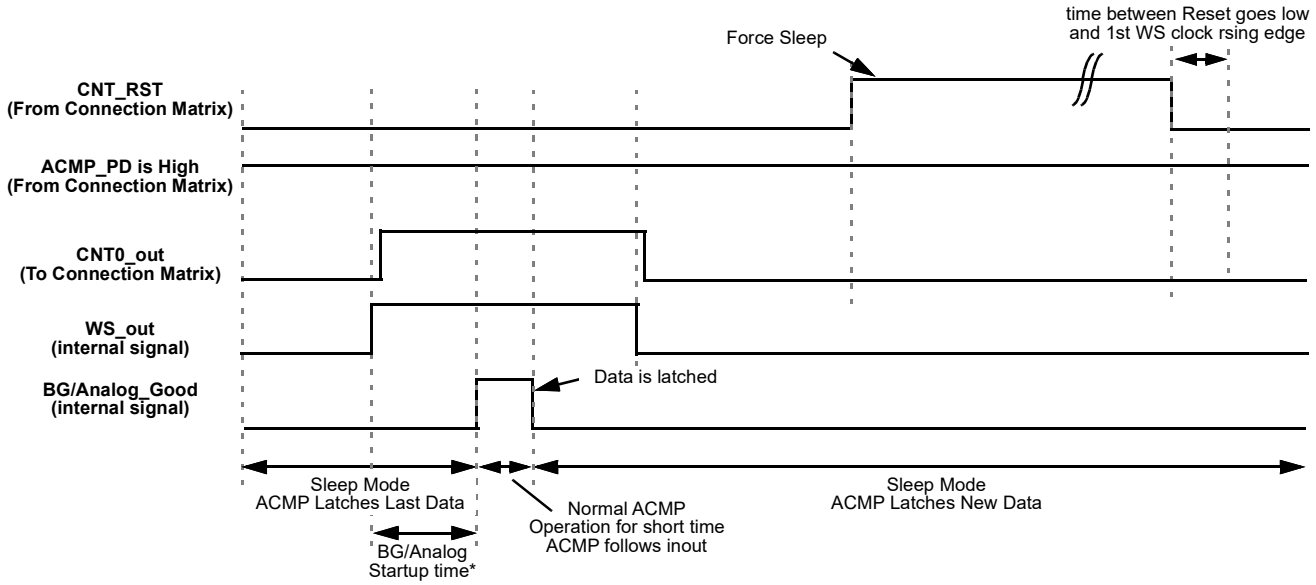
Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 70: Wake/Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used



Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 71: Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used



Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during LATCH.

Figure 72: Wake/Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by WS, the wake time should be longer than 2.1 ms. The BG/analog start up time will take maximal 2 ms. Therefore, 8 periods of the Oscillator0 is recommended for the wake time, when BG is configured to Auto Power mode. If low power BG is always on, Oscillator0 period is longer than required wake time. The BG/analog start up time will take maximal 450 us for ACMP0/1. The short wake mode can be used to reduce the current consumption.

To use any ACMP under WS controller, the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately);
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMP);
- Register WS → enable (for each ACMP separately);
- CNT/DLY0 set/reset input = 0 (for all ACMP).

The user can select a period of time while the ACMP is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.
  Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMPs. When Reset signal goes out, the WS counter will go Low and turn off the ACMP until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMP. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMP while counter is counting up to the end.

Note: The OSC0 matrix power-down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode. High level Set/Reset - switches mode Set/Reset when level is High.

Note: Q mode operates only in case of "High Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPxH on.

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 0.

9 Analog Comparators

There are two High Speed Rail-to-Rail General Purpose Analog Comparators (ACMP) macrocells in the SLG47512/13. For the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0H PWR UP and ACMP1H PWR UP) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be ON continuously, OFF continuously, or switched on periodically, based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low. It is possible to decrease Power-On time of ACMP by forcing internal bias current generator, register [1532] = 1.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1x, 0.5x) before connection to the analog comparator. The gain divider is unbuffered and has input resistance of 1.2 MΩ (typ.) for 0.5x and 100 MΩ for 1x. Each of the ACMP cells has a negative input signal that is either created from an internal Vref or provided by any external source (GPIO 2). Note that the external Vref signal is filtered with a 2nd order low pass filter with 300 kHz typical bandwidth, see Figure 73 to Figure 74.

Input bias current < 1 nA (typ).

PWR UP = 1 => ACMP is powered up.

PWR UP = 0 => ACMP is powered down.

During power-up, the ACMP output will remain LOW, and then becomes valid after power up signal goes high for ACMP0H and ACMP1H (see parameter t_{start} in Table 18).

It is possible to enable Low Pass Filter (LPF) either on ACMP IN+ or on ACMP out, registers [1497:1496] and register [1513:1512].

Each cell also has a hysteresis selection, to offer hysteresis of (0, 25, 50, 150) mV. The hysteresis option is available when using an internal Vref only.

ACMP0H IN+ options are GPIO and V_{DD}.

ACMP1H IN+ options are GPIO, ACMP0H IN+ MUX output, Temperature Sensor.
See Table 34 for ACMP Inputs selection.

Table 34: ACMP Input Selection

Register [1530]	Register [1500]	Register [1516]	ACMP0H Positive Input	ACMP1H Positive Input
0	0	0	ACMP0H+ PIN	ACMP1H+ PIN
0	0	1	ACMP0H+ PIN	ACMP0H+ PIN
0	1	0	V_{DD}	ACMP1H+ PIN
0	1	1	V_{DD}	V_{DD}
1	0	0	ACMP0H+ PIN	Temp Sensor
1	0	1	ACMP0H+ PIN	Temp Sensor
1	1	0	V_{DD}	Temp Sensor
1	1	1	V_{DD}	Temp Sensor

9.1 ACMP0H BLOCK DIAGRAM

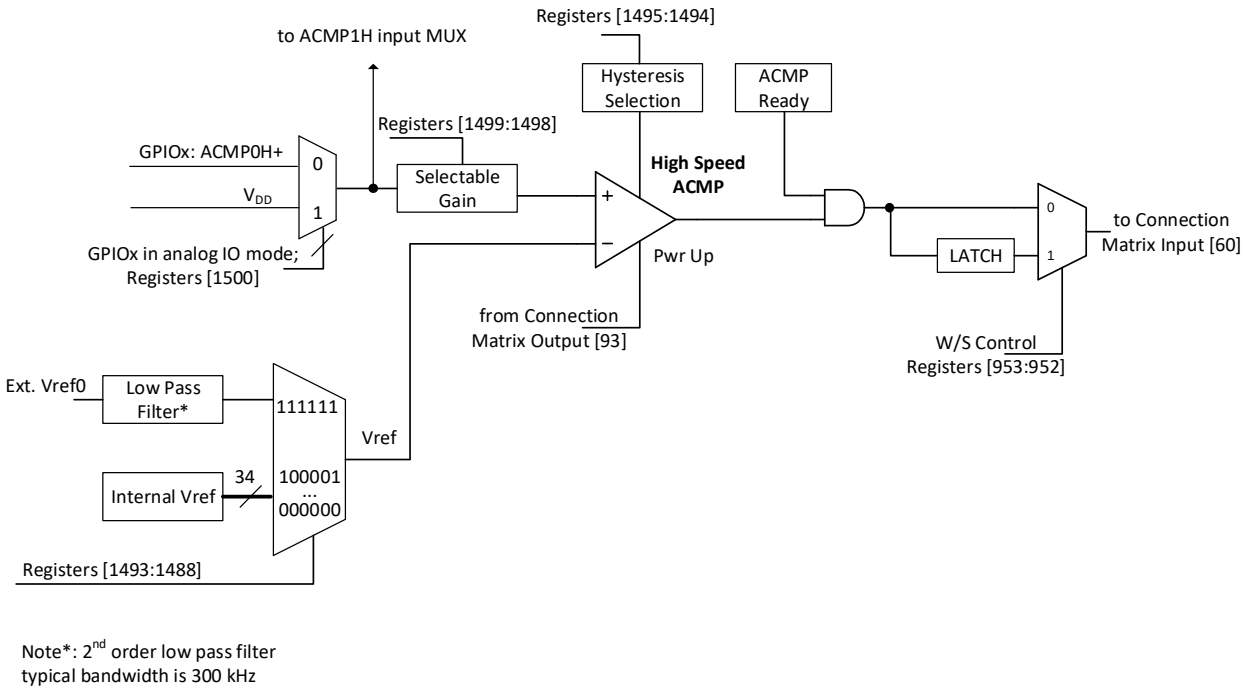
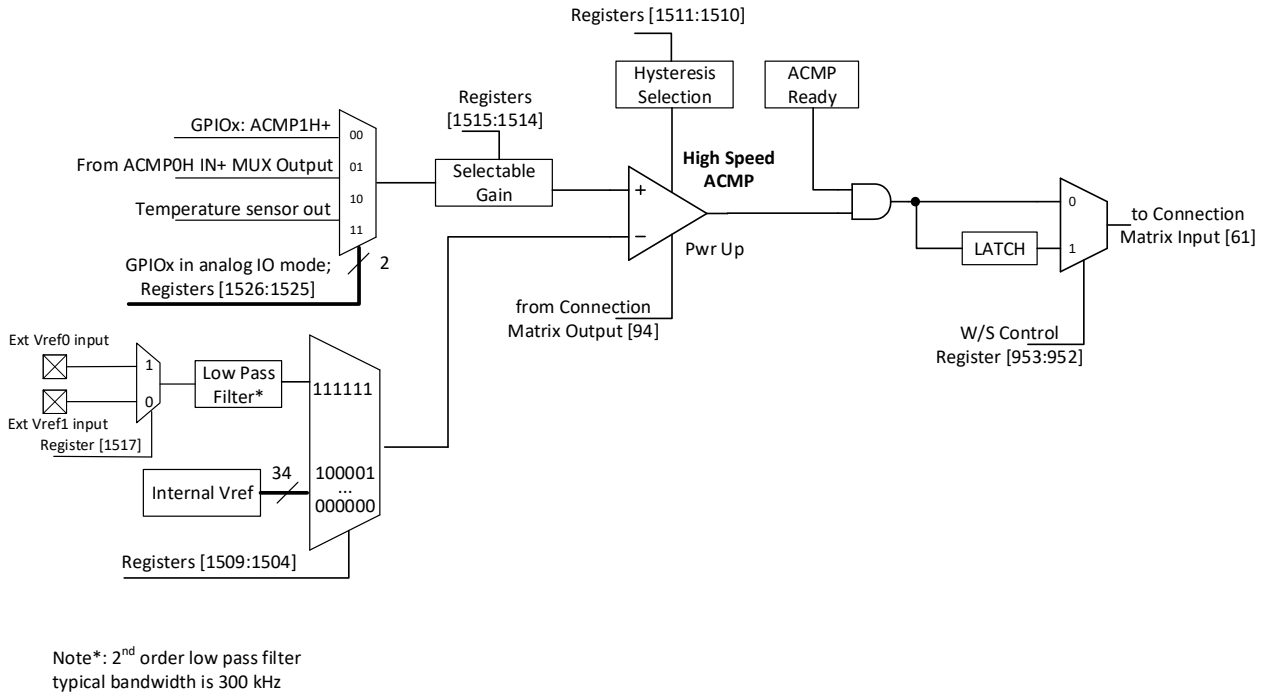


Figure 73: ACMP0H Block Diagram

9.2 ACMP1H BLOCK DIAGRAM



Note*: 2nd order low pass filter typical bandwidth is 300 kHz

Figure 74: ACMP1H Block Diagram

9.3 ACMP TYPICAL PERFORMANCE

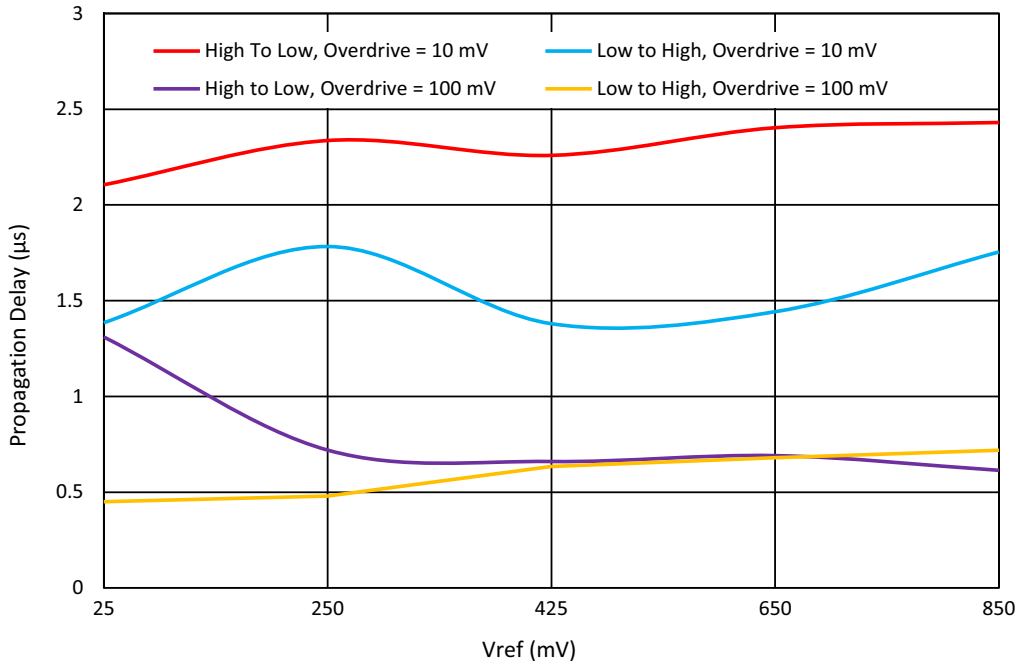


Figure 75: Typical Propagation Delay vs. Vref for ACMPxH at T = 25 °C, Gain = 1, Hysteresis = 0, V_{DD} = 1.0 V to 1.65 V

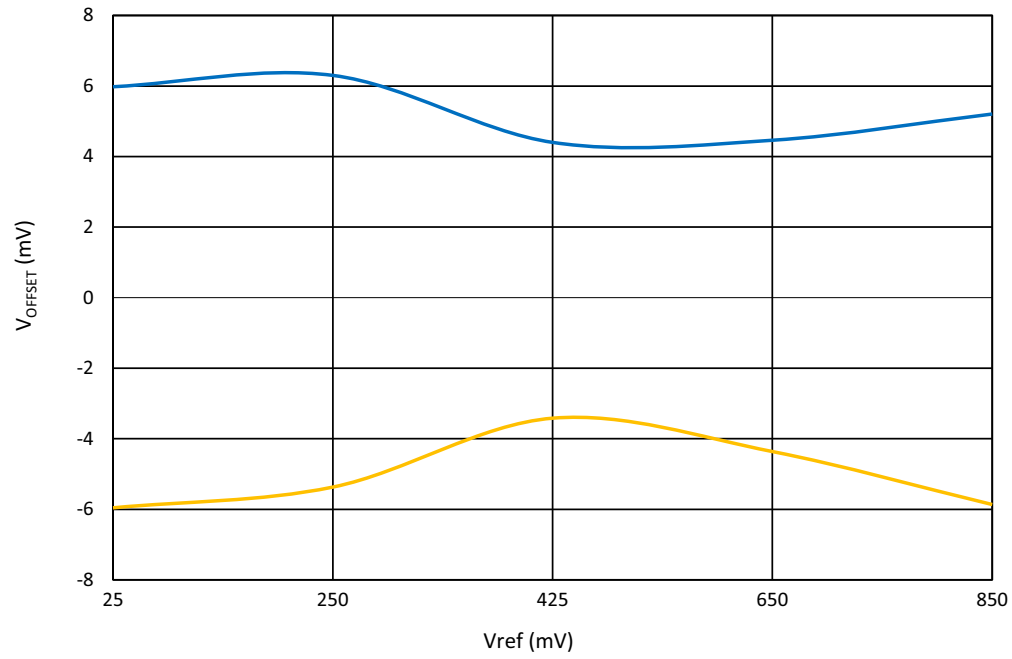


Figure 76: ACMPxH Input Offset Voltage vs. Vref at T = -40 °C to 85 °C, V_{DD} = 1.0 V to 1.65 V

10 Programmable Delay/Edge Detector

The SLG47512/13 has a programmable time delay logic cell that can generate a delay that is selectable from one of four timings configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 77 and Figure 78 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

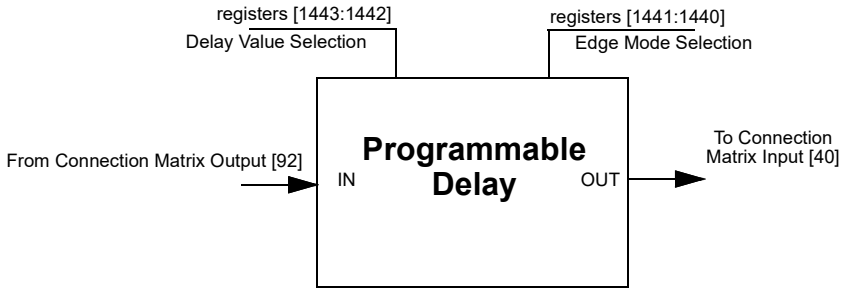


Figure 77: Programmable Delay

10.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

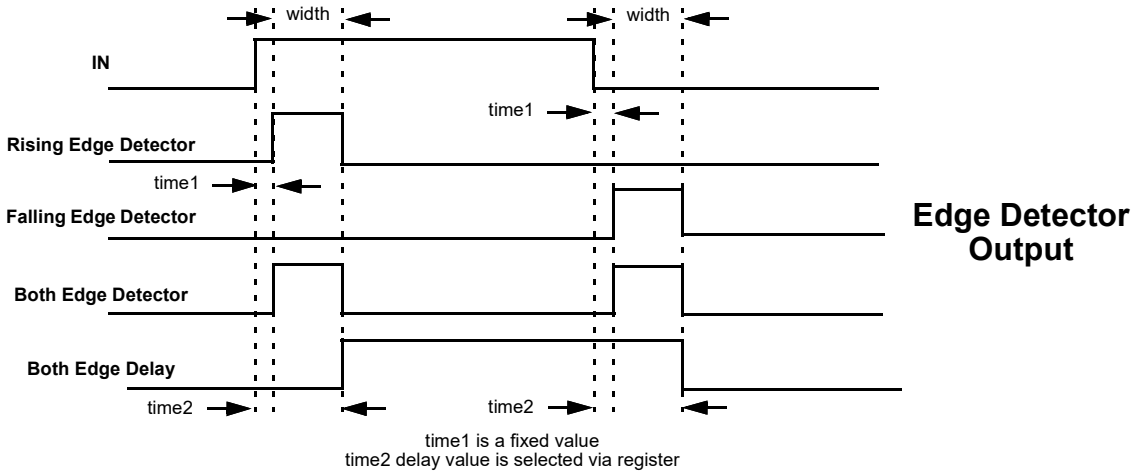


Figure 78: Edge Detector Output

Please refer to Table 11.

11 Additional Logic Function. Deglitch Filter

The SLG47512/13 has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection Matrix inputs and outputs. The filter blocks the input signal for pulse width < t_{block} (at typical temperature 25 °C. See Table 14) and pass the input signal for pulse width > t_{pass} (at typical temperature 25 °C). For width in between, the output pulse width will be reduced.

In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay

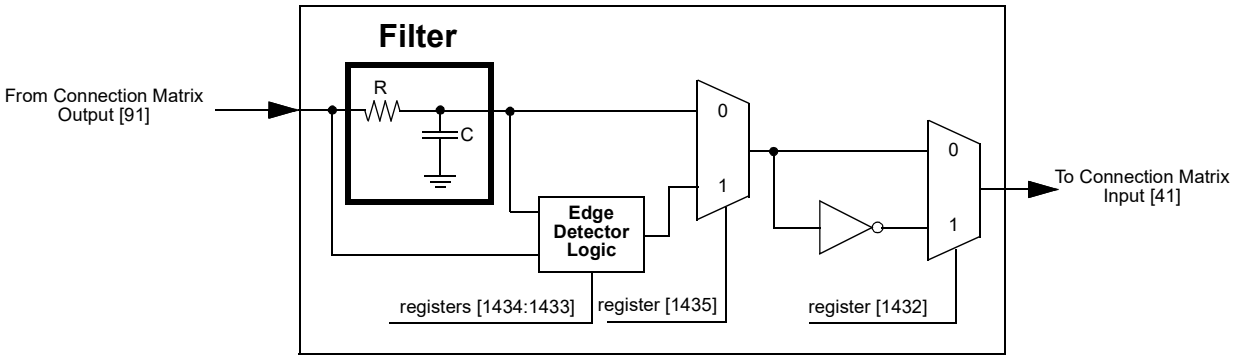


Figure 79: Deglitch Filter/Edge Detector Simplified Structure

12 Voltage Reference

12.1 VOLTAGE REFERENCE OVERVIEW

The SLG47512/13 has a Voltage Reference (Vref) macrocell to provide references to the two analog comparators. This macrocell can supply a user selection of fixed voltage references, or temperature sensor output. The macrocell also has the option to output reference voltages on GPIO. See Table 35 for the available selections for each analog comparator.

When changing power-down source settings or power-down register settings in a Voltage Reference block, similar changes of these settings automatically occur in an Analog Temperature Sensor block.

Also see Figure 80, which shows the reference output structure.

12.2 VREF SELECTION TABLE

Table 35: Vref Selection Table

SEL[5:0]	Vref	SEL[5:0]	Vref
0	0.025	18	0.475
1	0.05	19	0.5
2	0.075	20	0.525
3	0.1	21	0.55
4	0.125	22	0.575
5	0.15	23	0.6
6	0.175	24	0.625
7	0.2	25	0.65
8	0.225	26	0.675
9	0.25	27	0.7
10	0.275	28	0.725
11	0.3	29	0.75
12	0.325	30	0.775
13	0.35	31	0.8
14	0.375	32	0.825
15	0.4	33	0.850
16	0.425	34 to 62	0.850
17	0.45	63	Ext. Vref

12.3 VREF BLOCK DIAGRAM

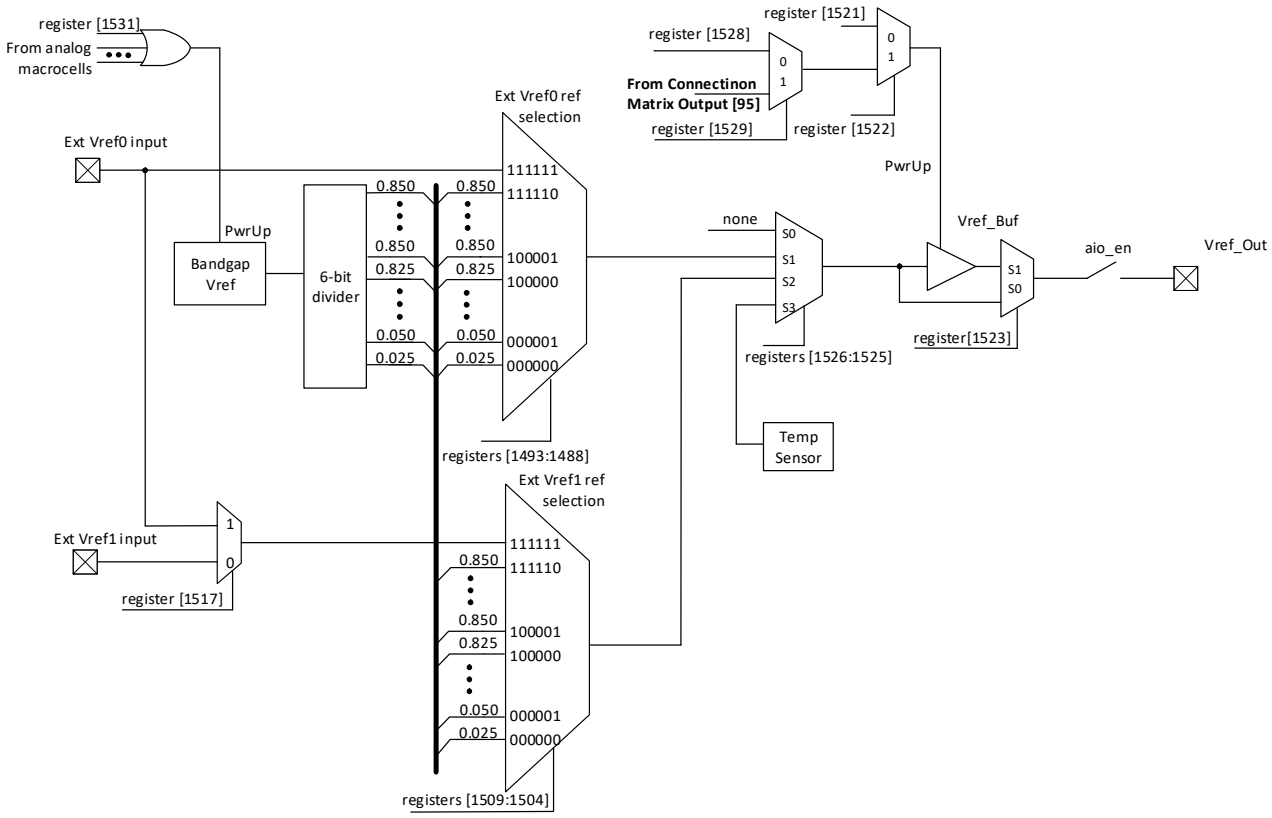


Figure 80: Voltage Reference Block Diagram

12.4 VREF TYPICAL PERFORMANCE

Note 1 It is not recommended to use Vref connected to external pin without buffer.

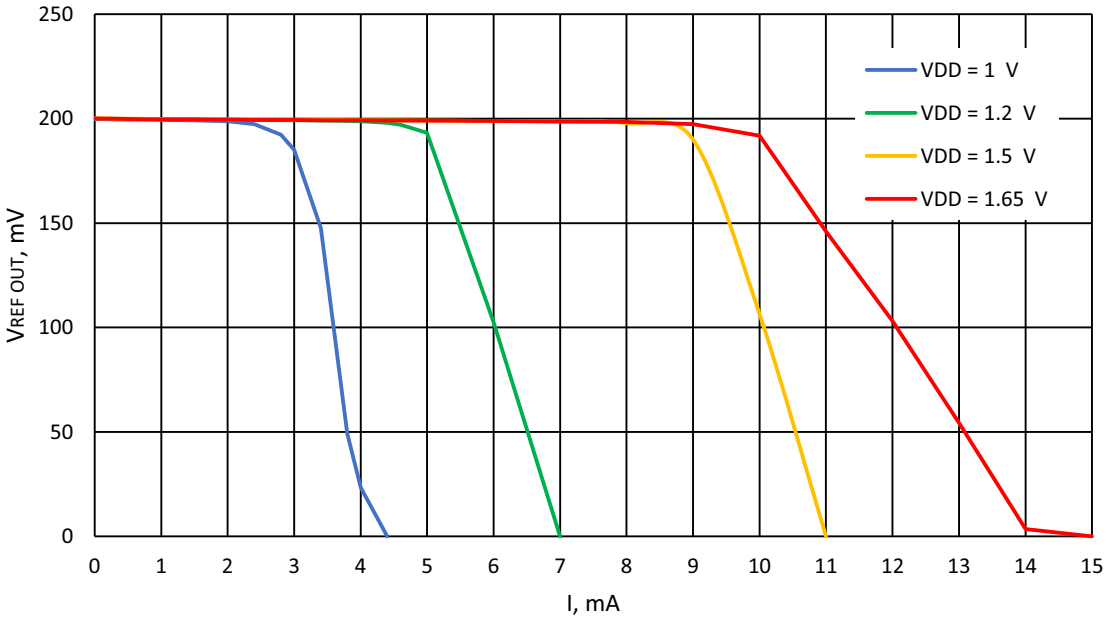


Figure 81: Typical Load Regulation, Vref = 200 mV, T = -40 °C to +85 °C, Buffer - Enable

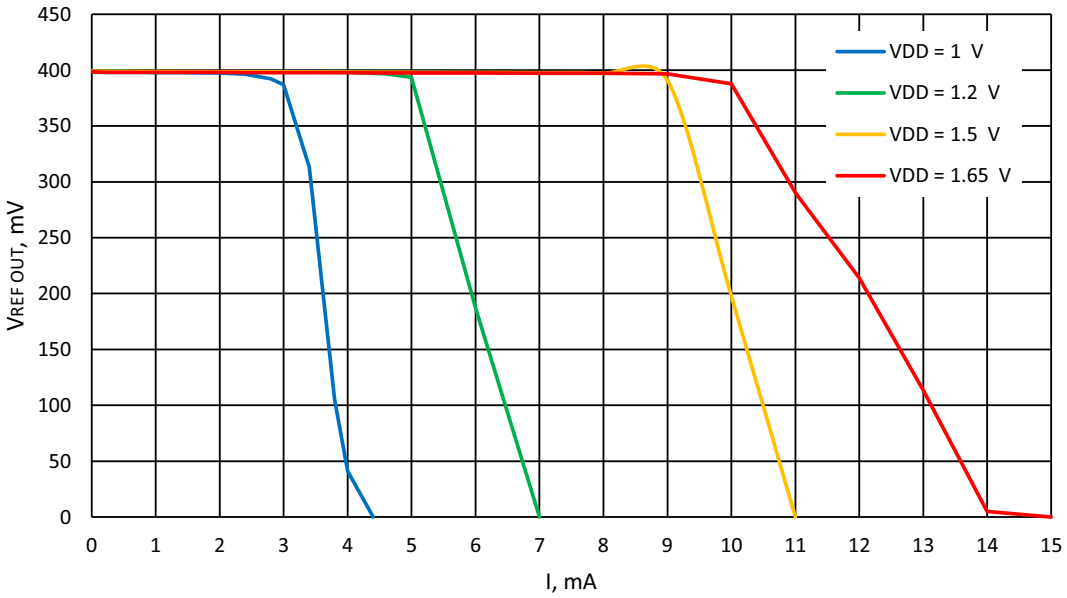


Figure 82: Typical Load Regulation, Vref = 400 mV, T = -40 °C to +85 °C, Buffer - Enable

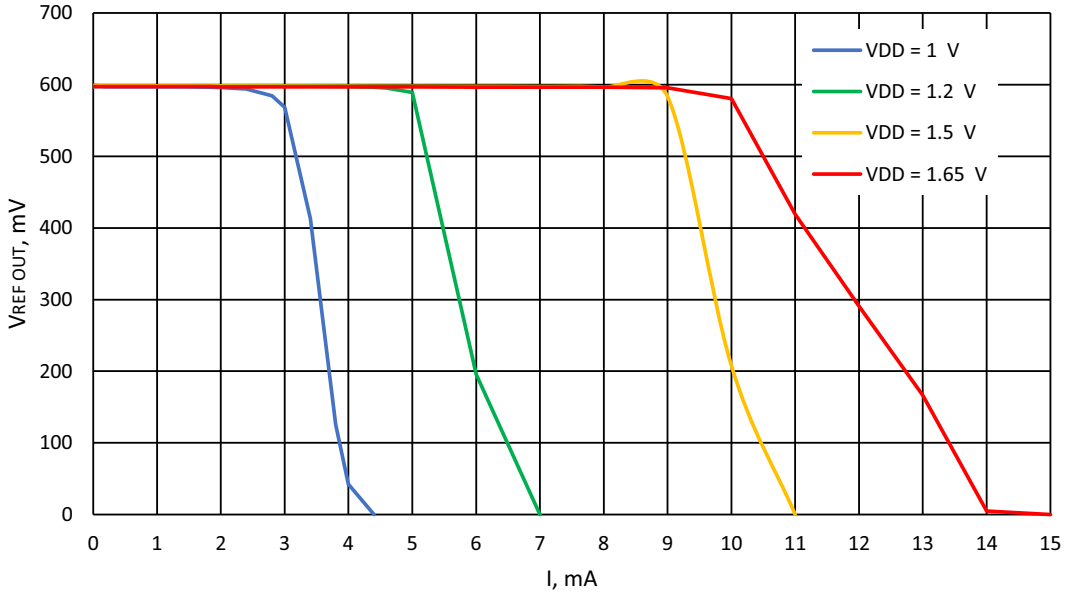


Figure 83: Typical Load Regulation, Vref = 600 mV, T = -40 °C to +85 °C, Buffer - Enable

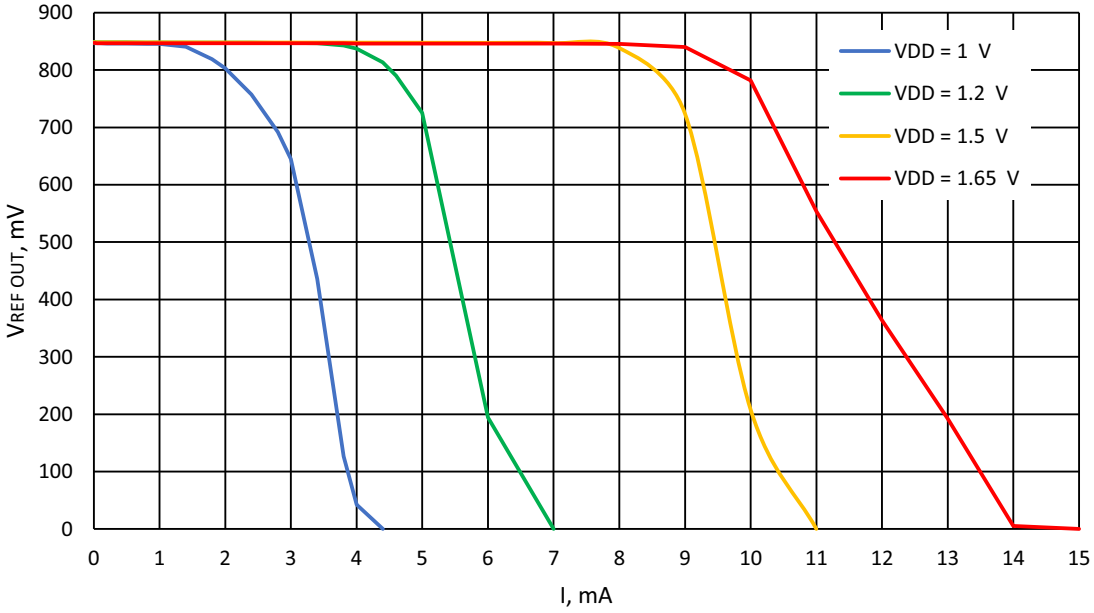


Figure 84: Typical Load Regulation, Vref = 850 mV, T = -40 °C to +85 °C, Buffer - Enable

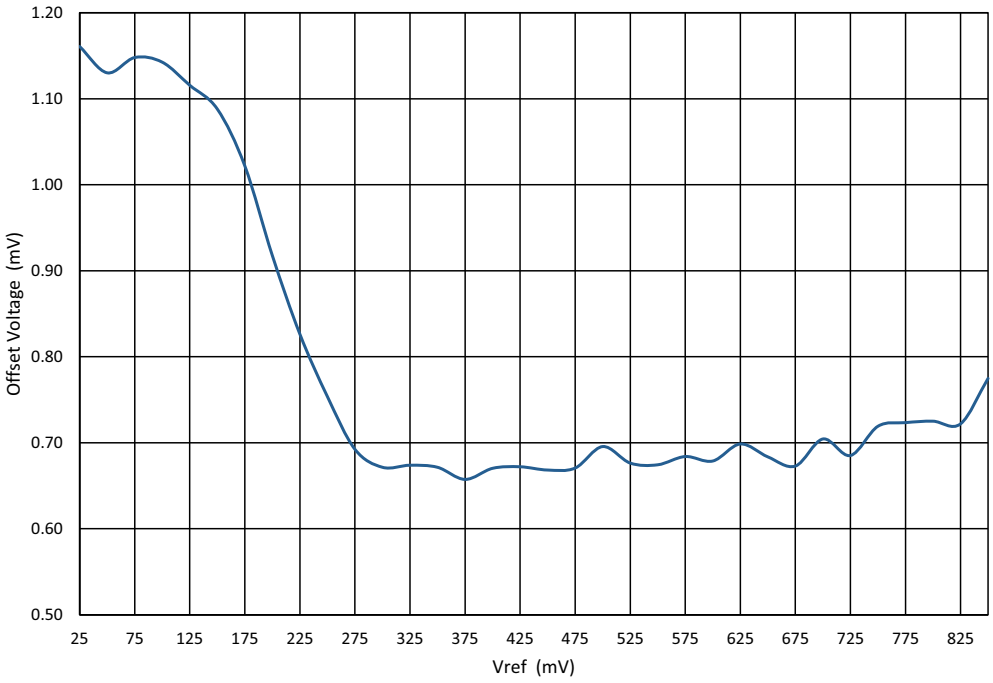


Figure 85: Typical Input Offset Voltage vs. Vref at V_{DD} = 1.2 V, T = 25 °C

13 Clocking

13.1 OSC GENERAL DESCRIPTION

The SLG47512/13 has two internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (25 MHz).

There are two divider stages for each oscillator that give the user flexibility for introducing clock signals to connection matrix, as well as various other macrocells. The pre-divider (first stage) for Oscillator0 allows the selection of /1, /2, /4, or /8 to divide down frequency from the fundamental. The pre-divider (first stage) for Oscillator1 allows the selection of /1, /2, /4, /8, /12, /24, /48, /96 to divide down frequency from the fundamental. The second stage divider of oscillators has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24, or /64 on Connection Matrix Input lines [57], [58] and [59]. Please see Figure 86, Figure 87, and Figure 88 for more details on the SLG47512/13 clock scheme.

Oscillator1 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [1480]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power-down/Force On (Connection Matrix Output [96], [97]) signal has the highest priority. The OSC operates according to the following table:

Table 36: Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal From Connection Matrix	Register: Power-Down or Force On by Matrix Input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF

Note 1 The OSC will run only when any macrocell that uses OSC is powered on.

To avoid metastability issue user can select synchronization type for Power-down signal:

- registers [1483:1482], [1487:1486] = 00 – two-DFF synchronization. Oscillator will have from 1 to 2 output pulses after Power-

down.

- registers [1483:1482], [1487:1486] = 01 – one-DFF synchronization by clock falling edge. When Oscillator Power-down signal comes, Oscillator generates full output pulse and then stops.
- registers [1483:1482], [1487:1486] = 10 or 11 – without synchronization (asynchronous reset). When Oscillator Power-down signal comes, Oscillator output goes low immediately.

If I^2C is used to change the synchronization mode there will be a pulse at the Oscillator output when the synchronization mode is changed from 10 or 11 (asynchronous reset).

13.2 OSCILLATOR0 (2.048 KHZ)

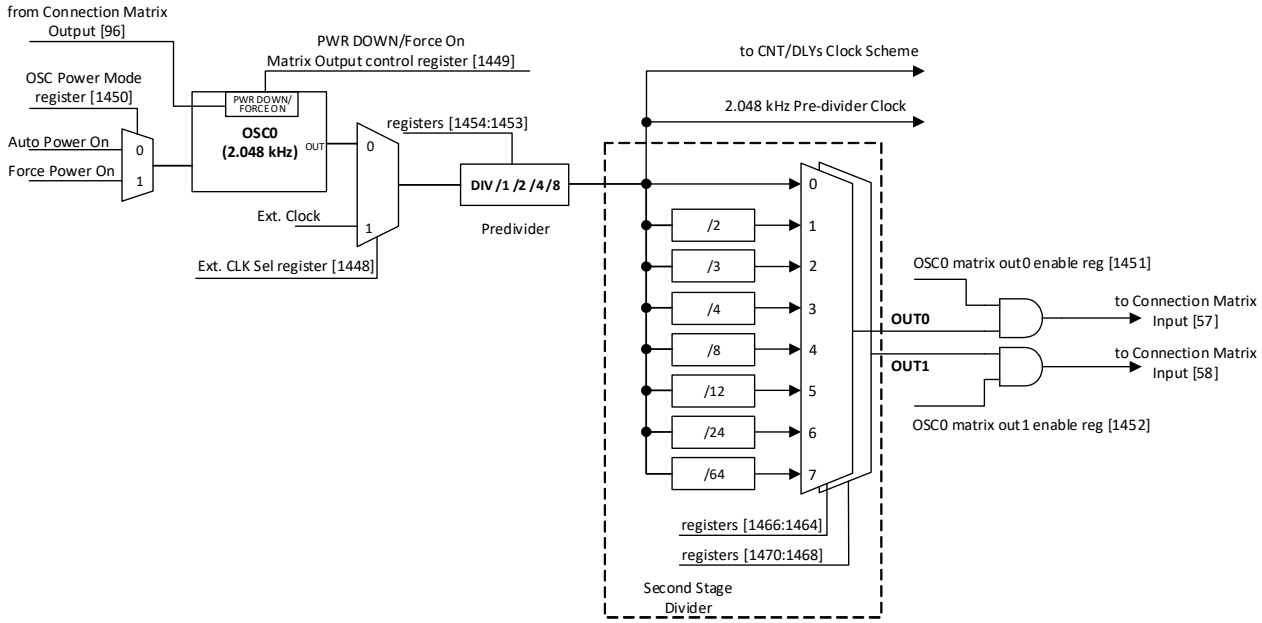


Figure 86: Oscillator0 Block Diagram

Note: It's highly recommended to use OSC0 without the startup delay (register[1484] = 1).

13.3 OSCILLATOR1 (25 MHZ)

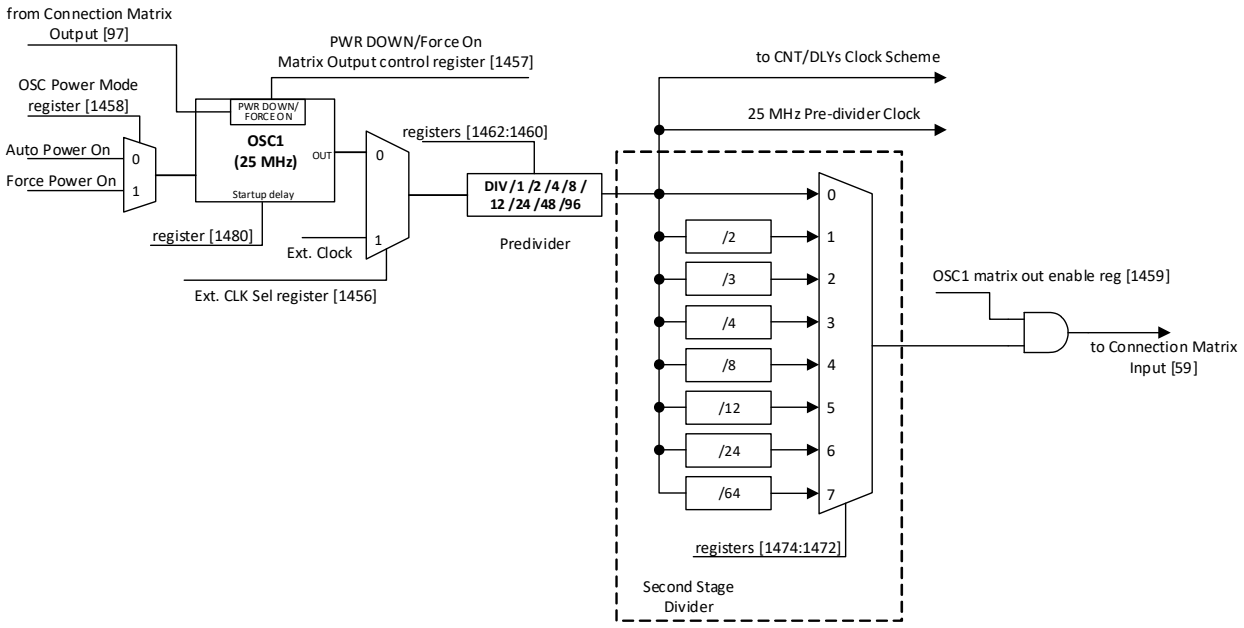


Figure 87: Oscillator1 Block Diagram

13.4 CNT/DLY CLOCK SCHEME

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/4, OSC1/8, OSC1/64, OSC1/512

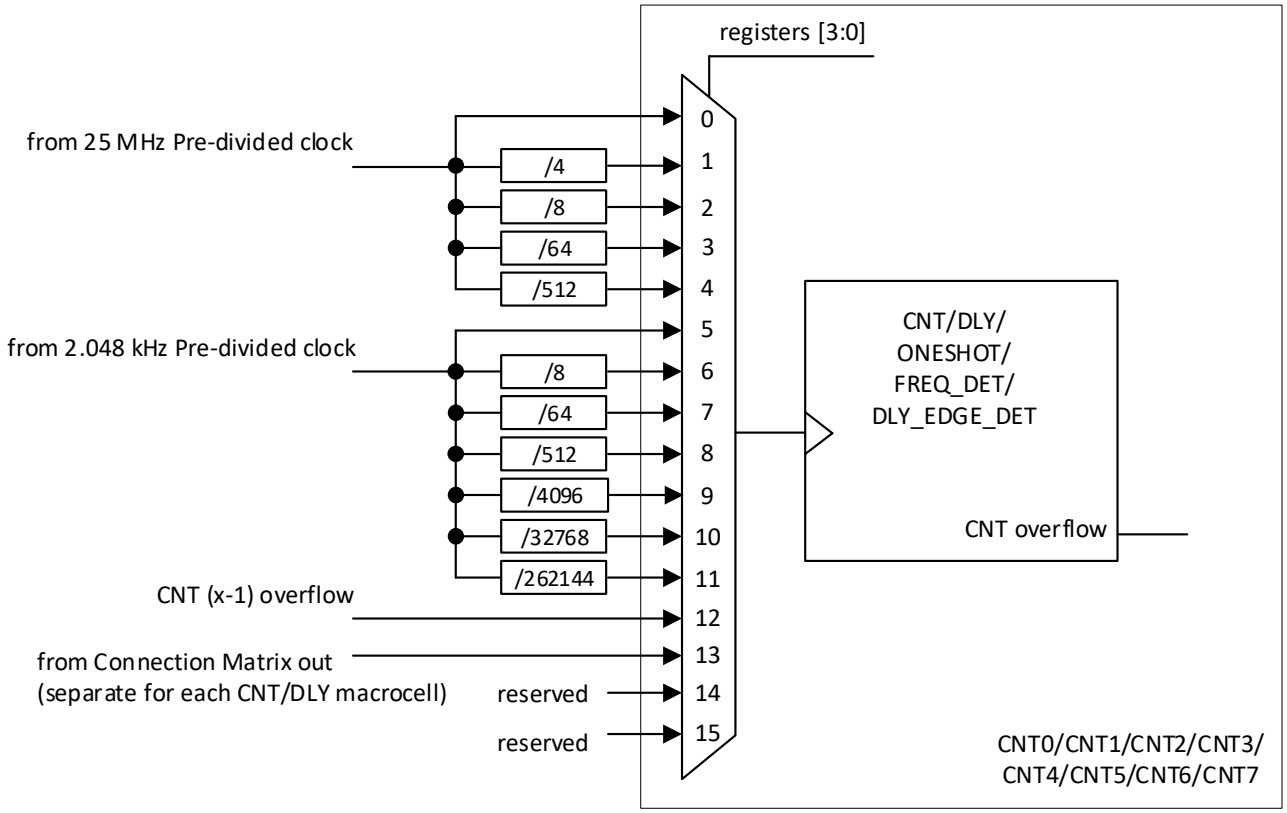


Figure 88: Clock Scheme

13.5 EXTERNAL CLOCKING

The SLG47512/13 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

13.5.1 GPIO Source for Oscillator0 (2.048 kHz)

When register [1448] is set to 1, an external clocking signal on GPIOx will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 86. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

13.5.2 GPIO Source for Oscillator1 (25 MHz)

When register [1456] is set to 1, an external clocking signal on GPIOx will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 87.

13.6 OSCILLATORS ACCURACY

Note: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

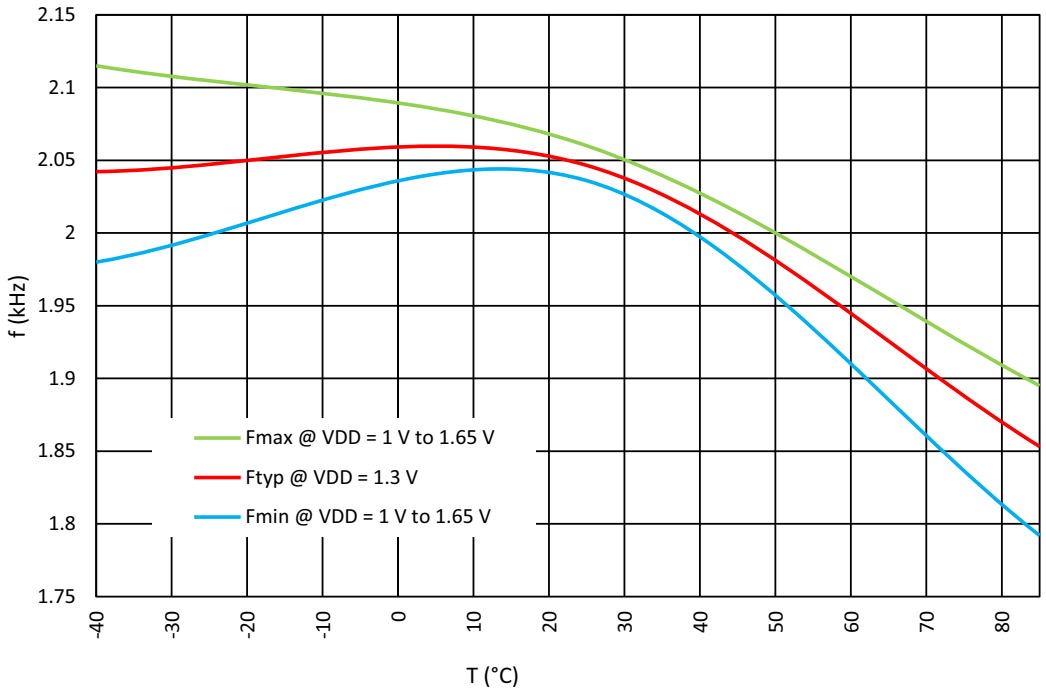


Figure 89: Oscillator0 Frequency vs. Temperature, OSC0 = 2.048 kHz

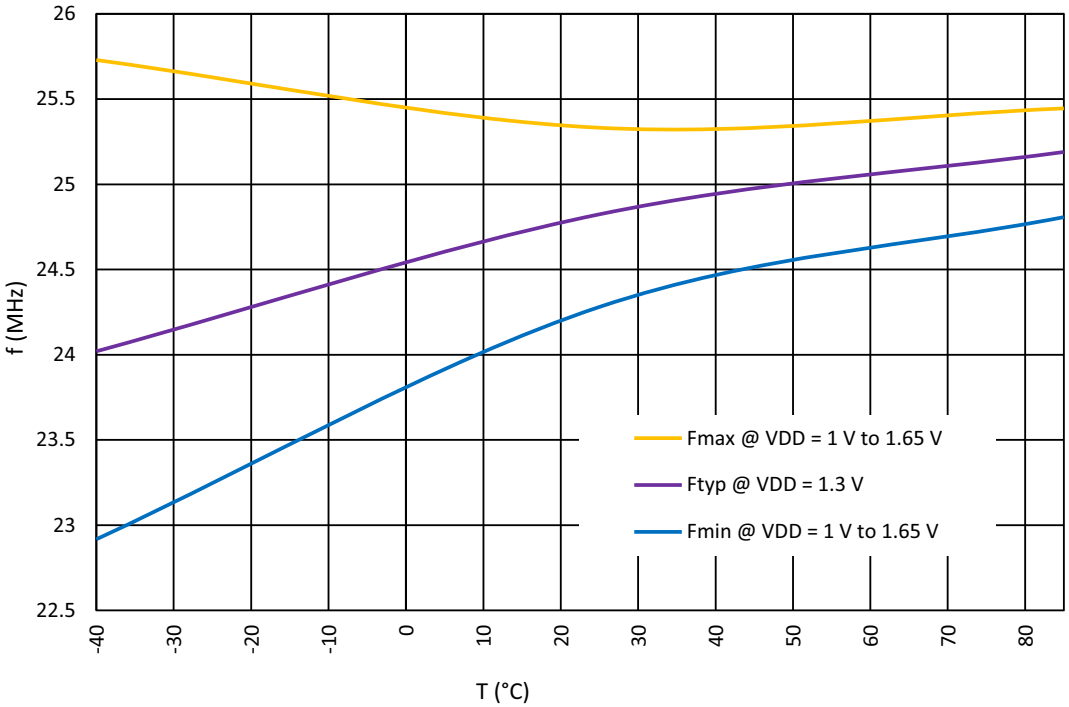


Figure 90: Oscillator1 Frequency vs. Temperature, OSC1 = 25 MHz

Note: For more information see Section 3.9.

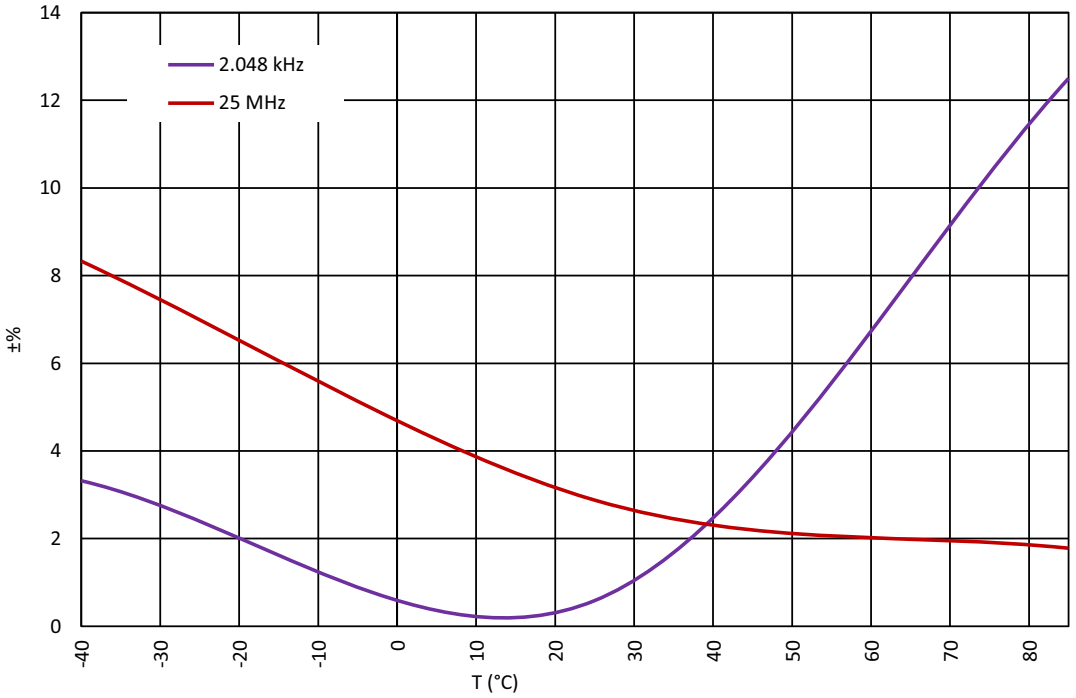


Figure 91: Oscillators Total Error vs. Temperature, V_{DD} = 1.0 V to 1.65 V

13.7 OSCILLATORS SETTLING TIME

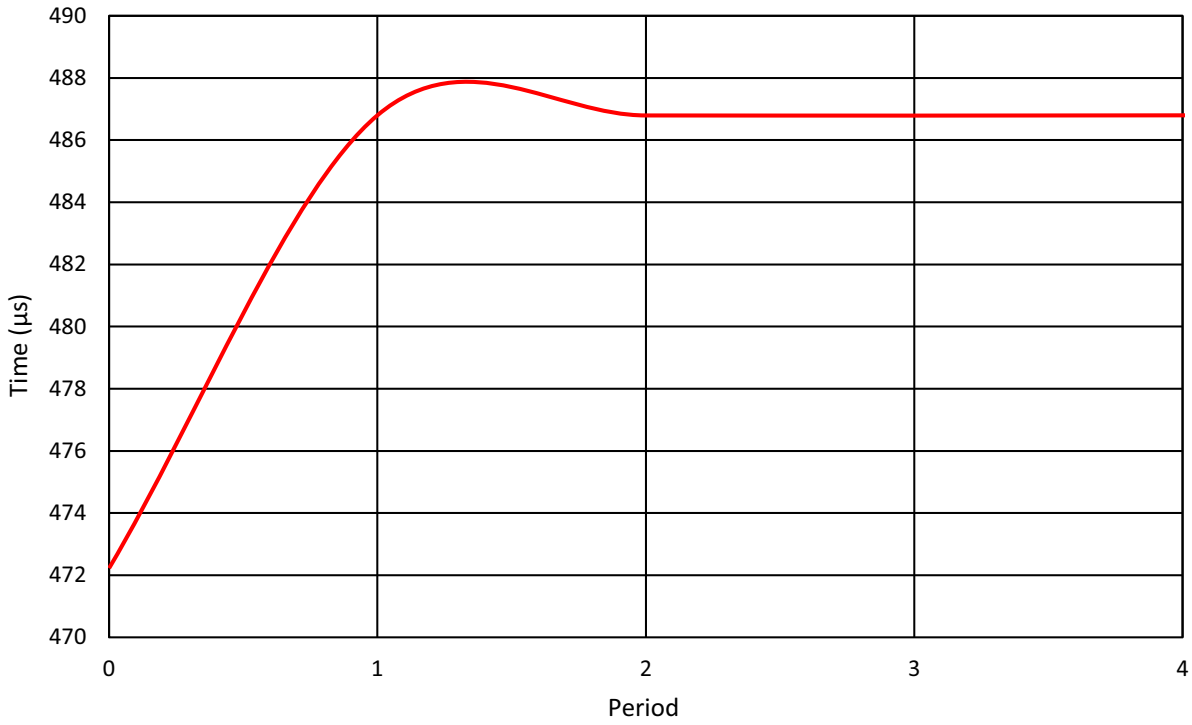


Figure 92: Oscillator0 Settling Time, V_{DD} = 1.2 V, T = 25 °C, OSC0 = 2.048 kHz

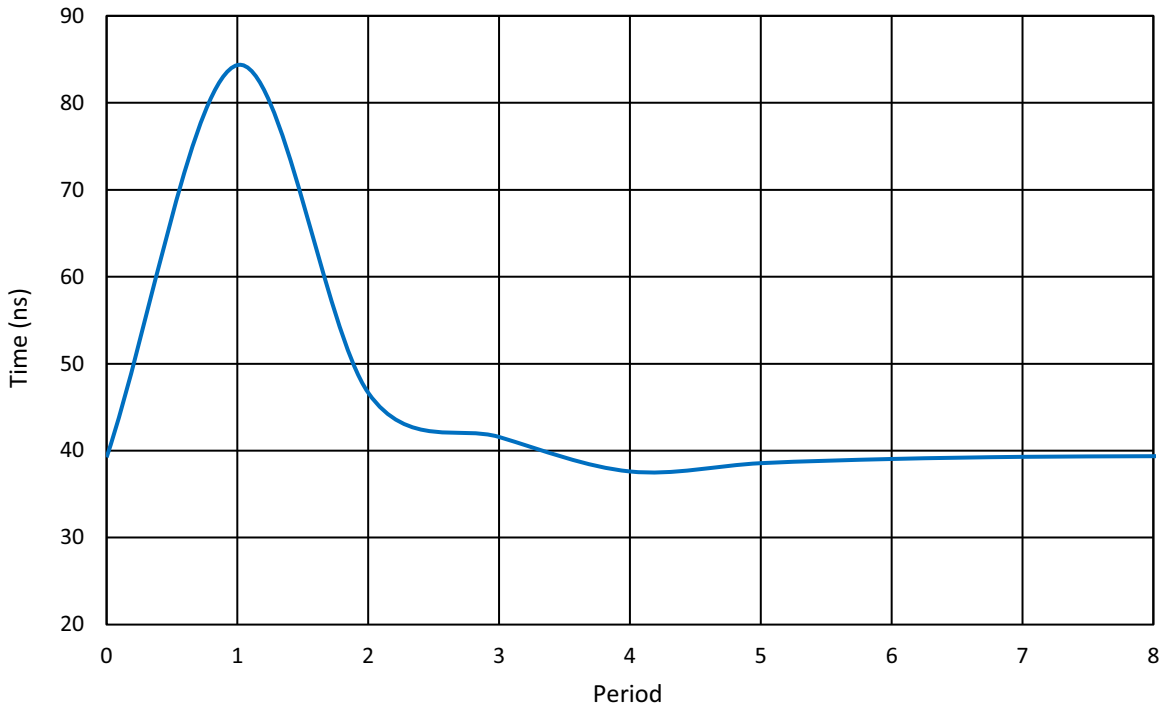


Figure 93: Oscillator1 Settling Time, V_{DD} = 1.2 V, T = 25 °C, OSC1 = 25 MHz (Normal Start)

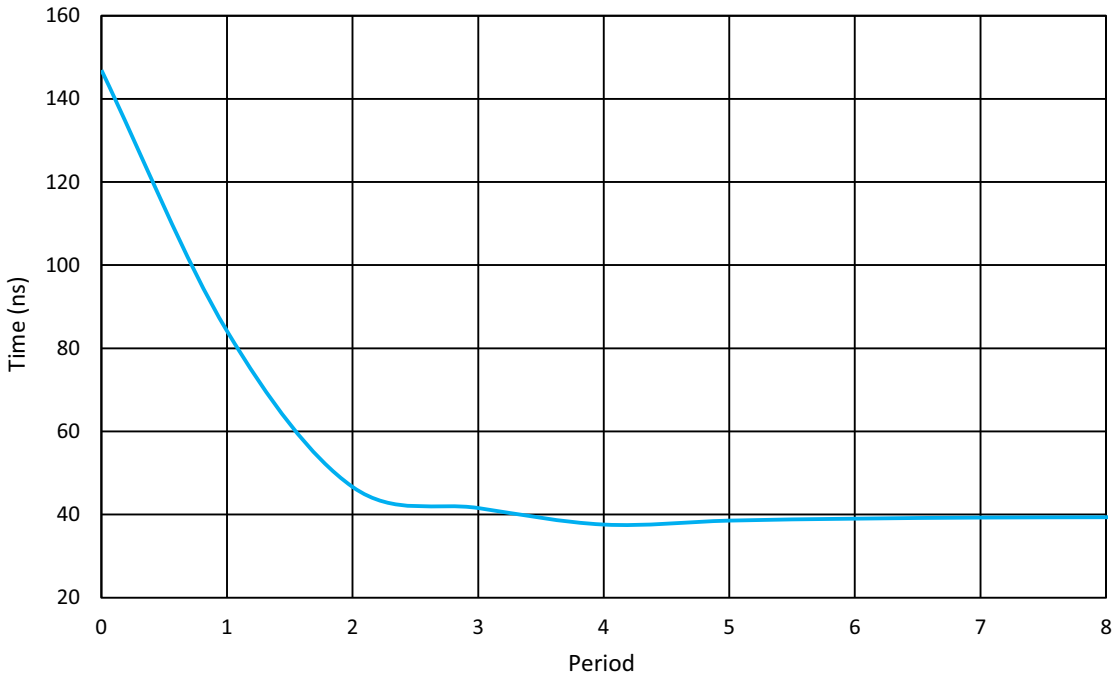


Figure 94: Oscillator1 Settling Time, V_{DD} = 1.2 V, T = 25 °C, OSC1 = 25 MHz (Start with Delay)

14 Power-On Reset

The SLG47512/13 has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

14.1 GENERAL OPERATION

The SLG47512/13 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on PIN1) is less than Power-Off Threshold (see in Table 6), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG47512/13, the voltage applied on the V_{DD} should be higher than the Power-On Threshold (Note). The full operational V_{DD} range for the SLG47512/13 is 1.0 V to 1.65 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On Threshold. After the POR sequence has started, the SLG47512/13 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device) and will be ready and completely operational after the POR sequence is complete.

Note: The Power-On Threshold is defined in Table 5.

To power down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

14.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 95.

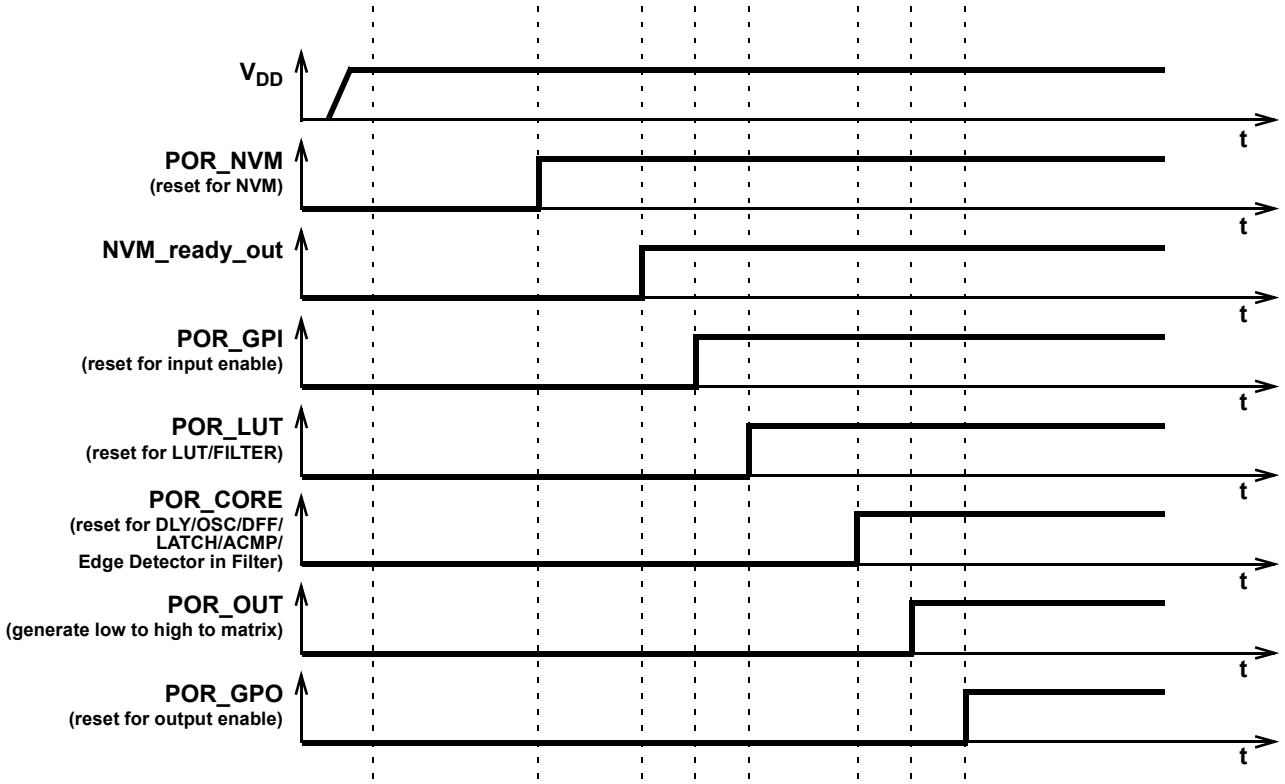


Figure 95: POR Sequence

As can be seen from Figure 95 after the V_{DD} has start ramping up and crosses the Power-On Threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to a CMOS LATCH, that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, and LATCHES are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

14.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG47512/13 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 96 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input pins are enabled.

Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

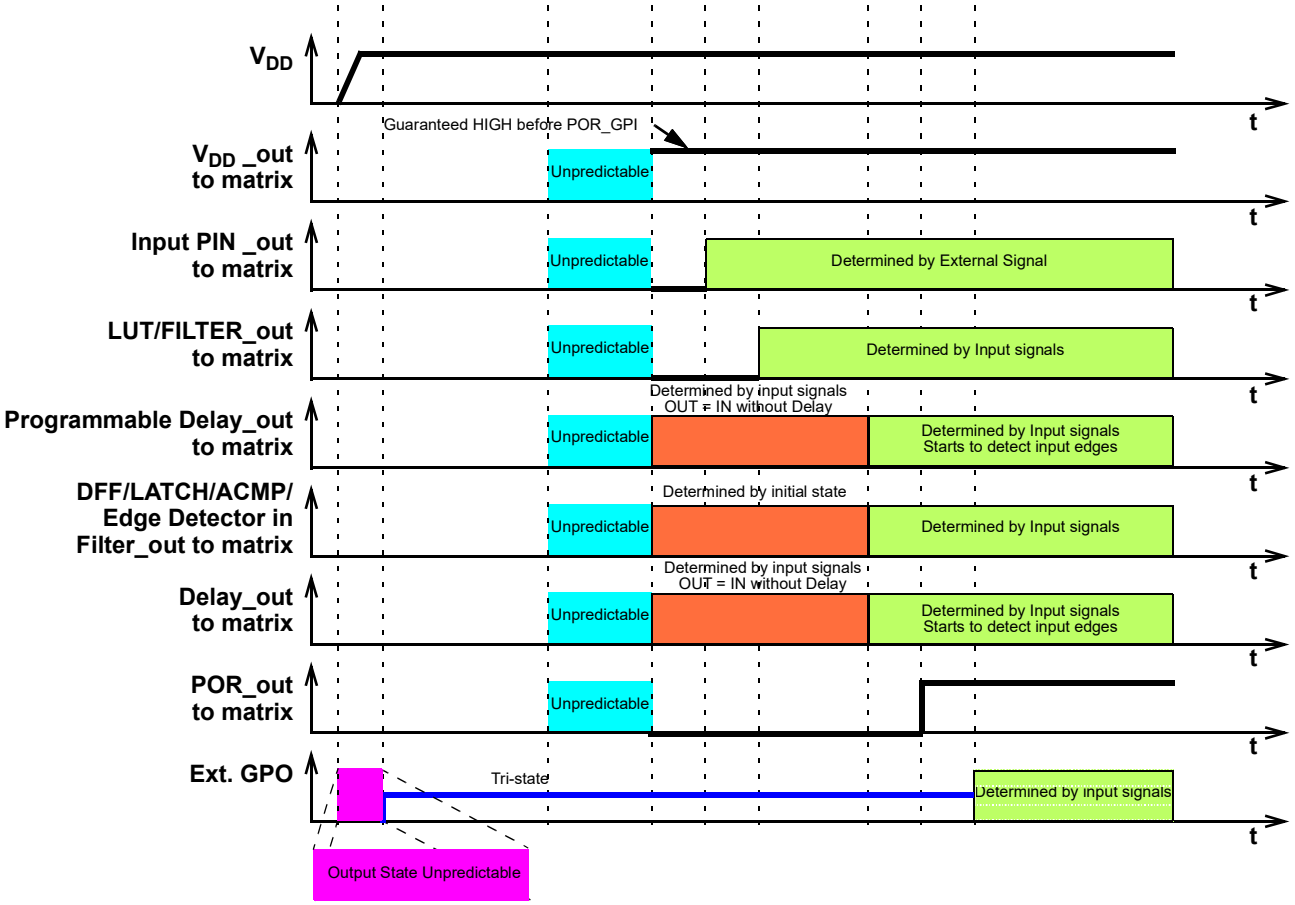


Figure 96: Internal Macrocell States During POR Sequence

14.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 0.811 V to 1.078 V, macrocells in SLG47512/13 are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, ACMP, Pull-up/down.
2. LUTs.
3. DFFs, Delays/Counters.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin →V_{DD} and pin → GND on each pin. So, if the input signal applied to pin is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

14.3.2 Power-Down

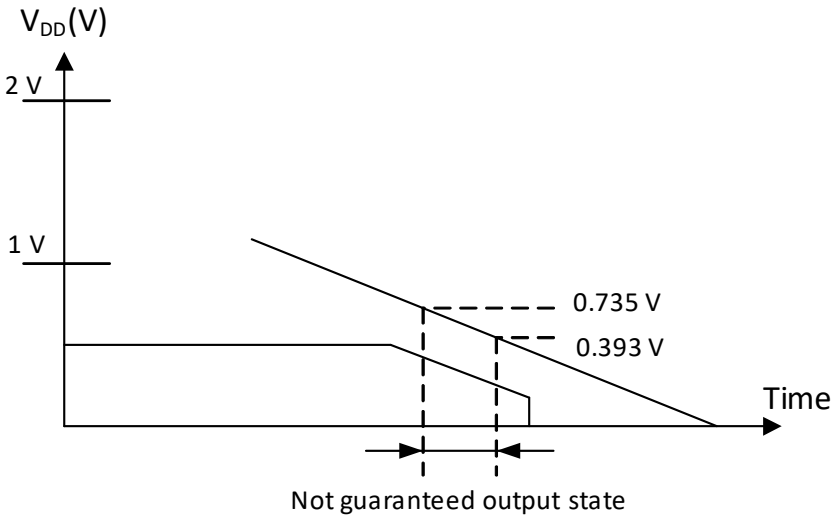


Figure 97: Power-Down

During Power-down, macrocells in SLG47512/13 are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

15 I²C Serial Communications Macrocell

15.1 I²C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

The I²C bus Master is also able to read and write other register bits that are not associated with NVM memory.

The user has the flexibility to control read access and write access via registers bits registers [1723:1720]. See Section 15.5 for more details on I²C read/write memory protection.

It is possible to use I²C in Standard/fast mode or Fast mode+. To use I²C in Fast mode+ registers [1312], [1328] should be enabled.

Note that extra current consumption can occur if I²C transaction was corrupted and Stop condition was not received. Next correct I²C transaction restores normal current consumption.

15.2 I²C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 98. After the Start bit, the next seven bits are a control code. The four MSB in a control code can be sourced independently from the register or by value defined externally by GPI, GPIO3, GPIO4, and GPIO8. The bit4 of the control code is defined by the value of GPI, while the bit7 is defined by the value of GPIO8. The address source (either register bit or PIN) for each bit is defined by registers [30:24]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the first 4 bits of a device address to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG47512/13 are in the range from 0 (0x00) to 255 (0xFF).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 98 shows this basic command structure.

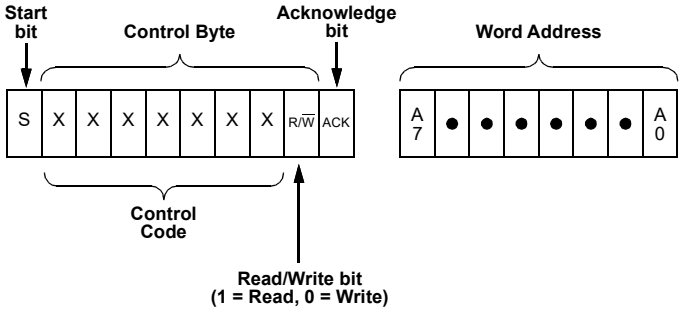


Figure 98: Basic Command Structure

15.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 99. Timing specifications can be found in the AC Characteristics section.

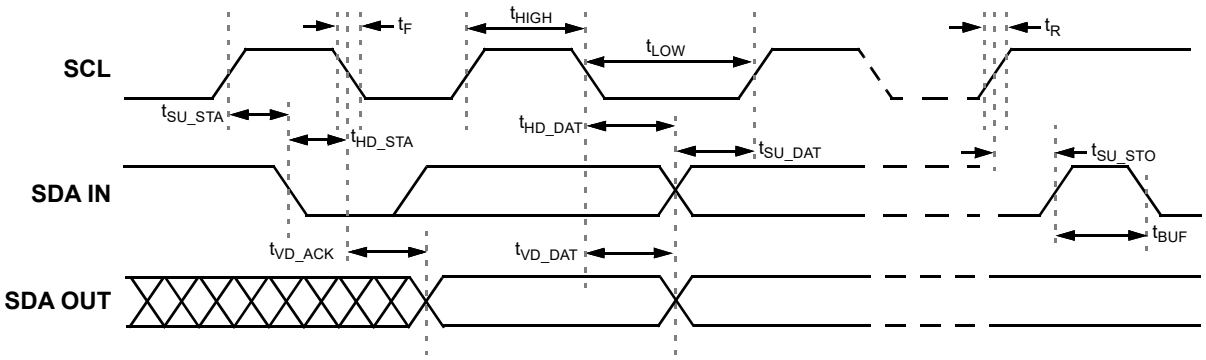


Figure 99: I²C General Timing Characteristics

15.4 I²C SERIAL COMMUNICATIONS COMMANDS

15.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [7 bits], and the R/W bit (set to “0”), are placed onto the I²C bus by the Master. After the SLG47512/13 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Word Address (A7 through A0) set the internal address pointer in the SLG47512/13, where the data byte is to be written. After the SLG47512/13 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG47512/13 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG47512/13 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [1425] = 1 - Enable. It means that IOs will remain their state until the write command is done.

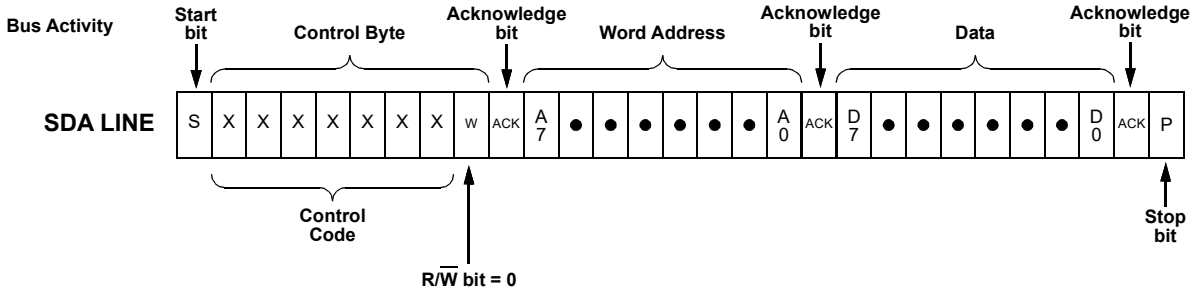


Figure 100: Byte Write Command, R/$\overline{W}$ = 0

15.4.2 Sequential Write Command

The write Control Byte, Word Address and the first data byte are transmitted to the SLG47512/13 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG47512/13. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG47512/13 generates the Acknowledge bit.

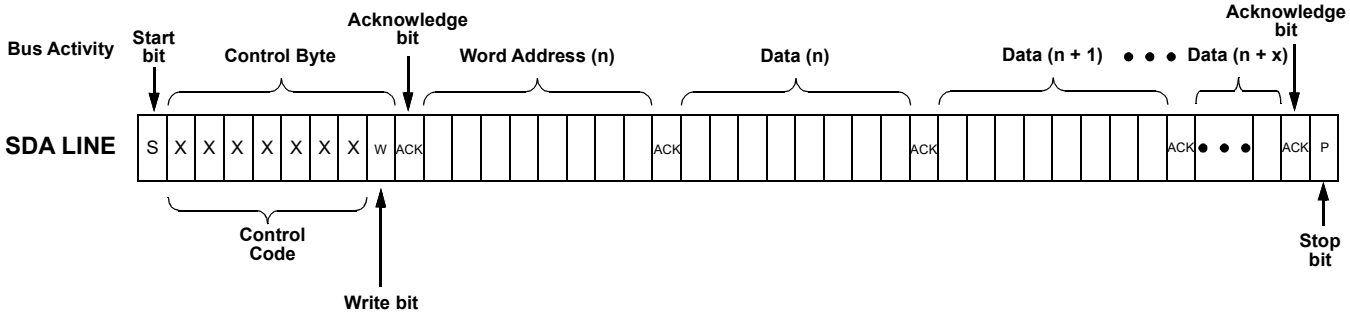


Figure 101: Sequential Write Command

15.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/W bit = “1”. The SLG47512/13 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

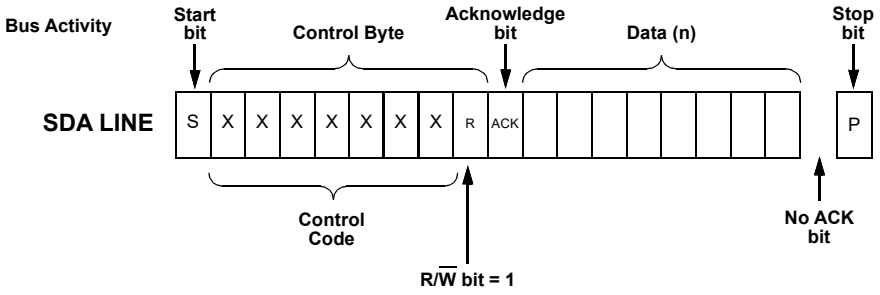


Figure 102: Current Address Read Command, R/W = 1

15.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG47512/13 issues an Acknowledge bit, followed by the requested eight data bits.

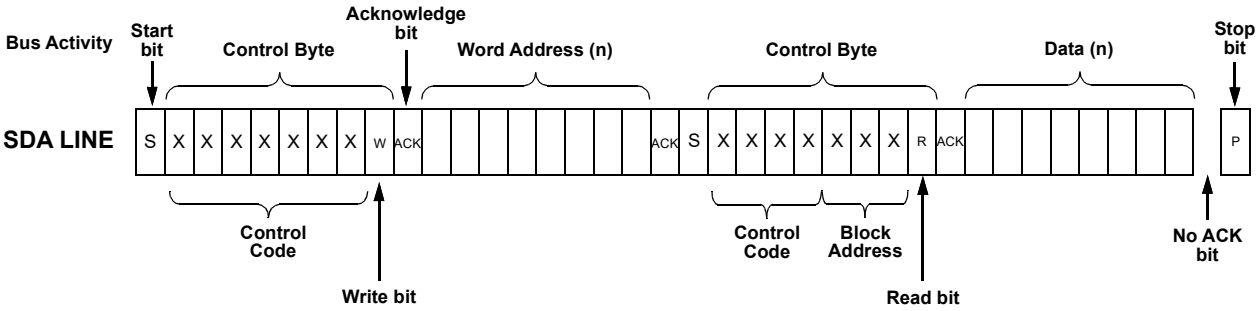


Figure 103: Random Read Command

15.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG47512/13 transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

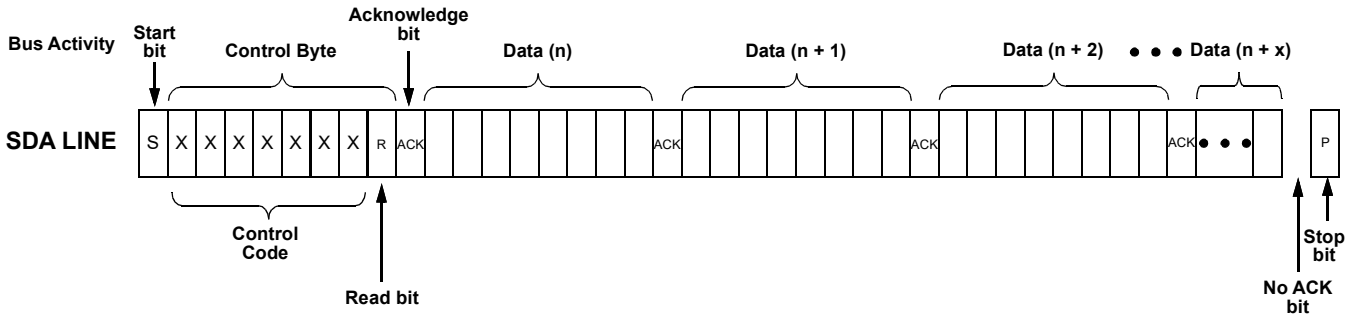


Figure 104: Sequential Read Command

15.4.6 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [17:16] I²C reset bit to "1", which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [17:16] will be set to "0" automatically. Figure 105 illustrates the sequence of events for this reset function.

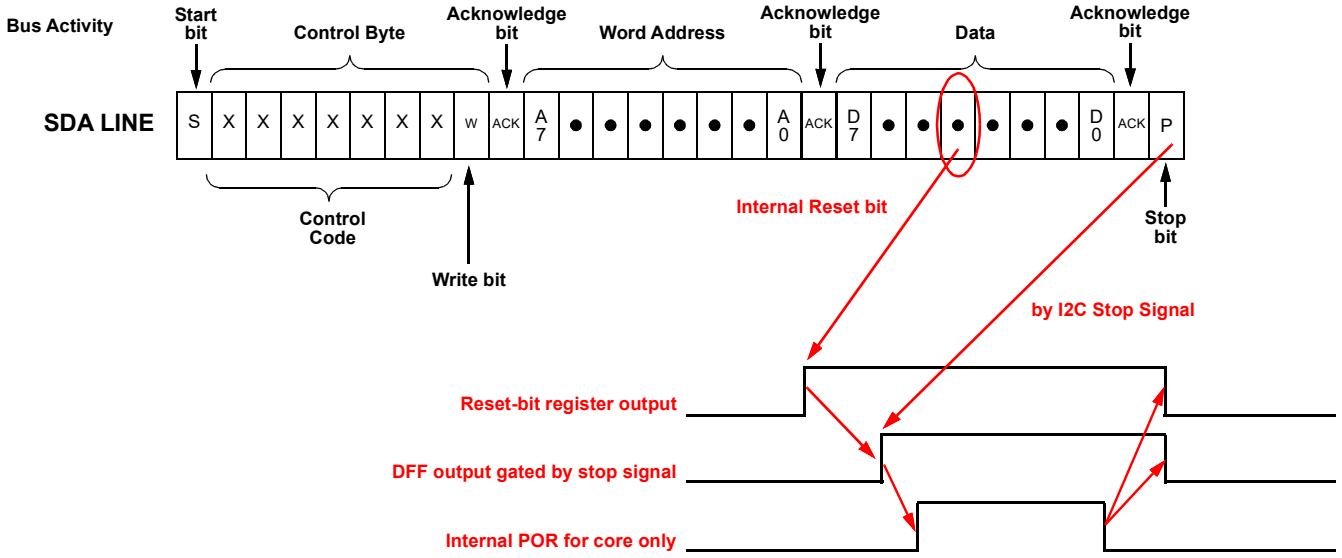


Figure 105: Reset Command Timing

15.4.7 I²C Additional Options

When Output latching during I²C write, register [1425] = 1 allows all PINs output value to be latched until I²C write is done. It will protect the output change due to configuration process during I²C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I²C write.

If the user sets GPIO0 and GPIO1 function to a selection other than SDA and SCL, all access via I²C will be disabled.

Note: Any write commands that come to the device via I²C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See Section 17 for detailed information on all registers.

15.4.8 Reading Counter Data via I²C

The current count value in all counters in the device can be read via I²C.

15.4.9 I²C Byte Write Bit Masking

The I²C macrocell inside SLG47512/13 supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 15.4.1 for details) on the I²C Byte Write Mask Register (address 0F6H) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to "1" in the I²C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I²C Byte Write Mask Register are reset (set to

00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I²C Byte Write Mask Register will be reset with no effect. Figure 106 shows an example of this function.

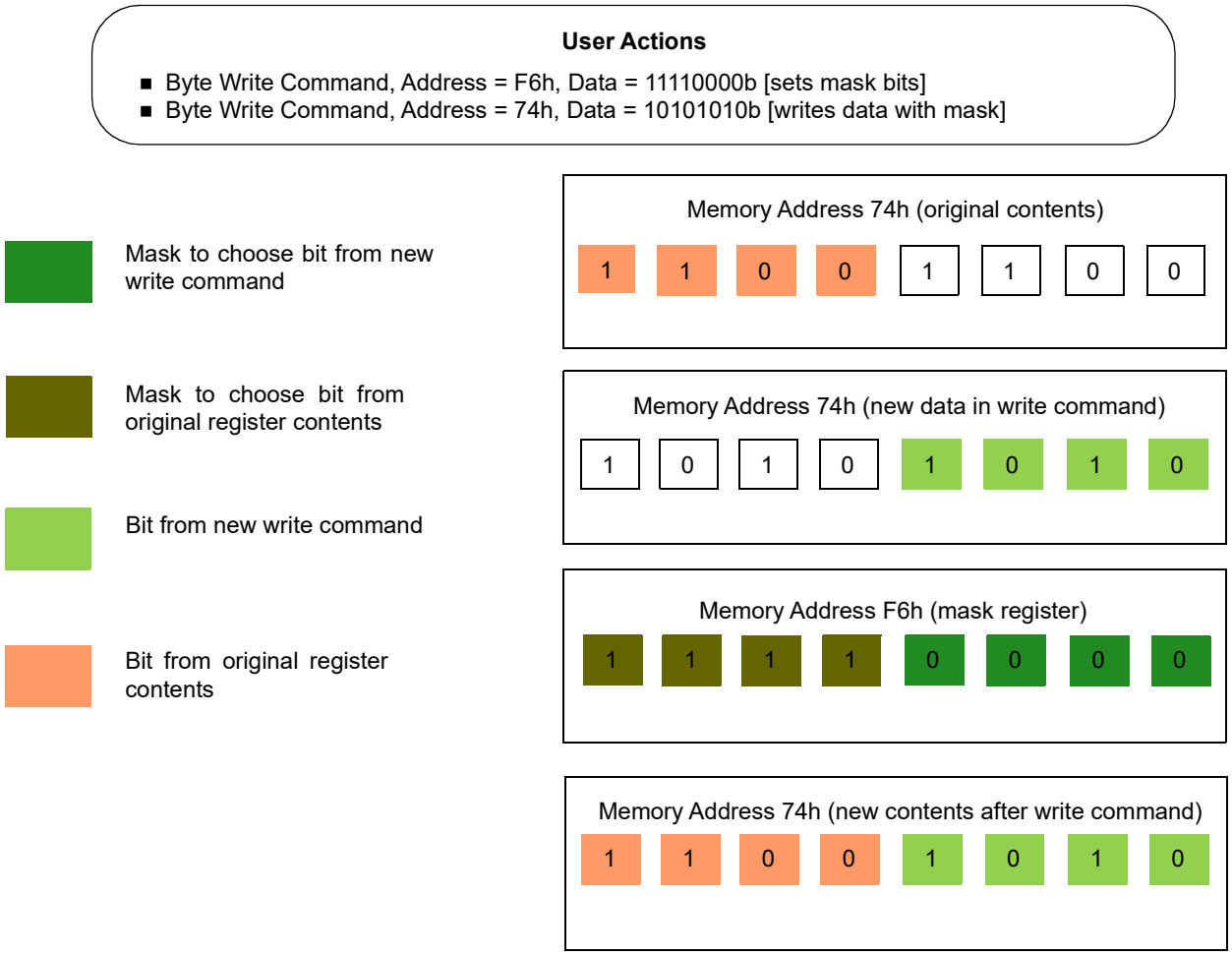


Figure 106: Example of I²C Byte Write Bit Masking

15.4.10 Writing a New Value to the Shift Register via I²C

The new value can be written to the Shift Register if low logic level presents at the CLK input of the macrocell. Otherwise, if the logic level at CLK input is high, the new value will be ignored.

It's recommended to perform the following actions to write the new value to the Shift Register:

- Read Shift Register value (Old_Value);
- Write new Shift Register value;
- Read Shift Register value (New_Value) and compare it with the result of the last read (Old_Value). If New_Value isn't equal to the Old_Value, the writing procedure was successful. Otherwise, if New_Value is equal to the Old_Value, the content of the Shift Register hasn't been updated (the logic level at the CLK input is high). I²C master should perform the following steps:
  - Connect the CLK input of the Shift Register to the GND (connect the corresponding matrix output to the matrix input x00);
  - Analyze the LSB, if the new value to be written to the Shift Register, for example xxxx xxx(y). y is the LSB of the 8-bit value to be written to the Shift Register.

If (y) is 0, then connect D input of the Shift Register to GND (connect the corresponding matrix output to the matrix input x00);
If (y) is 1, then connect D input of the Shift Register to V_{DD} (connect the corresponding matrix output to the matrix input x3F);

- Shift the new value to one bit right and write it to the Shift Register, for example if the data to be written to the Shift Register is x5A (1010 0101), then the I^2C master should write x52 (01010010) to the Shift Register.
- Connect CLK input of the Shift Register to its original source (change the matrix output setting from x00 to original source code). This will clock the Shift Register to one bit left.
- Connect D input of the Shift Register to its original source (change the matrix output setting from V_{DD} (x3F) or GND (x00) to the original source code).

15.5 I^2C SERIAL COMMAND REGISTER MAP

There are seven read/write protect modes for the design sequence from being corrupted or copied. See Table 37 for details.

Table 37: Read/Write Protection Options

Configurations	Protection Modes Configuration									Data Output From	Register Address
	Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/ Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/ Write		
RPR[1:0]	**00**	**01**	**00**	**01**	**01**	**10**	**10**	**00**	**10**		
WPR[1:0]	**00**	**00**	**01**	**01**	**10**	**01**	**00**	**10**	**10**		
I^2C Write Mask Control Register (section 15.4.9)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Memory	00
I^2C Virtual Input Control Register (section 6.3)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Macro-cell	01
I^2C Reset Control Register (section 15.4.6)	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Memory	02
I^2C Configuration Register	R/W	R/W	R	R	R	R	R/W	R	R	Memory	03~04
Matrix Output Configuration (section 6.2)	R/W	W	R	-	-	-	W	R	-	Memory	05~4E
Combination Function Macrocell Configuration	R/W	W	R	-	-	-	W	R	-	Memory	4F~6C
Multi-Function Macrocell Configuration	R/W	W	R	-	-	-	W	R	-	Memory	6D~A1
IO Configuration	R/W	W	R	-	-	-	W	R	-	Memory	A2~B2
OSC, ACMP, Vref Configuration	R/W	W	R	-	-	-	W	R	-	Memory	B3~C0

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as counter current value, connection matrix, and connection matrix virtual inputs. The I^2C write will not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allows identifying silicon family, its revision, and others.

See Section 17 for detailed information on all registers.

16 Analog Temperature Sensor

The SLG47512/13 has an Analog Temperature Sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS cell shares buffer with Vref 0, so it is impossible to use both cells simultaneously, its output can be connected directly to the GPIO or to the ACPM1_H positive input. Using buffer causes low-output impedance, linear output and makes interfacing to readout or control circuitry especially easy. The TS is rated to operate over a -40 °C to 85 °C temperature range. The error in the whole temperature range does not exceed ±2.5 %. TS output voltage variation over V_{DD} at constant temperature is less than ±1.5 %. When changing power-down source settings or enable temperature sensor settings in the Analog Temperature Sensor block, similar changes of these settings automatically occur in the Voltage Reference block. For more details refer to section 3.11.

The equation below calculates the typical analog voltage passed from the TS to the ACMPs' IN+ source input. It is important to note that there will be a chip to chip variation of about ±2 °C.

$$V_{TS} = -1.95 \times T + 734$$

where:

V_{TS} (mV) - TS Output Voltage

T (°C) - Temperature

Temperature hysteresis can be setup by enabling the GreenPAK's internal ACMP hysteresis.

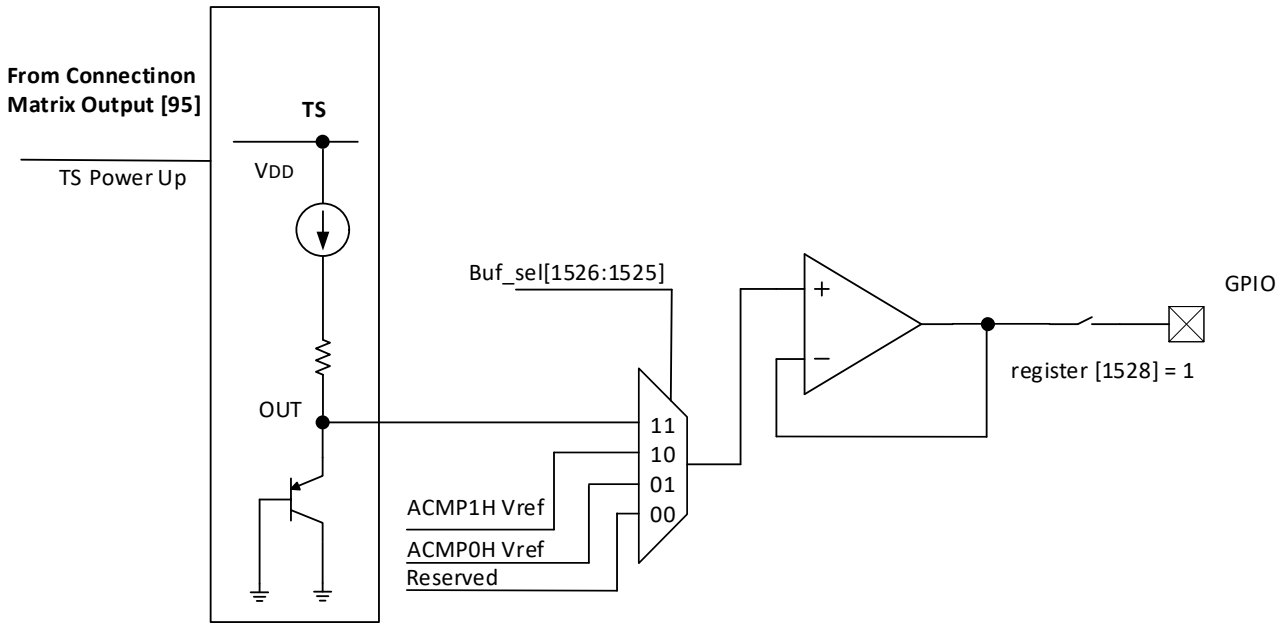


Figure 107: Analog Temperature Sensor Structure Diagram

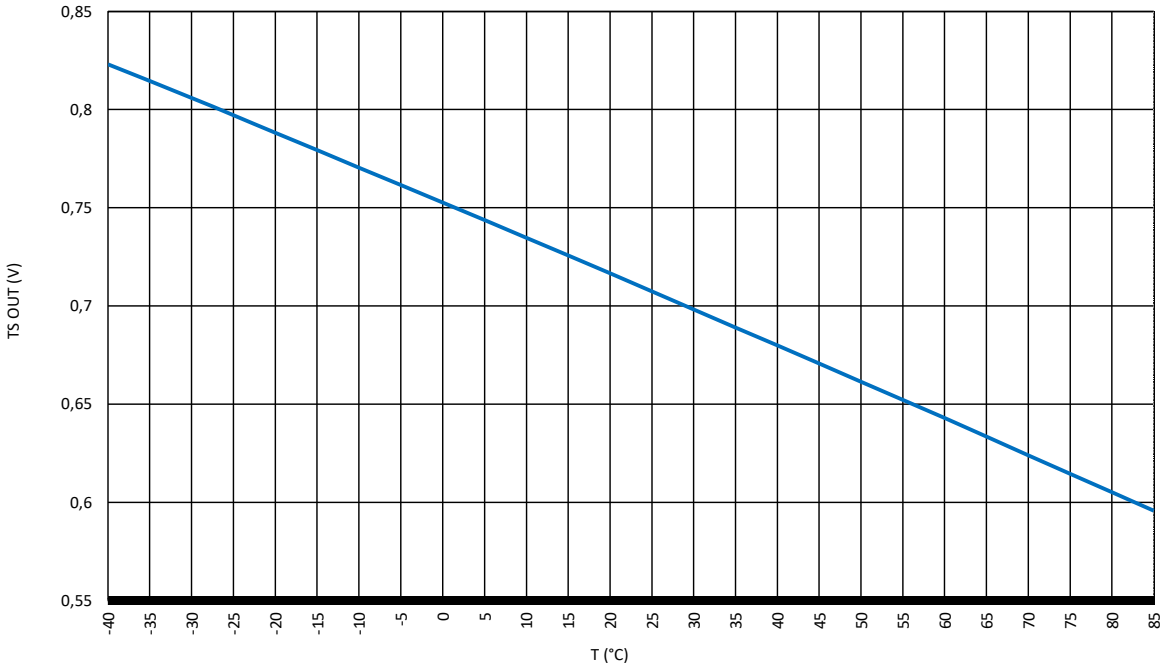


Figure 108: TS Output vs. Temperature, V_{DD} = 1.0 V to 1.65 V

17 Register Definitions

17.1 REGISTER MAP

Table 38: Register Map

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
Matrix Output			
0	0	I²C Write Mask Control	Host write data bit-mask: 0: write 1: mask (don't change) (This mask does not effect on NVM write and masks register update)
	1		
	2		
	3		
	4		
	5		
	6		
	7		
1	8	I²C Virtual Input Control	Host Virtual Input Bit 0
	9		Host Virtual Input Bit 1
	10		Host Virtual Input Bit 2
	11		Host Virtual Input Bit 3
	12		Host Virtual Input Bit 4
	13		Host Virtual Input Bit 5
	14		Host Virtual Input Bit 6
	15		Host Virtual Input Bit 7
2	16	I²C Reset Control	0: Normal 1: Reset (Self-Clear Bit. Shuts down device (simulates a Chip POR))
	17		Reserved
	18		Reserved
	19		Reserved
	20		Reserved
	21		Reserved
	22		Reserved
	23		Reserved
3	24	Reserved	
	25	Reserved	
	26	Reserved	
	27	I²C Slave Address	Bits [30:27] are I²C Slave Address. Bits [30:27] can be optional selected to GPIOx with I2C_CONTROL_CODE_BITx_SEL configuration
	28	I²C Slave Address	
	29	I²C Slave Address	
	30	I²C Slave Address	
	31	I²C Mode Enable	0: I2C mode disable 1: I2C mode enable

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
4	32	I^2C CONTROL CODE BIT3 SEL	0: Used I2C_CONTROL_CODE Value 1: Use SLA_0 Value
	33	I^2C CONTROL CODE BIT4 SEL	0: Used I2C_CONTROL_CODE Value 1: Use SLA_0 Value
	34	I^2C CONTROL CODE BIT5 SEL	0: Used I2C_CONTROL_CODE Value 1: Use SLA_0 Value
	35	I^2C CONTROL CODE BIT6 SEL	0: Used I2C_CONTROL_CODE Value 1: Use SLA_0 Value
	36		Reserved
	37		Reserved
	38		Reserved
	39		Reserved
5	40	LUT2_0 & DFF0	OUT0: IN0 of LUT2_0 or Clock Input of DFF0 or Clock Input of Shift_Reg0
	41		
	42		
	43		
	44		
	45		
	46		OUT1: IN1 of LUT2_0 or Data Input of DFF0 or Data Input of Shift_Reg0
	47		
6	48		
	49		
	50		
	51		
	52	LUT2_1 & DFF1	OUT2: IN0 of LUT2_1 or Clock Input of DFF1 or Clock Input of Shift_Reg1
	53		
	54		
	55		
7	56		
	57		
	58		OUT3: IN1 of LUT2_1 or Data Input of DFF1 or Data Input of Shift_Reg1
	59		
	60		
	61		
	62		
	63		
8	64	LUT2_2 & DFF2	OUT4: IN0 of LUT2_2 or Clock Input of DFF2 or Clock Input of Shift_Reg2
	65		
	66		
	67		
	68		
	69		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
8	70	LUT2_2 & DFF2	OUT5: IN1 of LUT2_2 or Data Input of DFF2 or Data Input of Shift_Reg2
	71		
9	72		
	73		
	74		
	75		
	76	LUT2_3 & PGen	OUT6: IN0 of LUT2_3 or Clock Input of PGen0
	77		
	78		
	79		
A	80		OUT7: IN1 of LUT2_3 or nRST of PGen0
	81		
	82		
	83		
	84		
	85		
	86		
	87		
B	88	LUT3_0 & DFF3	OUT8: IN0 of LUT3_0 or Clock Input of DFF3 or Clock Input of Shift_Reg3
	89		
	90		
	91		
	92		
	93		
	94		OUT9: IN1 of LUT3_0 or Data Input of DFF3 or Data Input of Shift_Reg3
	95		
C	96		
	97		
	98		
	99		
	100		OUT10: IN2 of LUT3_0 or nRST(nSET) of DFF3 or nRST (nSET) of Shift_Reg3
	101		
	102		
	103		
D	104		
	105		
	106	LUT3_1 & DFF4	OUT11: IN0 of LUT3_1 or Clock Input of DFF4 or Clock Input of Shift_Reg4
	107		
	108		
	109		
	110		
	111		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
E	112	LUT3_1 & DFF4	OUT12: IN1 of LUT3_1 or Data Input of DFF4 or Data Input of Shift_Reg4
	113		
	114		
	115		
	116		
	117		
	118		OUT13: IN2 of LUT3_1 or nRST (nSET) of DFF4 or nRST(nSET) of Shift_Reg4
	119		
F	120		
	121		
	122		
	123		
	124	LUT3_2 & DFF5	OUT14: IN0 of LUT3_2 or Clock Input of DFF5 or Clock Input of Shift_Reg5
	125		
	126		
	127		
10	128		
	129		
	130		OUT15: IN1 of LUT3_2 or Data Input of DFF5 or Data Input of Shift_Reg5
	131		
	132		
	133		
	134		
	135		
11	136		OUT16: IN2 of LUT3_2 or nRST(nSET) of DFF5 or nRST(nSET) of Shift_Reg5
	137		
	138		
	139		
	140		
	141		
	142	LUT3_3 & DFF6	OUT17: IN0 of LUT3_3 or Clock Input of DFF6 or Clock Input of Shift_Reg6
	143		
12	144		
	145		
	146		
	147		
	148		OUT18: IN1 of LUT3_3 or Data Input of DFF6 or Data Input of Shift_Reg6
	149		
	150		
	151		
13	152		
	153		
	154		OUT19: IN2 of LUT3_3 or nRST(nSET) of DFF6 or nRST(nSET) of Shift_Reg6
	155		
	156		
	157		
	158		
	159		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
14	160	LUT3_4 & DFF7	OUT20: IN0 of LUT3_4 or Clock Input of DFF7 or Clock Input of Shift_Reg7
	161		
	162		
	163		
	164		
	165		
	166		OUT21: IN1 of LUT3_4 or Data Input of DFF7 or Data Input of Shift_Reg7
	167		
15	168		
	169		
	170		
	171		
	172		OUT22: IN2 of LUT3_4 or nRST(nSET) of DFF7 or nRST(nSET) of Shift_Reg7
	173		
	174		
	175		
16	176		
	177		
	178	LUT3_5 & DFF8	OUT23: IN0 of LUT3_5 or Clock Input of DFF8 or Clock Input of Shift_Reg8
	179		
	180		
	181		
	182		
	183		
17	184		OUT24: IN1 of LUT3_5 or Data Input of DFF8 or Data Input of Shift_Reg8
	185		
	186		
	187		
	188		
	189		
	190		OUT25: IN2 of LUT3_5 or nRST(nSET) of DFF8 or nRST(nSET) of Shift_Reg8
	191		
18	192		
	193		
	194		
	195		
	196	LUT3_6 & DFF9	OUT26: IN0 of LUT3_6 or Clock Input of DFF9 or Clock Input of Shift_Reg9
	197		
	198		
	199		
19	200		
	201		
	202		OUT27: IN1 of LUT3_6 or Data Input of DFF9 or Data Input of Shift_Reg9
	203		
	204		
	205		
	206		
	207		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1A	208	LUT3_6 & DFF9	OUT28: IN2 of LUT3_6 or nRST(nSET) of DFF9 or nRST(nSET) of Shift_Reg9
	209		
	210		
	211		
	212		
	213		
	214	LUT3_7 & DFF10	OUT29: IN0 of LUT3_7 or Clock Input of DFF10 or Clock Input of Shift_Reg10
	215		
1B	216		
	217		
	218		
	219		
	220		OUT30: IN1 of LUT3_7 or Data Input of DFF10 or Data Input of Shift_Reg10
	221		
	222		
	223		
1C	224		
	225		
	226		
	227		OUT31: IN2 of LUT3_7 or nRST(nSET) of DFF10 or nRST(nSET) of Shift_Reg10
	228		
	229		
	230		
	231		
1D	232	LUT3_8 & DFF11	OUT32: IN0 of LUT3_8 or Clock Input of DFF11 or Clock Input of Shift_Reg11
	233		
	234		
	235		
	236		
	237		
	238		OUT33: IN1 of LUT3_8 or Data Input of DFF11 or Data Input of Shift_Reg11
	239		
1E	240		
	241		
	242		
	243		
	244		OUT34: IN2 of LUT3_8 or nRST(nSET) of DFF11 or nRST(nSET) of Shift_Reg11
	245		
	246		
	247		
1F	248		
	249		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
1F	250	LUT3_9 & DFF12	OUT35: IN0 of LUT3_9 or Clock Input of DFF12 or Clock Input of Shift_Reg12
	251		
	252		
	253		
	254		
	255		
20	256		OUT36: IN1 of LUT3_9 or Data Input of DFF12 or Data Input of Shift_Reg12
	257		
	258		
	259		
	260		
	261		
	262		OUT37: IN2 of LUT3_9 or nRST(nSET) of DFF12 or nRST(nSET) of Shift_Reg12
	263		
21	264		
	265		
	266		
	267		
	268	LUT4_0 & DFF13	OUT38: IN0 of LUT4_0 or Clock Input of DFF13 or Clock Input of Shift_Reg13
	269		
	270		
	271		
22	272		
	273		
	274		OUT39: IN1 of LUT4_0 or Data Input of DFF13 or Data Input of Shift_Reg13
	275		
	276		
	277		
	278		
	279		
23	280		
	281		
	282		OUT40: IN2 of LUT4_0 or nRST(nSET) of DFF13 or nRST(nSET) of Shift_Reg13
	283		
	284		
	285		
	286		
	287		
24	288		OUT41: IN3 of LUT4_0 or Clock Enable of DFF13 or Clock Enable of Shift_Reg13
	289		
	290		
	291		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
24	292	Multi-function0	OUT42: IN0 of MLT0_LUT4_1 or Clock Input of DFF14 or Delay0 Input (or Counter0 nRST Input)
	293		
	294		
	295		
25	296		OUT43: IN1 of MLT0_LUT4_1 or nRST of DFF14 or Delay0 Input (or Counter0 nRST Input or External Clock Source)
	297		
	298		
	299		
	300		
	301		
	302		
	303		
26	304		OUT44: IN2 of IN2 of MLT0_LUT4_1 or nSET of DFF14 or KEEP of Delay0/Counter0
	305		
	306		
	307		
	308		
	309		
	310		OUT45: IN3 of MLT0_LUT4_1 or Data Input of DFF14 or UP of Delay0/Counter0
	311		
27	312		
	313		
	314		
	315		
	316	Multi-function1	OUT46: IN0 of MLT1_LUT3_10 or Clock Input of DFF15 or Delay1 Input (or Counter1 nRST Input)
	317		
	318		
	319		
28	320		OUT47: IN1 of MLT1_LUT3_10 or nRST(nSET) of DFF15 or Delay1 Input (or Counter1 nRST Input or External Clock Source)
	321		
	322		
	323		
	324		
	325		
	326		
	327		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
29	328	Multi-function1	OUT48: IN2 of MLT1_LUT3_10 or Data Input of DFF15 or Delay1 Input (or Counter1 nRST Input)
	329		
	330		
	331		
	332		
	333		
	334	Multi-function2	OUT49: IN0 of MLT2_LUT3_11 or Clock Input of DFF16 or Delay2 Input (or Counter2 nRST Input)
	335		
2A	336		
	337		
	338		
	339		
	340		OUT50: IN1 of MLT2_LUT3_11 or nRST(nSET) of DFF16 or Delay2 Input (or Counter2 nRST Input or External Clock Source
	341		
	342		
	343		
2B	344		
	345		
	346		
	347		OUT51: IN2 of MLT2_LUT3_11 or Data Input of DFF16 or Delay2 Input (or Counter2 nRST Input)
	348		
	349		
	350		
	351		
2C	352	Multi-function3	OUT52: IN0 of MLT3_LUT3_12 or Clock Input of DFF17 or Delay3 Input (or Counter3 nRST Input)
	353		
	354		
	355		
	356		
	357		
	358		OUT53: IN1 of MLT3_LUT3_12 or nRST(nSET) of DFF17 or Delay3 Input (or Counter3 nRST Input or External Clock Source)
	359		
2D	360		
	361		
	362		
	363		
	364		OUT54: IN2 of MLT3_LUT3_12 or Data Input of DFF17 or Delay3 Input (or Counter3 nRST Input)
	365		
	366		
	367		
2E	368		
	369		
	370	Multi-function4	OUT55: IN0 of MLT4_LUT3_13 or Clock Input of DFF18 or Delay4 Input (or Counter4 nRST Input)
	371		
	372		
	373		
	374		
	375		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
2F	376	Multi-function4	OUT56: IN1 of MLT4_LUT3_13 or nRST(nSET) of DFF18 or Delay4 Input (or Counter4 nRST Input or External Clock Source
	377		
	378		
	379		
	380		
	381		
	382		OUT57: IN2 of MLT4_LUT3_13 or Data Input of DFF18 or Delay4 Input (or Counter4 nRST Input)
	383		
30	384		
	385		
	386		
	387		
	388	Multi-function5	OUT58: IN0 of MLT5_LUT3_14 or Clock Input of DFF19 or Delay5 Input (or Counter5 nRST Input)
	389		
	390		
	391		
31	392		
	393		
	394		
	395		OUT59: IN1 of MLT5_LUT3_14 or nRST(nSET) of DFF19 or Delay5 Input (or Counter5 nRST Input or External Clock Source)
	396		
	397		
	398		
	399		
32	400		
	401		
	402		OUT60: IN2 of MLT5_LUT3_14 or Data Input of DFF19 or Delay5 Input (or Counter5 nRST Input)
	403		
	404		
	405		
	406	Multi-function6	OUT61: IN0 of MLT6_LUT3_15 or Clock Input of DFF20 or Delay6 Input (or Counter6 nRST Input)
	407		
33	408		
	409		
	410		
	411		OUT62: IN1 of MLT6_LUT3_15 or nRST(nSET) of DFF20 or Delay6 Input (or Counter6 nRST Input or External Clock Source)
	412		
	413		
	414		
	415		
34	416		
	417		
	418		OUT63: IN2 of MLT6_LUT3_15 or Data Input of DFF20 or Delay6 Input (or Counter6 nRST Input)
	419		
	420		
	421		
	422		
	423		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
35	424	Multi-function7	OUT64: IN0 of MLT7_LUT3_16 or Clock Input of DFF21 or Delay7 Input (or Counter7 nRST Input)
	425		
	426		
	427		
	428		
	429		
	430		OUT65: IN1 of MLT7_LUT3_16 or nRST(nSET) of DFF21 or Delay7 Input (or Counter7 nRST Input or External Clock Source)
	431		
36	432		
	433		
	434		
	435		
	436		OUT66: IN2 of MLT7_LUT3_16 or Data Input of DFF21 or Delay7 Input (or Counter7 nRST Input)
	437		
	438		
	439		
37	440		
	441		
	442	GPIO0	OUT67: GPIO0 Digital Output
	443		
	444		
	445		
	446		
	447		
38	448	GPIO1	OUT68: GPIO1 Digital Output
	449		
	450		
	451		
	452		
	453		
	454	GPIO2	OUT69: GPIO2 Digital Output OE
	455		
39	456		
	457		
	458		
	459		
	460		OUT70: GPIO2 Digital Output
	461		
	462		
	463		
3A	464		
	465		
	466	GPIO3	OUT71: GPIO3 Digital Output OE
	467		
	468		
	469		
	470		
	471		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
3B	472	GPIO3	OUT72: GPIO3 Digital Output
	473		
	474		
	475		
	476		
	477		
	478	GPIO4	OUT73: GPIO4 Digital Output OE
	479		
3C	480		
	481		
	482		
	483		
	484		OUT74: GPIO4 Digital Output
	485		
	486		
	487		
3D	488		
	489		
	490	GPIO5	OUT75: GPIO5 Digital Output OE
	491		
	492		
	493		
	494		
	495		
3E	496		OUT76: GPIO5 Digital Output
	497		
	498		
	499		
	500		
	501		
	502	GPIO6	OUT77: GPIO6 Digital Output OE
	503		
3F	504		
	505		
	506		
	507		
	508		OUT78: GPIO6 Digital Output
	509		
	510		
	511		
40	512		
	513		
	514	GPIO7	OUT79: GPIO7 Digital Output OE
	515		
	516		
	517		
	518		
	519		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
41	520	GPIO7	OUT80: GPIO7 Digital Output
	521		
	522		
	523		
	524		
	525		
	526	GPIO8	OUT81: GPIO8 Digital Output OE
	527		
42	528		
	529		
	530		
	531		
	532		OUT82: GPIO8 Digital Output
	533		
	534		
	535		
43	536		
	537		
	538	GPIO9	OUT83: GPIO9 Digital Output OE (16-PIN Version)
	539		
	540		
	541		
	542		
	543		
44	544		OUT84: GPIO9 Digital Output (16-PIN Version)
	545		
	546		
	547		
	548		
	549		
	550	GPIO10	OUT85: GPIO10 Digital Output OE (16-PIN Version)
	551		
45	552		
	553		
	554		
	555		
	556		OUT86: GPIO10 Digital Output (16-PIN Version)
	557		
	558		
	559		
46	560		
	561		
	562	GPIO11	OUT87: GPIO11 Digital Output OE (16-PIN Version)
	563		
	564		
	565		
	566		
	567		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
47	568	GPIO11	OUT88: GPIO11 Digital Output (16-PIN Version)
	569		
	570		
	571		
	572		
	573		
	574	GPIO12	OUT89: GPIO12 Digital Output OE (16-PIN Version)
	575		
48	576		
	577		
	578		
	579		
	580		OUT90: GPIO12 Digital Output (16-PIN Version)
	581		
	582		
	583		
49	584		
	585		
	586	Filter/Edge detect	OUT91: Filter/Edge detect input
	587		
	588		
	589		
	590		
	591		
4A	592	Programmable delay/edge detect	OUT92: Programmable delay/edge detect input
	593		
	594		
	595		
	596		
	597		
	598	ACMP0H	OUT93: Power Up of ACMP0_H
	599		
4B	600		
	601		
	602		
	603		
	604	ACMP1H	OUT94: Power Up of ACMP1_H
	605		
	606		
	607		
4C	608		
	609		
	610	Temp sensor	OUT95: Temp sensor, Vref Out_0 Power Up
	611		
	612		
	613		
	614		
	615		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
4D	616	OSC0	OUT96: Oscillator0 (LFOSC) ENABLE
	617		
	618		
	619		
	620		
	621		
	622	OSC1	OUT97: Oscillator1 (RINGOSC) ENABLE
	623		
4E	624		
	625		
	626		
	627		
	628	Reserved	
	629	Reserved	
	630	Reserved	
	631	Reserved	
4F	632	LUT2_0_DFF0_SHR0	LUT2_0 bit[0]/Shift_Reg0 bit[0]
	633		LUT2_0 bit[1]/Shift_Reg0 bit[1]
	634		LUT2_0 bit[2]/Shift_Reg0 bit[2]
	635		LUT2_0 bit[3]/DFF0 /Shift_Reg0 bit[3]
	636	LUT2_1_DFF1_SHR1	LUT2_1 bit[0]/Shift_Reg1 bit[0]
	637		LUT2_1 bit[1]/Shift_Reg1 bit[1]
	638		LUT2_1 bit[2]/Shift_Reg1 bit[2]
	639		LUT2_1 bit[3]/DFF1 /Shift_Reg1 bit[3]
50	640	LUT2_2_ DFF2_SHR2	LUT2_2 bit[0]/Shift_Reg2 bit[0]
	641		LUT2_2 bit[1]/Shift_Reg2 bit[1]
	642		LUT2_2 bit[2]/Shift_Reg2 bit[2]
	643		LUT2_2 bit[3]/DFF2 /Shift_Reg2 bit[3]
	644	LUT2_3_PGEN0	LUT2_3 bit[0]/PGEN0 Size bit [0]
	645		LUT2_3 bit[1]/PGEN0 Size bit [1]
	646		LUT2_3 bit[2]/PGEN0 Size bit [2]
	647		LUT2_3 bit[3]/PGEN0 Size bit [3]
51	648	LUT3_0_DFF3_SHR3	LUT3_0 bit[0]/Shift_Reg3 bit[0]
	649		LUT3_0 bit[1]/Shift_Reg3 bit[1]
	650		LUT3_0 bit[2]/Shift_Reg3 bit[2]
	651		LUT3_0 bit[3]/Shift_Reg3 bit[3]
	652		LUT3_0 bit[4]/Shift_Reg3 bit[4]
	653		LUT3_0 bit[5]/Shift_Reg3 bit[5]
	654		LUT3_0 bit[6]/Shift_Reg3 bit[6]
	655		LUT3_0 bit[7]/DFF3/Shift_Reg3 bit[7]
52	656	LUT3_1_DFF4_SHR4	LUT3_1 bit[0]/Shift_Reg4 bit[0]
	657		LUT3_1 bit[1]/Shift_Reg4 bit[1]
	658		LUT3_1 bit[2]/Shift_Reg4 bit[2]
	659		LUT3_1 bit[3]/Shift_Reg4 bit[3]
	660		LUT3_1 bit[4]/Shift_Reg4 bit[4]
	661		LUT3_1 bit[5]/Shift_Reg4 bit[5]
	662		LUT3_1 bit[6]/Shift_Reg4 bit[6]
	663		LUT3_1 bit[7]/DFF4/Shift_Reg4 bit[7]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
53	664	LUT3_2_DFF5_SHR5	LUT3_2 bit[0]/Shift_Reg5 bit[0]
	665		LUT3_2 bit[1]/Shift_Reg5 bit[1]
	666		LUT3_2 bit[2]/Shift_Reg5 bit[2]
	667		LUT3_2 bit[3]/Shift_Reg5 bit[3]
	668		LUT3_2 bit[4]/Shift_Reg5 bit[4]
	669		LUT3_2 bit[5]/Shift_Reg5 bit[5]
	670		LUT3_2 bit[6]/Shift_Reg5 bit[6]
	671		LUT3_2 bit[7]/DFF5/Shift_Reg5 bit[7]
54	672	LUT3_3_DFF6_SHR6	LUT3_3 bit[0]/Shift_Reg6 bit[0]
	673		LUT3_3 bit[1]/Shift_Reg6 bit[1]
	674		LUT3_3 bit[2]/Shift_Reg6 bit[2]
	675		LUT3_3 bit[3]/Shift_Reg6 bit[3]
	676		LUT3_3 bit[4]/Shift_Reg6 bit[4]
	677		LUT3_3 bit[5]/Shift_Reg6 bit[5]
	678		LUT3_3 bit[6]/Shift_Reg6 bit[6]
	679		LUT3_3 bit[7]/DFF6/Shift_Reg6 bit[7]
55	680	LUT3_4_DFF7_SHR7	LUT3_4 bit[0]/Shift_Reg7 bit[0]
	681		LUT3_4 bit[1]/Shift_Reg7 bit[1]
	682		LUT3_4 bit[2]/Shift_Reg7 bit[2]
	683		LUT3_4 bit[3]/Shift_Reg7 bit[3]
	684		LUT3_4 bit[4]/Shift_Reg7 bit[4]
	685		LUT3_4 bit[5]/Shift_Reg7 bit[5]
	686		LUT3_4 bit[6]/Shift_Reg7 bit[6]
	687		LUT3_4 bit[7]/DFF7/Shift_Reg7 bit[7]
56	688	LUT3_5_DFF8_SHR8	LUT3_5 bit[0]/Shift_Reg8 bit[0]
	689		LUT3_5 bit[1]/Shift_Reg8 bit[1]
	690		LUT3_5 bit[2]/Shift_Reg8 bit[2]
	691		LUT3_5 bit[3]/Shift_Reg8 bit[3]
	692		LUT3_5 bit[4]/Shift_Reg8 bit[4]
	693		LUT3_5 bit[5]/Shift_Reg8 bit[5]
	694		LUT3_5 bit[6]/Shift_Reg8 bit[6]
	695		LUT3_5 bit[7]/DFF8/Shift_Reg8 bit[7]
57	696	LUT3_6_DFF9_SHR9	LUT3_6 bit[0]/Shift_Reg9 bit[0]
	697		LUT3_6 bit[1]/Shift_Reg9 bit[1]
	698		LUT3_6 bit[2]/Shift_Reg9 bit[2]
	699		LUT3_6 bit[3]/Shift_Reg9 bit[3]
	700		LUT3_6 bit[4]/Shift_Reg9 bit[4]
	701		LUT3_6 bit[5]/Shift_Reg9 bit[5]
	702		LUT3_6 bit[6]/Shift_Reg9 bit[6]
	703		LUT3_6 bit[7]/DFF9 /Shift_Reg9 bit[7]
58	704	LUT3_7_DFF10_SHR10	LUT3_7 bit[0]/Shift_Reg10 bit[0]
	705		LUT3_7 bit[1]/Shift_Reg10 bit[1]
	706		LUT3_7 bit[2]/Shift_Reg10 bit[2]
	707		LUT3_7 bit[3]/Shift_Reg10 bit[3]
	708		LUT3_7 bit[4]/Shift_Reg10 bit[4]
	709		LUT3_7 bit[5]/Shift_Reg10 bit[5]
	710		LUT3_7 bit[6]/Shift_Reg10 bit[6]
	711		LUT3_7 bit[7]/DFF10/Shift_Reg10 bit[7]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
59	712	LUT3_8_DFF11_SHR11	LUT3_8 bit[0]/Shift_Reg11 bit[0]
	713		LUT3_8 bit[1]/Shift_Reg11 bit[1]
	714		LUT3_8 bit[2]/Shift_Reg11 bit[2]
	715		LUT3_8 bit[3]/Shift_Reg11 bit[3]
	716		LUT3_8 bit[4]/Shift_Reg11 bit[4]
	717		LUT3_8 bit[5]/Shift_Reg11 bit[5]
	718		LUT3_8 bit[6]/Shift_Reg11 bit[6]
	719		LUT3_8 bit[7]/DFF11/Shift_Reg11 bit[7]
5A	720	LUT3_9_DFF12_SHR12	LUT3_9 bit[0]/Shift_Reg12 bit[0]
	721		LUT3_9 bit[1]/Shift_Reg12 bit[1]
	722		LUT3_9 bit[2]/Shift_Reg12 bit[2]
	723		LUT3_9 bit[3]/Shift_Reg12 bit[3]
	724		LUT3_9 bit[4]/Shift_Reg12 bit[4]
	725		LUT3_9 bit[5]/Shift_Reg12 bit[5]
	726		LUT3_9 bit[6]/Shift_Reg12 bit[6]
	727		LUT3_9 bit[7]/DFF12/Shift_Reg12 bit[7]
5B	728	LUT4_0_DFF13_SHR13	LUT4_0 bit[0]/Shift_Reg13 bit[0]
	729		LUT4_0 bit[1]/Shift_Reg13 bit[1]
	730		LUT4_0 bit[2]/Shift_Reg13 bit[2]
	731		LUT4_0 bit[3]/Shift_Reg13 bit[3]
	732		LUT4_0 bit[4]/Shift_Reg13 bit[4]
	733		LUT4_0 bit[5]/Shift_Reg13 bit[5]
	734		LUT4_0 bit[6]/Shift_Reg13 bit[6]
	735		LUT4_0 bit[7]/Shift_Reg13 bit[7]
5C	736		LUT4_0 bit[8]/Shift_Reg13 bit[8]
	737		LUT4_0 bit[9]/Shift_Reg13 bit[9]
	738		LUT4_0 bit[10]/Shift_Reg13 bit[10]
	739		LUT4_0 bit[11]/Shift_Reg13 bit[11]
	740		LUT4_0 bit[12]/Shift_Reg13 bit[12]
	741		LUT4_0 bit[13]/Shift_Reg13 bit[13]
	742		LUT4_0 bit[14]/Shift_Reg13 bit[14]
	743		LUT4_0 bit[15]/DFF13/Shift_Reg13 bit[15]
5D	744	LUT2_0_DFF0_SHR0 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	745	LUT2_0_DFF0_SHR0 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	746		
	747	LUT2_0_DFF0_SHR0 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	748	LUT2_0_DFF0_SHR0 Output Polarity Select	0: Non-inverted 1: Inverted
	749	LUT2_1_DFF1_SHR1 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	750	LUT2_1_DFF1_SHR1 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	751		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
5E	752	LUT2_1_DFF1_SHR1 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	753	LUT2_1_DFF1_SHR1 Output Polarity Select	0: Non-inverted 1: Inverted
	754	LUT2_2_DFF2_SHR2 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	755	LUT2_2_DFF2_SHR2 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	756		
	757	LUT2_2_DFF2_SHR2 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	758	LUT2_2_DFF2_SHR2 Output Polarity Select	0: Non-inverted 1: Inverted
	759	LUT2_3_PGEN0 Function Select	0: LUT 1: Pattern Generator
5F	760	LUT2_3_PGEN0 Active Level Selection for RST/SET	0: Active Low Level for reset/set 1: Active High Level for reset/set
	761	LUT3_0_DFF3_SHR3 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	762	LUT3_0_DFF3_SHR3 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	763		
	764		
	765	LUT3_0_DFF3_SHR3 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	766	LUT3_0_DFF3_SHR3 Output Polarity Select	0: Non-inverted 1: Inverted
	767	LUT3_0_DFF3_SHR3 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
60	768	LUT3_0_DFF3_SHR3 Set/Reset active level select	0: Active Low 1: Active High
	769	LUT3_1_DFF4_SHR4 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	770	LUT3_1_DFF4_SHR4 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	771		
	772		
	773	LUT3_1_DFF4_SHR4 DFF or Latch Select. Only valid when LUT_SEL=0 and SHR_LEN=0	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	774	LUT3_1_DFF4_SHR4 Output Polarity Select	0: Non-inverted 1: Inverted
	775	LUT3_1_DFF4_SHR4 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
61	776	LUT3_1_DFF4_SHR4 Set/Reset active level select	0: Active Low 1: Active High
	777	LUT3_2_DFF5_SHR5 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	778	LUT3_2_DFF5_SHR5 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	779		
	780		
	781	LUT3_2_DFF5_SHR5 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	782	LUT3_2_DFF5_SHR5 Output Polarity Select	0: Non-inverted 1: Inverted
	783	LUT3_2_DFF5_SHR5 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
62	784	LUT3_2_DFF5_SHR5 Set/Reset active level select	0: Active Low 1: Active High
	785	LUT3_3_DFF6_SHR6 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	786	LUT3_3_DFF6_SHR6 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	787		
	788		
	789	LUT3_3_DFF6_SHR6 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	790	LUT3_3_DFF6_SHR6 Output Polarity Select	0: Non-inverted 1: Inverted
	791	LUT3_3_DFF6_SHR6 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
63	792	LUT3_3_DFF6_SHR6 Set/Reset active level select	0: Active Low 1: Active High
	793	LUT3_4_DFF7_SHR7 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	794	LUT3_4_DFF7_SHR7 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	795		
	796		
	797	LUT3_4_DFF7_SHR7 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	798	LUT3_4_DFF7_SHR7 Output Polarity Select	0: Non-inverted 1: Inverted
	799	LUT3_4_DFF7_SHR7 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
64	800	LUT3_4_DFF7_SHR7 Set/Reset active level select	0: Active Low 1: Active High

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
64	801	LUT3_5_DFF8_SHR8 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	802	LUT3_5_DFF8_SHR8 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	803		
	804		
	805	LUT3_5_DFF8_SHR8 DFF or Latch Select.	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	806	LUT3_5_DFF8_SHR8 Output Polarity Select	0: Non-inverted 1: Inverted
	807	LUT3_5_DFF8_SHR8 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
65	808	LUT3_5_DFF8_SHR8 Set/Reset active level select	0: Active Low 1: Active High
	809	LUT3_6_DFF9_SHR9 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	810	LUT3_6_DFF9_SHR9 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	811		
	812		
	813	LUT3_6_DFF9_SHR9 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	814	LUT3_6_DFF9_SHR9 Output Polarity Select	0: Non-inverted 1: Inverted
	815	LUT3_6_DFF9_SHR9 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
66	816	LUT3_6_DFF9_SHR9 Set/Reset active level select	0: Active Low 1: Active High
	817	LUT3_7_DFF10_SHR10 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	818	LUT3_7_DFF10_SHR10 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	819		
	820		
	821	LUT3_7_DFF10_SHR10 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	822	LUT3_7_DFF10_SHR10 Output Polarity Select	0: Non-inverted 1: Inverted
	823	LUT3_7_DFF10_SHR10 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
67	824	LUT3_7_DFF10_SHR10 Set/Reset active level select	0: Active Low 1: Active High
	825	LUT3_8_DFF11_SHR11 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
67	826	LUT3_8_DFF11_SHR11 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	827		
	828		
	829	LUT3_8_DFF11_SHR11 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	830	LUT3_8_DFF11_SHR11 Output Polarity Select	0: Non-inverted 1: Inverted
	831	LUT3_8_DFF11_SHR11 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
68	832	LUT3_8_DFF11_SHR11 Set/Reset active level select	0: Active Low 1: Active High
	833	LUT3_9_DFF12_SHR12 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	834	LUT3_9_DFF12_SHR12 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	835		
	836		
	837	LUT3_9_DFF12_SHR12 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	838	LUT3_9_DFF12_SHR12 Output Polarity Select	0: Non-inverted 1: Inverted
	839	LUT3_9_DFF12_SHR12 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
69	840	LUT3_9_DFF12_SHR12 Set/Reset active level select	0: Active Low 1: Active High
	841	LUT4_0_DFF13_SHR13 DFF/Latch/Shift or LUT Select	0: LUT 1: DFF/Latch/Shift Register
	842	LUT4_0_DFF13_SHR13 Shift Register Length	Value=0 DFF/Latch Mode, Value=1 Length=2, Value=2 Length=3, Value=3 Length=4...
	843		
	844		
	845		
	846	LUT4_0_DFF13_SHR13 DFF or Latch Select	0: DFF 1: Latch (Only valid when LUT_SEL=0 and SHR_LEN=0)
	847	LUT4_0_DFF13_SHR13 Output Polarity Select	0: Non-inverted 1: Inverted
6A	848	LUT4_0_DFF13_SHR13 nRST/nSet Select	0: DFF/SHR use nRST 1: DFF/SHR use nSET (Only valid in DFF/Latch mode)
	849	LUT4_0_DFF13_SHR13 Set/Reset active level select	0: Active Low 1: Active High
	850	Reserved	
	851	Reserved	
	852	Reserved	
	853	Reserved	
6A	854	Reserved	
	855	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
6B	856	LUT2_3_PGEN0_DATA_LSB[7:0]	Pattern Data LSB
	857		
	858		
	859		
	860		
	861		
	862		
	863		
6C	864	LUT2_3_PGEN0_DATA_MSB[7:0]	Pattern Data MSB
	865		
	866		
	867		
	868		
	869		
	870		
	871		
6D	872	LUT4_1_DFF14_CNTDLY0	MLT0_LUT4_1 bit[0]/DFF14 DFF or Latch Select: 0: LUT: LUT[0]; DFF: DFF function 1: LUT: LUT[0]; DFF: Latch function
	873		MLT0_LUT4_1 bit[1]/DFF14 Output Select: 0: LUT: LUT[1]; DFF: Q output 1: LUT: LUT[1]; DFF: QB output
	874		MLT0_LUT4_1 bit[2]/DFF14 Initial Polarity Select: 0: LUT: LUT[2]; DFF: Low 1: LUT: LUT[2]; DFF: High
	875		MLT0_LUT4_1 bit[3]
	876		MLT0_LUT4_1 bit[4]
	877		MLT0_LUT4_1 bit[5]
	878		MLT0_LUT4_1 bit[6]
	879		MLT0_LUT4_1 bit[7]
6E	880		MLT0_LUT4_1 bit[8]
	881		MLT0_LUT4_1 bit[9]
	882		MLT0_LUT4_1 bit[10]
	883		MLT0_LUT4_1 bit[11]
	884		MLT0_LUT4_1 bit[12]
	885		MLT0_LUT4_1 bit[13]
	886		MLT0_LUT4_1 bit[14]
	887		MLT0_LUT4_1 bit[15]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
6F	888	CNTDLY0 Function and Edge mode selection	0000: Both edge Delay 0001: Falling edge Delay 0010: Rising edge Delay 0011: Prohibited 0100: Both edge One Shot 0101: Falling edge One Shot 0110: Rising edge One Shot 0111: Prohibited 1000: Both edge frequency detect 1001: Falling edge frequency detect 1010: Rising edge frequency detect 1011: Prohibited 1100: Both edge reset CNT 1101: Falling edge reset CNT 1110: Rising edge reset CNT 1111: High level reset CNT
	889		
	890		
	891		
	892	MLT0_LUT4_1_DFF14 LUT/DFF Function Select	0: LUT 1: DFF/Latch
	893	CNT0 CNT/DLY output Polarity selection	0: Default Output 1: Inverted Output
	894	CNT0 DLY mode edge detection selection	0: Normal 1: Enable DLY mode edge detection
	895	CNT0 CNT mode synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
70	896	LUT4_1_DFF14_CNTDLY0 Multi function selection	00: Single LUT or DFF (DLY input is low) 01: Single CNT/DLY (DLY output connect to LUT/DFF) 10: CNT/DLY connected to LUT or DFF 11: LUT or DFF connected to CNT/DLY
	897		
	898	MLT0_LUT4_1_DFF14_CNTDLY0 CNT/DLY and LUT or DFF connection (only works when multi_func_sel_reg is 2'b10)	00: DLY input from matrix A; DLY output connected to LUT's In3 or DFF's D 01: DLY input from matrix B; DLY output connected to LUT's In2 or DFF's nSET 10: DLY input from matrix C; DLY output connected to LUT's In1 or DFF's nRST 11: DLY input from matrix D; DLY output connected to LUT's In0 or DFF's CLK
	899		
	900	CNT0 CNT/DLY initial value selection	00: Bypass the initial 01: Bypass the initial 10: Initial 0 11: Initial 1
	901		
	902	CNT0 CNT external clock selection (only works when multi_func_sel_reg is not 2'b00)	00: Connected to LOW 01: Form matrix B 10: From matrix C 11: Connected to LOW
	903		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
71	904	CNT0 CNT/DLY clock source selection	0000: RingOSC(25 MHz) 0001: RingOSC(25 MHz)/4 0010: RingOSC(25 MHz)/8 0011: RingOSC(25 MHz)/64 0100: RingOSC(25 MHz)/512 0101: LFOSC(2 kHz) 0110: LFOSC(2 kHz)/8 0111: LFOSC(2 kHz)/64 1000: LFOSC(2KkHz)/512 1001: LFOSC(2 kHz)/4096 1010: LFOSC(2 kHz)/32768 1011: LFOSC(2 kHz)/262144 1100: CNTx_END 1101: External 1110: Not used 1111: Not used
	905		
	906		
	907		
	908	Reserved	
	909	Reserved	
	910	Reserved	
	911	Reserved	
72	912	CNT0 MSB of CNT Data	Data [15:8]
	913		
	914		
	915		
	916		
	917		
	918		
	919		
73	920	CNT0 LSB of CNT Data	Data [7:0]
	921		
	922		
	923		
	924		
	925		
	926		
	927		
74	928	CNT0 MSB of Current CNT Value	Data [15:8]
	929		
	930		
	931		
	932		
	933		
	934		
	935		
75	936	CNT0 LSB of Current CNT Value	Data [7:0]
	937		
	938		
	939		
	940		
	941		
	942		
	943		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
76	944	CNT0 CNT set or rest selection	0: Reset to 0 1: Set to data
	945	CNT0 CNT up signal synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
	946	CNT0 CNT keep signal synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
	947	CNT0 Wake sleep power-down state selection	0: Low 1: High
	948	CNT0 CNT wake sleep mode selection	0: Default mode 1: Wake-up sleep mode (func_sel_reg configure as CNT mode)
	949	CNT0 ACMP Wake/Sleep time selection	0: Normal 1: Short Time
	950	CNT0 Allow short wake-up signal	0: Disable 1: Enable
	951	Reserved	
77	952	ACMP0 wake sleep enable	0: Disable 1: Enable
	953	ACMP1 wake sleep enable	0: Disable 1: Enable
	954	Reserved	
	955	Reserved	
	956	Reserved	
	957	Reserved	
	958	Reserved	
	959	Reserved	
78	960	LUT3_10_DFF15_CNTDLY1	MLT1_LUT3_10 bit[0]/DFF15 DFF or Latch Select: 0: LUT: LUT[0]; DFF: DFF function 1: LUT: LUT[0]; DFF: Latch function
	961		MLT1_LUT3_10 bit[1]/DFF15 Output Select: 0: LUT: LUT[1]; DFF: Q output 1: LUT: LUT[1]; DFF: QB output
	962		MLT1_LUT3_10 bit[2]/DFF15 Initial Polarity Select: 0: LUT: LUT[2]; DFF: Low 1: LUT: LUT[2]; DFF: High
	963		MLT1_LUT3_10 bit[3]/DFF15 nRST or nSET Select: 0: LUT: LUT[3]; DFF: nRST 1: LUT: LUT[3]; DFF: nSET
	964		MLT1_LUT3_10 bit[4]
	965		MLT1_LUT3_10 bit[5]
	966		MLT1_LUT3_10 bit[6]
	967		MLT1_LUT3_10 bit[7]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
79	968	CNTDLY1 Function and Edge mode selection	0000: both edge Delay 0001: falling edge Delay 0010: rising edge Delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	969		
	970		
	971		
	972	MLT1_LUT3_10_DFF15 LUT/DFF Function Select	0: LUT 1: DFF/Latch
	973	CNT1 CNT/DLY output Polarity selection	0: Default Output 1: Inverted Output
	974	CNT1 DLY mode edge detection selection	0: Normal 1: Enable DLY mode edge detection
	975	CNT1 CNT mode synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
7A	976	LUT3_10_DFF15_CNTDLY1 Multi function selection	00: Single LUT or DFF (DLY input is low) 01: Single CNT/DLY (DLY output connect to LUT/DFF) 10: CNT/DLY connected to LUT or DFF 11: LUT or DFF connected to CNT/DLY
	977		
	978	MLT1_LUT3_10_DFF15_CNTDLY1 CNT/DLY and LUT or DFF connection (only works when multi_func_sel_reg is 2'b10)	00: DLY input from matrix A; DLY output connected to LUT's In2 or DFF's D 01: DLY input from matrix B; DLY output connected to LUT's In1 or DFF's nSET/nRST 10: DLY input from matrix C; DLY output connected to LUT's In0 or DFF's CLK 11: Prohibited
	979		
	980	CNT1 CNT/DLY initial value selection	00: Bypass the initial 01: Bypass the initial 10: Initial 0 11: Initial 1
	981		
	982	Reserved	
	983	Reserved	
7B	984	CNT1 CNT/DLY clock source selection	0000: RingOSC(25 MHz) 0001: RingOSC(25 MHz)/4 0010: RingOSC(25 MHz)/8 0011: RingOSC(25 MHz)/64 0100: RingOSC(25 MHz)/512 0101: LFOSC(2 kHz) 0110: LFOSC(2 kHz)/8 0111: LFOSC(2 kHz)/64 1000: LFOSC(2 kHz)/512 1001: LFOSC(2 kHz)/4096 1010: LFOSC(2 kHz)/32768 1011:LFOSC(2 kHz)/262144 1100: CNTx_END 1101: External 1110: Not used 1111: Not used
	985		
	986		
	987		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
7B	988	Reserved	
	989	Reserved	
	990	Reserved	
	991	Reserved	
7C	992	CNT1 CNT Data	Data [7:0]
	993		
	994		
	995		
	996		
	997		
	998		
	999		
7D	1000	CNT1 Current CNT Value	Data [7:0]
	1001		
	1002		
	1003		
	1004		
	1005		
	1006		
	1007		
7E	1008	LUT3_11_DFF16_CNTDLY2	MLT2_LUT3_11 bit[0]/DFF16 DFF or Latch Select: 0: LUT: LUT[0]; DFF: DFF function 1: LUT: LUT[0]; DFF: Latch function
	1009		MLT2_LUT3_11 bit[1]/DFF16 Output Select: 0: LUT: LUT[1]; DFF: Q output 1: LUT: LUT[1]; DFF: QB output
	1010		MLT2_LUT3_11 bit[2]/DFF16 Initial Polarity Select: 0: LUT: LUT[2]; DFF: Low 1: LUT: LUT[2]; DFF: High
	1011		MLT2_LUT3_11 bit[3]/DFF16 nRST or nSET Select: 0: LUT: LUT[3]; DFF: nRST 1: LUT: LUT[3]; DFF: nSET
	1012		MLT2_LUT3_11 bit[4]
	1013		MLT2_LUT3_11 bit[5]
	1014		MLT2_LUT3_11 bit[6]
	1015		MLT2_LUT3_11 bit[7]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
7F	1016	CNTDLY2 Function and Edge mode selection	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1017		
	1018		
	1019		
	1020	MLT2_LUT3_11_DFF16 LUT/DFF Function Select	0: LUT 1: DFF/Latch
	1021	CNT2 CNT/DLY output Polarity selection	0: Default Output 1: Inverted Output
	1022	CNT2 DLY mode edge detection selection	0: Normal 1: Enable DLY mode edge detection
	1023	CNT2 CNT mode synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
80	1024	LUT3_11_DFF16_CNTDLY2 Multi function selection	00: Single LUT or DFF (DLY input is low) 01: Single CNT/DLY (DLY output connect to LUT/DFF) 10: CNT/DLY connected to LUT or DFF 11: LUT or DFF connected to CNT/DLY
	1025		
	1026	MLT2_LUT3_11_DFF16_CNTDLY2 CNT/DLY and LUT or DFF connection (only works when multi_func_sel_reg is 2'b10)	00: DLY input from matrix A; DLY output connected to LUT's In2 or DFF's D 01: DLY input from matrix B; DLY output connected to LUT's In1 or DFF's nSET/nRST 10: DLY input from matrix C; DLY output connected to LUT's In0 or DFF's CLK 11: Prohibited
	1027		
	1027	CNT2 CNT/DLY initial value selection	00: Bypass the initial 01: Bypass the initial 10: Initial 0 11: Initial 1
	1029		
	1030	Reserved	
	1031	Reserved	
81	1032	Matrix Divider Ratio Control	0000: RingOSC(25 MHz) 0001: RingOSC(25 MHz)/4 0010: RingOSC(25 MHz)/8 0011: RingOSC(25 MHz)/64 0100: RingOSC(25MHz)/512 0101: LFOSC(2 kHz) 0110: LFOSC(2 kHz)/8 0111: LFOSC(2 kHz)/64 1000: LFOSC(2 kHz)/512 1001: LFOSC(2 kHz)/4096 1010: LFOSC(2 kHz)/32768 1011: LFOSC(2 kHz)/262144 1100: CNTx_END 1101: External 1110: Not used 1111: Not used
	1033		
	1034		
	1035		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
81	1036	Reserved	
	1037	Reserved	
	1038	Reserved	
	1039	Reserved	
82	1040	CNT2 CNT Data	Data [7:0]
	1041		
	1042		
	1043		
	1044		
	1045		
	1046		
	1047		
83	1048	CNT2 Current CNT Value	Data [7:0]
	1049		
	1050		
	1051		
	1052		
	1053		
	1054		
	1055		
84	1056	LUT3_12_DFF17_CNTDLY3	MLT3_LUT3_12 bit[0]/DFF17 DFF or Latch Select: 0: LUT: LUT[0]; DFF: DFF function 1: LUT: LUT[0]; DFF: Latch function
	1057		MLT3_LUT3_12 bit[1]/DFF17 Output Select: 0: LUT: LUT[1]; DFF: Q output 1: LUT: LUT[1]; DFF: QB output
	1058		MLT3_LUT3_12 bit[2]/DFF17 Initial Polarity Select: 0: LUT: LUT[2]; DFF: Low 1: LUT: LUT[2]; DFF: High
	1059		MLT3_LUT3_12 bit[3]/DFF17 nRST or nSET Select: 0: LUT: LUT[3]; DFF: nRST 1: LUT: LUT[3]; DFF: nSET
	1060		MLT3_LUT3_12 bit[4]
	1061		MLT3_LUT3_12 bit[5]
	1062		MLT3_LUT3_12 bit[6]
	1063		MLT3_LUT3_12 bit[7]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
85	1064	CNTDLY3 Function and Edge mode selection	0000: both edge Delay 0001: falling edge Delay 0010: rising edge Delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1065		
	1066		
	1067		
	1068	MLT3_LUT3_12_DFF17 LUT/DFF Function Select	0: LUT 1: DFF/Latch
	1069	CNT3 CNT/DLY output Polarity selection	0: Default Output 1: Inverted Output
	1070	CNT3 DLY mode edge detection selection	0: Normal 1: Enable DLY mode edge detection
	1071	CNT3 CNT mode synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
86	1072	LUT3_12_DFF17_CNTDLY3 Multi function selection	00: Single LUT or DFF (DLY input is low) 01: Single CNT/DLY (DLY output connect to LUT/DFF) 10: CNT/DLY connected to LUT or DFF 11: LUT or DFF connected to CNT/DLY
	1073		
	1074	MLT3_LUT3_12_DFF17_CNTDLY3 CNT/DLY and LUT or DFF connection (only works when multi_func_sel_reg is 2'b10)	00: DLY input from matrix A; DLY output connected to LUT's In2 or DFF's D 01: DLY input from matrix B; DLY output connected to LUT's In1 or DFF's nSET/nRST 10: DLY input from matrix C; DLY output connected to LUT's In0 or DFF's CLK 11: Prohibited
	1075		
	1076	CNT3 CNT/DLY initial value selection	00: Bypass the initial 01: Bypass the initial 10: Initial 0 11: Initial 1
	1077		
	1078	Reserved	
	1079	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
87	1080	CNT3 CNT/DLY clock source selection	0000: RingOSC(25 MHz) 0001: RingOSC(25 MHz)/4 0010: RingOSC(25 MHz)/8 0011:RingOSC(25 MHz)/64 0100: RingOSC(25 MHz)/512 0101: LFOSC(2 kHz) 0110: LFOSC(2 kHz)/8 0111: LFOSC(2 kHz)/64 1000:LFOSC(2 kHz)/512 1001: LFOSC(2 kHz)/4096 1010: LFOSC(2 kHz)/32768 1011:LFOSC(2 kHz)/262144 1100: CNTx_END 1101: External 1110: Not used 1111: Not used
	1081		
	1082		
	1083		
	1084	Reserved	
	1085	Reserved	
	1086	Reserved	
	1087	Reserved	
88	1088	CNT3 CNT Data	Data [7:0]
	1089		
	1090		
	1091		
	1092		
	1093		
	1094		
	1095		
89	1096	CNT3 Current CNT Value	Data [7:0]
	1097		
	1098		
	1099		
	1100		
	1101		
	1102		
	1103		
8A	1104	LUT3_13_DFF18_CNTDLY4	MLT4_LUT3_13 bit[0]/DFF18 DFF or Latch Select: 0: LUT: LUT[0]; DFF: DFF function 1: LUT: LUT[0]; DFF: Latch function
	1105		MLT4_LUT3_13 bit[1]/DFF18 Output Select: 0: LUT: LUT[1]; DFF: Q output 1: LUT: LUT[1]; DFF: QB output
	1106		MLT4_LUT3_13 bit[2]/DFF18 Initial Polarity Select: 0: LUT: LUT[2]; DFF: Low 1: LUT: LUT[2]; DFF: High
	1107		MLT4_LUT3_13 bit[3]/DFF18 nRST or nSET Select: 0: LUT: LUT[3]; DFF: nRST 1: LUT: LUT[3]; DFF: nSET
	1108		MLT4_LUT3_13 bit[4]
	1109		MLT4_LUT3_13 bit[5]
	1110		MLT4_LUT3_13 bit[6]
8A	1111	LUT3_13_DFF18_CNTDLY4	MLT4_LUT3_13 bit[7]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
8B	1112	CNTDLY4 Function and Edge mode selection	0000: both edge Delay 0001: falling edge Delay 0010: rising edge Delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1113		
	1114		
	1115		
	1116	MLT4_LUT3_13_DFF18 LUT/DFF Function Select	0: LUT 1: DFF/Latch
	1117	CNT4 CNT/DLY output Polarity selection	0: Default Output 1: Inverted Output
	1118	CNT4 DLY mode edge detection selection	0: Normal 1: Enable DLY mode edge detection
	1119	CNT4 CNT mode synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
8C	1120	LUT3_13_DFF18_CNTDLY4 Multi function selection	00: Single LUT or DFF (DLY input is low) 01: Single CNT/DLY (DLY output connect to LUT/DFF) 10: CNT/DLY connected to LUT or DFF 11: LUT or DFF connected to CNT/DLY
	1121		
	1122	MLT4_LUT3_13_DFF18_CNTDLY4 CNT/DLY and LUT or DFF connection (only works when multi_func_sel_reg is 2'b10)	00: DLY input from matrix A; DLY output connected to LUT's In2 or DFF's D 01: DLY input from matrix B; DLY output connected to LUT's In1 or DFF's nSET/nRST 10: DLY input from matrix C; DLY output connected to LUT's In0 or DFF's CLK 11: Prohibited
	1123		
	1124	CNT4 CNT/DLY initial value selection	00: Bypass the initial 01: Bypass the initial 10: Initial 0 11: Initial 1
	1125		
	1126	Reserved	
	1127	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
8D	1128	CNT4 CNT/DLY clock source selection	0000: RingOSC(25 MHz) 0001: RingOSC(25 MHz)/4 0010: RingOSC(25 MHz)/8 0011:RingOSC(25 MHz)/64 0100: RingOSC(25 MHz)/512 0101: LFOSC(2 kHz) 0110: LFOSC(2 kHz)/8 0111: LFOSC(2 kHz)/64 1000:LFOSC(2 kHz)/512 1001: LFOSC(2 kHz)/4096 1010: LFOSC(2 kHz)/32768 1011:LFOSC(2 kHz)/262144 1100: CNTx_END 1101: External 1110: Not used 1111: Not used
	1129		
	1130		
	1131		
	1132	Reserved	
	1133	Reserved	
	1134	Reserved	
	1135	Reserved	
8E	1136	CNT4 CNT Data	Data [7:0]
	1137		
	1138		
	1139		
	1140		
	1141		
	1142		
	1143		
8F	1144	CNT4 Current CNT Value	Data [7:0]
	1145		
	1146		
	1147		
	1148		
	1149		
	1150		
	1151		
90	1152	LUT3_14_DFF19_CNTDLY5	MLT5_LUT3_14 bit[0]/DFF19 DFF or Latch Select: 0: LUT: LUT[0]; DFF: DFF function 1: LUT: LUT[0]; DFF: Latch function
	1153		MLT5_LUT3_14 bit[1]/DFF19 Output Select: 0: LUT: LUT[1]; DFF: Q output 1: LUT: LUT[1]; DFF: QB output
	1154		MLT5_LUT3_14 bit[2]/DFF19 Initial Polarity Select: 0: LUT: LUT[2]; DFF: Low 1: LUT: LUT[2]; DFF: High
	1155		MLT5_LUT3_14 bit[3]/DFF19 nRST or nSET Select: 0: LUT: LUT[3]; DFF: nRST 1: LUT: LUT[3]; DFF: nSET
	1156		MLT5_LUT3_14 bit[4]
	1157		MLT5_LUT3_14 bit[5]
	1158		MLT5_LUT3_14 bit[6]
90	1159	LUT3_14_DFF19_CNTDLY5	MLT5_LUT3_14 bit[7]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
91	1160	CNTDLY5 Function and Edge mode selection	0000: both edge Delay 0001: falling edge Delay 0010: rising edge Delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1161		
	1162		
	1163		
	1164	MLT5_LUT3_14_DFF19 LUT/DFF Function Select	0: LUT 1: DFF/Latch
	1165	CNT5 CNT/DLY output Polarity selection	0: Default Output 1: Inverted Output
	1166	CNT5 DLY mode edge detection selection	0: Normal 1: Enable DLY mode edge detection
	1167	CNT5 CNT mode synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
92	1168	LUT3_14_DFF19_CNTDLY5 Multi function selection	00: Single LUT or DFF (DLY input is low) 01: Single CNT/DLY (DLY output connect to LUT/DFF) 10: CNT/DLY connected to LUT or DFF 11: LUT or DFF connected to CNT/DLY
	1169		
	1170	MLT5_LUT3_14_DFF19_CNTDLY5 CNT/DLY and LUT or DFF connection (only works when multi_func_sel_reg is 2'b10)	00: DLY input from matrix A; DLY output connected to LUT's In2 or DFF's D 01: DLY input from matrix B; DLY output connected to LUT's In1 or DFF's nSET/nRST 10: DLY input from matrix C; DLY output connected to LUT's In0 or DFF's CLK 11: Prohibited
	1171		
	1172	CNT5 CNT/DLY initial value selection	00: Bypass the initial 01: Bypass the initial 10: Initial 0 11: Initial 1
	1173		
	1174	Reserved	
	1175	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
93	1176	CNT5 CNT/DLY clock source selection	0000: RingOSC(25 MHz) 0001: RingOSC(25 MHz)/4 0010: RingOSC(25 MHz)/8 0011:RingOSC(25 MHz)/64 0100: RingOSC(25 MHz)/512 0101: LFOSC(2 kHz) 0110: LFOSC(2 kHz)/8 0111: LFOSC(2 kHz)/64 1000:LFOSC(2 kHz)/512 1001: LFOSC(2 kHz)/4096 1010: LFOSC(2 kHz)/32768 1011:LFOSC(2 kHz)/262144 1100: CNTx_END 1101: External 1110: Not used 1111: Not used
	1177		
	1178		
	1179		
	1180	Reserved	
	1181	Reserved	
	1182	Reserved	
	1183	Reserved	
94	1184	CNT5 CNT Data	Data [7:0]
	1185		
	1186		
	1187		
	1188		
	1189		
	1190		
	1191		
95	1192	CNT5 Current CNT Value	Data [7:0]
	1193		
	1194		
	1195		
	1196		
	1197		
	1198		
	1199		
96	1200	LUT3_15_DFF20_CNTDLY6	MLT6_LUT3_15 bit[0]/DFF20 DFF or Latch Select: 0: LUT: LUT[0]; DFF: DFF function 1: LUT: LUT[0]; DFF: Latch function
	1201		MLT6_LUT3_15 bit[1]/DFF20 Output Select: 0: LUT: LUT[1]; DFF: Q output 1: LUT: LUT[1]; DFF: QB output
	1202		MLT6_LUT3_15 bit[2]/DFF20 Initial Polarity Select: 0: LUT: LUT[2]; DFF: Low 1: LUT: LUT[2]; DFF: High
	1203		MLT6_LUT3_15 bit[3]/DFF20 nRST or nSET Select: 0: LUT: LUT[3]; DFF: nRST 1: LUT: LUT[3]; DFF: nSET
	1204		MLT6_LUT3_15 bit[4]
	1205		MLT6_LUT3_15 bit[5]
	1206		MLT6_LUT3_15 bit[6]
96	1207	LUT3_15_DFF20_CNTDLY6	MLT6_LUT3_15 bit[7]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
97	1208	CNTDLY6 Function and Edge mode selection	0000: both edge Delay 0001: falling edge Delay 0010: rising edge Delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1209		
	1210		
	1211		
	1212	MLT6_LUT3_15_DFF20 LUT/DFF Function Select	0: LUT 1: DFF/Latch
	1213	CNT6 CNT/DLY output Polarity selection	0: Default Output 1: Inverted Output
	1214	CNT6 DLY mode edge detection selection	0: Normal 1: Enable DLY mode edge detection
	1215	CNT6 CNT mode synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
98	1216	LUT3_15_DFF20_CNTDLY6 Multi function selection	00: Single LUT or DFF (DLY input is low) 01: Single CNT/DLY (DLY output connect to LUT/DFF) 10: CNT/DLY connected to LUT or DFF 11: LUT or DFF connected to CNT/DLY
	1217		
	1218	MLT6_LUT3_15_DFF20_CNTDLY6 CNT/DLY and LUT or DFF connection (only works when multi_func_sel_reg is 2'b10)	00: DLY input from matrix A; DLY output connected to LUT's In2 or DFF's D 01: DLY input from matrix B; DLY output connected to LUT's In1 or DFF's nSET/nRST 10: DLY input from matrix C; DLY output connected to LUT's In0 or DFF's CLK 11: Prohibited
	1219		
	1220	CNT6 CNT/DLY initial value selection	00: Bypass the initial 01: Bypass the initial 10: Initial 0 11: Initial 1
	1221		
	1222	Reserved	
	1223	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
99	1224	CNT6 CNT/DLY clock source selection	0000: RingOSC(25 MHz) 0001: RingOSC(25 MHz)/4 0010: RingOSC(25 MHz)/8 0011:RingOSC(25 MHz)/64 0100: RingOSC(25 MHz)/512 0101: LFOSC(2 kHz) 0110: LFOSC(2 kHz)/8 0111: LFOSC(2 kHz)/64 1000:LFOSC(2 kHz)/512 1001: LFOSC(2 kHz)/4096 1010: LFOSC(2 kHz)/32768 1011:LFOSC(2 kHz)/262144 1100: CNTx_END 1101: External 1110: Not used 1111: Not used
	1225		
	1226		
	1227		
	1228	Reserved	
	1229	Reserved	
	1230	Reserved	
	1231	Reserved	
9A	1232	CNT6 CNT Data	Data [7:0]
	1233		
	1234		
	1235		
	1236		
	1237		
	1238		
	1239		
9B	1240	CNT6 Current CNT Value	Data [7:0]
	1241		
	1242		
	1243		
	1244		
	1245		
	1246		
	1247		
9C	1248	LUT3_16_DFF21_CNTDLY7	MLT7_LUT3_16 bit[0]/DFF21 DFF or Latch Select: 0: LUT: LUT[0]; DFF: DFF function 1: LUT: LUT[0]; DFF: Latch function
	1249		MLT7_LUT3_16 bit[1]/DFF21 Output Select: 0: LUT: LUT[1]; DFF: Q output 1: LUT: LUT[1]; DFF: QB output
	1250		MLT7_LUT3_16 bit[2]/DFF21 Initial Polarity Select: 0: LUT: LUT[2]; DFF: Low 1: LUT: LUT[2]; DFF: High
	1251		MLT7_LUT3_16 bit[3]/DFF21 nRST or nSET Select: 0: LUT: LUT[3]; DFF: nRST 1: LUT: LUT[3]; DFF: nSET
	1252		MLT7_LUT3_16 bit[4]
	1253		MLT7_LUT3_16 bit[5]
	1254		MLT7_LUT3_16 bit[6]
9C	1255	LUT3_16_DFF21_CNTDLY7	MLT7_LUT3_16 bit[7]

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
9D	1256	CNTDLY7 Function and Edge mode selection	0000: both edge Delay 0001: falling edge Delay 0010: rising edge Delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1257		
	1258		
	1259		
	1260	MLT7_LUT3_16_DFF21 LUT/DFF Function Select	0: LUT 1: DFF/Latch
	1261	CNT7 CNT/DLY output Polarity selection	0: Default Output 1: Inverted Output
	1262	CNT7 DLY mode edge detection selection	0: Normal 1: Enable DLY mode edge detection
	1263	CNT7 CNT mode synchronizer selection	0: Bypass synchronizer 1: Enable synchronizer (after two DFFs)
9E	1264	LUT3_16_DFF21_CNTDLY7 Multi function selection	00: Single LUT or DFF (DLY input is low) 01: Single CNT/DLY (DLY output connect to LUT/DFF) 10: CNT/DLY connected to LUT or DFF 11: LUT or DFF connected to CNT/DLY
	1265		
	1266	MLT7_LUT3_16_DFF21_CNTDLY7 CNT/DLY and LUT or DFF connection (only works when multi_func_sel_reg is 2'b10)	00: DLY input from matrix A; DLY output connected to LUT's In2 or DFF's D 01: DLY input from matrix B; DLY output connected to LUT's In1 or DFF's nSET/nRST 10: DLY input from matrix C; DLY output connected to LUT's In0 or DFF's CLK 11: Prohibited
	1267		
	1268	CNT7 CNT/DLY initial value selection	00: Bypass the initial 01: Bypass the initial 10: Initial 0 11: Initial 1
	1269		
	1270	Reserved	
	1271	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
9F	1272	CNT7 CNT/DLY clock source selection	0000: RingOSC(25 MHz) 0001: RingOSC(25 MHz)/4 0010: RingOSC(25 MHz)/8 0011:RingOSC(25 MHz)/64 0100: RingOSC(25 MHz)/512 0101: LFOSC(2 kHz) 0110: LFOSC(2 kHz)/8 0111: LFOSC(2kHz)/64 1000:LFOSC(2 kHz)/512 1001: LFOSC(2 kHz)/4096 1010: LFOSC(2 kHz)/32768 1011:LFOSC(2 kHz)/262144 1100: CNTx_END 1101: External 1110: Not used 1111: Not used
	1273		
	1274		
	1275		
	1276	Reserved	
	1277	Reserved	
	1278	Reserved	
	1279	Reserved	
A0	1280	CNT7 CNT Data	Data [7:0]
	1281		
	1282		
	1283		
	1284		
	1285		
	1286		
	1287		
A1	1288	CNT7 Current CNT Value	Data [7:0]
	1289		
	1290		
	1291		
	1292		
	1293		
	1294		
	1295		
A2	1296	GPI0 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1297		
	1298	Reserved	
	1299	Reserved	
	1300	Reserved	
	1301	Reserved	
	1302		
	1303	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
A3	1304	GPIO0 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1305		
	1306	Reserved	
	1307	Reserved	
	1308	Reserved	
	1309	GPIO0 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1310		
	1311	GPIO0 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
A4	1312	GPIO0 I^2C fast mode plus enable	0: enable 1: disable
	1313	GPIO0 Open-Drain mode enable	0: disable (Output = HiZ) 1: enable (Applicable only when i2c_en = 0)
	1314	Reserved	
	1315	Reserved	
	1316	Reserved	
	1317	Reserved	
	1318	Reserved	
	1319	Reserved	
A5	1320	GPIO1 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1321		
	1322	Reserved	
	1323	Reserved	
	1324	Reserved	
	1325	GPIO1 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1326		
	1327	GPIO1 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
A6	1328	GPIO1 I^2C fast mode plus enable	0: enable 1: disable
	1329	GPIO1 Open-Drain mode enable	0: disable (Output = HiZ) 1: enable (Applicable only when i2c_en = 0)
	1330	Reserved	
	1331	Reserved	
	1332	Reserved	
	1333	Reserved	
	1334	Reserved	
	1335	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
A7	1336	GPIO2 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1337		
	1338	GPIO2 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1339		
	1340	Reserved	
	1341	GPIO2 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1342		
	1343	GPIO2 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
A8	1344	GPIO3 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1345		
	1346	GPIO3 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1347		
	1348	Reserved	
	1349	GPIO3 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1350		
	1351	GPIO3 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
A9	1352	GPIO4 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1353		
	1354	GPIO4 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1355		
	1356	Reserved	
	1357	GPIO4 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1358		
	1359	GPIO4 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
AA	1360	GPIO5 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1361		
	1362	GPIO5 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1363		
	1364	Reserved	
	1365	GPIO5 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1366		
	1367	GPIO5 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
AB	1368	GPIO6 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1369		
	1370	GPIO6 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1371		
	1372	Reserved	
	1373	GPIO6 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1374		
	1375	GPIO6 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
AC	1376	GPIO7 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1377		
	1378	GPIO7 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1379		
	1380	Reserved	
	1381	GPIO7 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1382		
	1383	GPIO7 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
AD	1384	GPIO8 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1385		
	1386	GPIO8 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1387		
	1388	Reserved	
	1389	GPIO8 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1390		
	1391	GPIO8 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
AE	1392	GPIO9 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1393		
	1394	GPIO9 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1395		
	1396	Reserved	
	1397	GPIO9 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1398		
	1399	GPIO9 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
AF	1400	GPIO10 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1401		
	1402	GPIO10 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1403		
	1404	Reserved	
	1405	GPIO10 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1406		
	1407	GPIO10 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
B0	1408	GPIO11 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1409		
	1410	GPIO11 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1411		
	1412	Reserved	
	1413	GPIO11 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1414		
	1415	GPIO11 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
B1	1416	GPIO12 input mode configuration	00: Digital in without Schmitt Trigger 01: Digital in with Schmitt Trigger 10: Low voltage digital in mode 11: Reserved/Analog IO
	1417		
	1418	GPIO12 output mode configuration	00: 1x Push-Pull 01: 2x Push-Pull 10: 1x Open-Drain pull down 11: 2x Open-Drain pull down
	1419		
	1420	Reserved	
	1421	GPIO12 Pull-up or Pull-down resistor selection	00: Floating (disconnected) 01: 10 kΩ 10: 100 kΩ 11: 1 MΩ
	1422		
	1423	GPIO12 Pull-up or Pull-down mode selection	0: Pull-down 1: Pull-up
B2	1424	Turn on I^2C open drain fast or slow	0: Turn on I2C open drain fast 1: Turn on I2C open drain slow
	1425	IO Latching Enable During Host Write	0: Disable 1: Pad digital output latches at previous state
	1426	Fast pull up or pull down during power up	0: Disable 1: Enable (During power-up, GPIO Pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value)
	1427	Pull pad to high when gpi_from_pad is high	0: Disable 1: Enable
	1428	Reserved	
	1429	Reserved	
	1430	Reserved	
	1431	Reserved	
B3	1432	Filter/Edge Detector Output Polarity	0: Non-inverted 1: Inverted
	1433	Edge Detect Mode	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
	1434		
	1435	Edge Detect Filter Function Select	0: Filter 1: Edge Detect
	1436	Reserved	
	1437	Reserved	
	1438	Reserved	
	1439	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
B4	1440	Edge Detect Mode	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
	1441		
	1442	Programmable Delay Selection	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
	1443		
	1444	Reserved	
	1445	Reserved	
	1446	Reserved	
	1447	Reserved	
B5	1448	OSC0 Divider Clock Source	0: Use OSC 1: Use External Clock Source
	1449	OSC0 Matrix power down or on selection	0: Matrix Down 1: Matrix On
	1450	OSC0 turn on by register	0: Auto on by Multi-Func CNT 1: Always On
	1451	OSC0 Divider Output0 control by matrix	0: Disable 1: Enable
	1452	OSC0 Divider Output1 control by matrix	0: Disable 1: Enable
	1453	OSC0 Pre-Divider Selection	00: DIV1 01: DIV2 10: DIV4 11: DIV8
	1454		
	1455	Reserved	
B6	1456	OSC1 Divider Clock Source	0: Use OSC 1: Use External Clock Source
	1457	OSC1 Matrix power down or on selection	0: Matrix Down 1: Matrix On
	1458	OSC1 turn on by register	0: Auto on by Multi-Func CNT 1: Always On
	1459	OSC1 Divider Output0 control by matrix	0: Disable 1: Enable
B6	1460	OSC1 Pre-Divider Selection	000: DIV1 001: DIV2 010: DIV4 011: DIV8 100: DIV12 101: DIV24 110: DIV48 111: DIV96
	1461		
	1462		
	1463	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
B7	1464	OSC0 OUT0 Post-Divider Selection	000: DIV1 001: DIV2 010: DIV3 011: DIV4 100: DIV8 101: DIV12 110: DIV24 111: DIV64
	1465		
	1466		
	1467	Reserved	
	1468	OSC0 OUT1 Post-Divider Selection	000: DIV1 001: DIV2 010: DIV3 011: DIV4 100: DIV8 101: DIV12 110: DIV24 111: DIV64
	1469		
	1470		
	1471	Reserved	
B8	1472	OSC1 OUT0 Post-Divider Selection	000: DIV1 001: DIV2 010: DIV3 011: DIV4 100: DIV8 101: DIV12 110: DIV24 111: DIV64
	1473		
	1474		
	1475	Reserved	
	1476	Reserved	
	1477	Reserved	
	1478	Reserved	
	1479	Reserved	
B9	1480	OSC1 Enable 100 ns delay	0: no delay 1: 100 ns delay
	1481	OSC1 Enable startup 1st edge function	0: Enable 1: Disable
	1482	OSC1 output synchronous type select	00: OSC will have 1-2 output pulses after Power Down 01: When OSC Power Down signal comes, OSC generates full output pulse and then stops 10: When OSC Power Down signal comes, OSC output goes low immediately 11: When OSC Power Down signal comes, OSC output goes low immediately
	1483		
B9	1484	OSC0 Enable 500 µs delay	0: 500 µs delay 1: no delay
	1485	Reserved	
	1486	OSC0 output synchronous type select	00: OSC will have 1-2 output pulses after Power Down 01: When OSC Power Down signal comes, OSC generates full output pulse and then stops 10: When OSC Power Down signal comes, OSC output goes low immediately 11: When OSC Power Down signal comes, OSC output goes low immediately
	1487		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
BA	1488	ACMP0 Vref Selection	000000: 25 mV 000001: 50 mV 011110: 775 mV 011111: 800 mV 100000: 825 mV 100001: 850 mV 100010~111110: Reserved 111111: external Vref (Default 25 mV)
	1489		
	1490		
	1491		
	1492		
	1493		
	1494	ACMP0 Hysteresis selection	00: 0 mV 01: 25 mV 10: 50 mV 11: 150 mV
	1495		
BB	1496	Reserved	
	1497	Reserved	
	1498	ACMPH0 Input Divider	00: 1x 01: 0.5x 10: Reserved 11: Reserved
	1499		
	1500	ACMP0 Input tie to V_{DD} Enable	0: Do not pull 1: Pull to V_{DD} (Pull positive input up to V_{DD})
	1501	Reserved	
	1502	Reserved	
	1503	Reserved	
BC	1504	ACMPH1 Vref Selection	000000: 25 mV 000001: 50 mV 011110: 775 mV 011111: 800 mV 100000: 825 mV 100001: 850 mV 100010~111110: Reserved 111111: external Vref (Default: 25 mV)
	1505		
	1506		
	1507		
	1508		
	1509		
BC	1510	ACMP1 Hysteresis selection	00: 0 mV 01: 25 mV 10: 50 mV 11: 150 mV
	1511		
BD	1512	Reserved	
	1513	Reserved	
	1514	ACMPH1 Input Divider	00: 1x 01: 0.5x 10: Reserved 11: Reserved
	1515		
	1516	ACMPH1 Input tie to ACMPH0 Enable	0: Do not pull 1: Pull to input of ACMPH0 (Pull positive input of ACMPH1 as the input of ACMPH0)
	1517	ACMP1 External Vref Select	0: Vinn of ACMPH1 from Pin 1: Vinn of ACMPH1 from Vinn of ACMPH0
	1518	Reserved	
	1519	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
BE	1520	ACMP reference voltage generator enable	0: Disable 1: Enable
	1521	ACMP Buffer Enable	0: Disable 1: Enable
	1522	ACMP Buffer Enable Selection	0: Enable by reg_buf_en 1: Enable by tempsense_en
	1523	ACMP Unit-gain-buffer enable	0: Disable and pass input voltage directly to output 1: Enable and apply UGB
	1524	ACMP Buffer Discharge	0: Disable discharge PIN9, GPIO5 1: Enable discharge PIN9, GPIO5
	1525	ACMP Buffer Select	00: Reserved (GND) 01: avref_acmph0 10: avref_acmph1 11: Tempsense Output
	1526		
	1527	Reserved	
BF	1528	ACMP Temp Sensor Enable	0: Do not select tempsense output as buffer out 1: Select tempsense output as buffer out
	1529	ACMP Temp Sensor Enable Select	0: Enable by tempsense_en 1: Enable by tempsense_en_matrix
	1530	Pass buffer output to ACMPH1 input	0: Do not pass 1: Pass
	1531	Bandgap control	0: BG always wake, non sleep 1: Sleep when w/s sleep
	1532	Option of Ibias enable	0: No change in ibias_en 1: Force ibias_en equal to bg_en
	1533	Reserved	
	1534	Reserved	
	1535	Reserved	
C0	1536	V_{DD} detector hysteresis selection	0: With hysteresis 0.1V 1: without hysteresis
	1537	BG, Vref gen and ACMP wake up sequence selection	0: Enable BG Vref gen and ACMP at same time 1: Enable BG first. After BG_ok, enable Vrefgen; After BG_ok and Vref_ok, enable ACMP
	1538	Reserved	
	1539	Reserved	
	1540	Reserved	
	1541	Reserved	
	1542	Reserved	
	1543	Reserved	
C1	1544	Reserved	
	1545	Reserved	
	1546	Reserved	
	1547	Reserved	
	1548	Reserved	
	1549	Reserved	
	1550	Reserved	
	1551	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
C2	1552	Reserved	
	1553		
	1554		
	1555		
	1556		
	1557		
	1558		
	1559		
C3	1560	Reserved	
	1561		
	1562	Reserved	
	1563		
	1564	Reserved	
	1565		
	1566	Reserved	
	1567	Reserved	
C4	1568	Reserved	
	1569		
	1570		
	1571		
	1572		
	1573		
	1574		
	1575	Reserved	
C5	1576	Reserved	
	1577		
	1578	Reserved	
	1579	Reserved	
	1580	Reserved	
	1581		
	1582		
	1583		
C6	1584	Reserved	
	1585		
	1586		
	1587		
	1588	Reserved	
C6	1589	Reserved	
	1590	Reserved	
	1591	Reserved	
C7	1592	Reserved	
	1593		
	1594		
	1595		
	1596	Reserved	
	1597	Reserved	
	1598	Reserved	
	1599	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
C8	1600	Reserved	
	1601	Reserved	
	1602	Reserved	
	1603	Reserved	
	1604	Reserved	
	1605	Reserved	
	1606	Reserved	
	1607	Reserved	
C9	1608	Reserved	
	1609	Reserved	
	1610	Reserved	
	1611	Reserved	
C9	1612	Reserved	
	1613	Reserved	
	1614	Reserved	
	1615	Reserved	
CA	1616	Reserved	
	1617	Reserved	
	1618		
	1619		
	1620	Reserved	
	1621	Reserved	
	1622	Reserved	
	1623	Reserved	
CB	1624	Reserved	
	1625		
	1626	Reserved	
	1627		
	1628	Reserved	
	1629	Reserved	
	1630	Reserved	
	1631	Reserved	
CC	1632	Reserved	
	1633		
	1634	Reserved	
	1635		
CC	1636	Reserved	
	1637		
	1638	Reserved	
	1639		
CD	1640	Reserved	
	1641		
	1642	Reserved	
	1643		
	1644	Reserved	
	1645		
	1646	Reserved	
	1647		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
CE	1648	Reserved	
	1649		
	1650		
	1651		
	1652		
	1653	Reserved	
	1654	Reserved	
	1655	Reserved	
CF	1656	Reserved	
	1657		
	1658		
	1659		
	1660		
	1661	Reserved	
	1662	Reserved	
	1663	Reserved	
D0	1664	Reserved	
	1665		
	1666		
	1667		
	1668		
	1669		
	1670	Reserved	
	1671	Reserved	
D1	1672	Reserved	
	1673		
	1674		
	1675		
	1676		
	1677		
	1678		
	1679	Reserved	
D2	1680	Reserved	
	1681		
	1682		
	1683		
	1684		
	1685		
	1686		
	1687	Reserved	
D3	1688	Reserved	
	1689		
	1690		
	1691		
	1692	Reserved	
	1693	Reserved	
	1694	Reserved	
	1695	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
D4	1696	Reserved	
	1697		
	1698		
	1699		
	1700		
	1701	Reserved	
	1702	Reserved	
	1703	Reserved	
D5	1704	Reserved	
	1705		
	1706		
	1707		
	1708		
	1709		
	1710		
	1711		
D6	1712	Reserved	
	1713		
	1714		
	1715		
	1716		
	1717		
	1718		
	1719		
D7	1720	RPR	Registers Read Protection Register. Valid only when PROTECT_EN is 1 00: 1K register data is unprotected for read 01: 1K register data is partly protected for read 10: 1K register data is fully protected for read 11: 1K register data is fully protected for read
	1721		
	1722	WPR	Registers Write Protection Register. Valid only when PROTECT_EN is 1 00: 1K register data is unprotected for write 01: 1K register data is partly protected for write 10: 1K register data is fully protected for write 11: 1K register data is fully protected for write
	1723		
	1724	Reserved	
	1725		
	1726	Reserved	
	1727	Reserved	
D8	1728	Reserved	
	1729		
	1730		
	1731		
	1732		
	1733		
	1734		
	1735		

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
D9	1736	Reserved	
	1737		
	1738		
	1739		
	1740		
	1741		
	1742		
	1743		
DA	1744	Reserved	
	1745		
	1746		
	1747		
	1748		
	1749		
	1750		
	1751		
DB	1752	Reserved	
	1753		
	1754		
	1755		
	1756		
	1757		
	1758		
	1759		
DC	1760	Reserved	
	1761		
	1762		
	1763		
	1764		
	1765		
	1766		
	1767		
DD	1768	Reserved	
	1769	Reserved	
	1770	Reserved	
	1771	Reserved	
	1772	Reserved	
	1773	Reserved	
	1774	Reserved	
	1775	Reserved	
DE	1776	Reserved	
	1777	Reserved	
	1778	Reserved	
	1779	Reserved	
	1780	Reserved	
	1781	Reserved	
	1782	Reserved	
	1783	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
DF	1784	Reserved	
	1785	Reserved	
	1786	Reserved	
	1787	Reserved	
	1788	Reserved	
	1789	Reserved	
	1790	Reserved	
	1791	Reserved	
E0	1792	Reserved	
	1793	Reserved	
	1794	Reserved	
	1795	Reserved	
	1796	Reserved	
	1797	Reserved	
	1798	Reserved	
	1799	Reserved	
E1	1800	Reserved	
	1801	Reserved	
	1802	Reserved	
	1803	Reserved	
	1804	Reserved	
	1805	Reserved	
	1806	Reserved	
	1807	Reserved	
E2	1808	Reserved	
	1809	Reserved	
	1810	Reserved	
	1811	Reserved	
	1812	Reserved	
	1813	Reserved	
	1814	Reserved	
	1815	Reserved	
E3	1816	Reserved	
	1817	Reserved	
	1818	Reserved	
	1819	Reserved	
	1820	Reserved	
	1821	Reserved	
	1822	Reserved	
	1823	Reserved	
E4	1824	Reserved	
	1825	Reserved	
	1826	Reserved	
	1827	Reserved	
	1828	Reserved	
	1829	Reserved	
	1830	Reserved	
	1831	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
E5	1832	Reserved	
	1833	Reserved	
	1834	Reserved	
	1835	Reserved	
	1836	Reserved	
	1837	Reserved	
	1838	Reserved	
	1839	Reserved	
E6	1840	Reserved	
	1841	Reserved	
	1842	Reserved	
	1843	Reserved	
	1844	Reserved	
	1845	Reserved	
	1846	Reserved	
	1847	Reserved	
E7	1848	Reserved	
	1849	Reserved	
	1850	Reserved	
	1851	Reserved	
	1852	Reserved	
	1853	Reserved	
	1854	Reserved	
	1855	Reserved	
E8	1856	Reserved	
	1857	Reserved	
	1858	Reserved	
	1859	Reserved	
	1860	Reserved	
	1861	Reserved	
	1862	Reserved	
	1863	Reserved	
E9	1864	Reserved	
	1865	Reserved	
	1866	Reserved	
	1867	Reserved	
	1868	Reserved	
	1869	Reserved	
	1870	Reserved	
	1871	Reserved	
EA	1872	Reserved	
	1873	Reserved	
	1874	Reserved	
	1875	Reserved	
	1876	Reserved	
	1877	Reserved	
	1878	Reserved	
	1879	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
EB	1880	Reserved	
	1881	Reserved	
	1882	Reserved	
	1883	Reserved	
	1884	Reserved	
	1885	Reserved	
	1886	Reserved	
	1887	Reserved	
EC	1888	Reserved	
	1889	Reserved	
	1890	Reserved	
	1891	Reserved	
	1892	Reserved	
	1893	Reserved	
	1894	Reserved	
	1895	Reserved	
ED	1896	Reserved	
	1897	Reserved	
	1898	Reserved	
	1899	Reserved	
	1900	Reserved	
	1901	Reserved	
	1902	Reserved	
	1903	Reserved	
EE	1904	Reserved	
	1905	Reserved	
	1906	Reserved	
	1907	Reserved	
	1908	Reserved	
	1909	Reserved	
	1910	Reserved	
	1911	Reserved	
EF	1912	Reserved	
	1913	Reserved	
	1914	Reserved	
	1915	Reserved	
	1916	Reserved	
	1917	Reserved	
	1918	Reserved	
	1919	Reserved	
F0	1920	Reserved	
	1921	Reserved	
	1922	Reserved	
	1923	Reserved	
	1924	Reserved	
	1925	Reserved	
	1926	Reserved	
	1927	Reserved	

Table 38: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F1	1928	Reserved	
	1929	Reserved	
	1930	Reserved	
	1931	Reserved	
	1932	Reserved	
	1933	Reserved	
	1934	Reserved	
	1935	Reserved	
F2	1936	Reserved	
	1937	Reserved	
	1938	Reserved	
	1939	Reserved	
	1940	Reserved	
	1941	Reserved	
	1942	Reserved	
	1943	Reserved	
F3	1944	Reserved	
	1945	Reserved	
	1946	Reserved	
	1947	Reserved	
	1948	Reserved	
	1949	Reserved	
	1950	Reserved	
	1951	Reserved	
F4	1952	Reserved	
	1953	Reserved	
	1954	Reserved	
	1955	Reserved	
	1956	Reserved	
	1957	Reserved	
	1958	Reserved	
	1959	Reserved	
F5	1960	Reserved	
	1961	Reserved	
	1962	Reserved	
	1963	Reserved	
	1964	Reserved	
	1965	Reserved	
	1966	Reserved	
	1967	Reserved	
F6	1968	Reserved	
	1969	Reserved	
	1970	Reserved	
	1971	Reserved	
	1972	Reserved	
	1973	Reserved	
	1974	Reserved	
	1975	Reserved	

Table 38: Register Map (Continued)

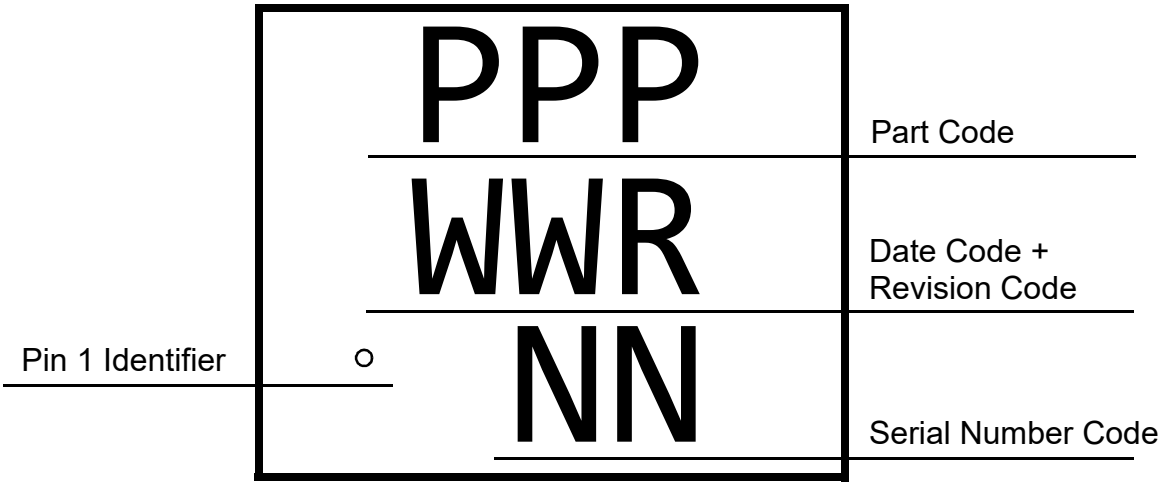
Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F7	1976	Reserved	
	1977	Reserved	
	1978	Reserved	
	1979	Reserved	
	1980	Reserved	
	1981	Reserved	
	1982	Reserved	
	1983	Reserved	
F8	1984	Reserved	
	1985	Reserved	
	1986	Reserved	
	1987	Reserved	
	1988	Reserved	
	1989	Reserved	
	1990	Reserved	
	1991	Reserved	
F9	1992	Reserved	
	1993	Reserved	
	1994	Reserved	
	1995	Reserved	
	1996	Reserved	
	1997	Reserved	
	1998	Reserved	
	1999	Reserved	
FA	2000	Reserved	
	2001	Reserved	
	2002	Reserved	
	2003	Reserved	
	2004	Reserved	
	2005	Reserved	
	2006	Reserved	
	2007	Reserved	
FB	2008	Reserved	
	2009	Reserved	
	2010	Reserved	
	2011	Reserved	
	2012	Reserved	
	2013	Reserved	
	2014	Reserved	
	2015	Reserved	
FC	2016	Reserved	
	2017	Reserved	
	2018	Reserved	
	2019	Reserved	
	2020	Reserved	
	2021	Reserved	
	2022	Reserved	
	2023	Reserved	

Table 38: Register Map (Continued)

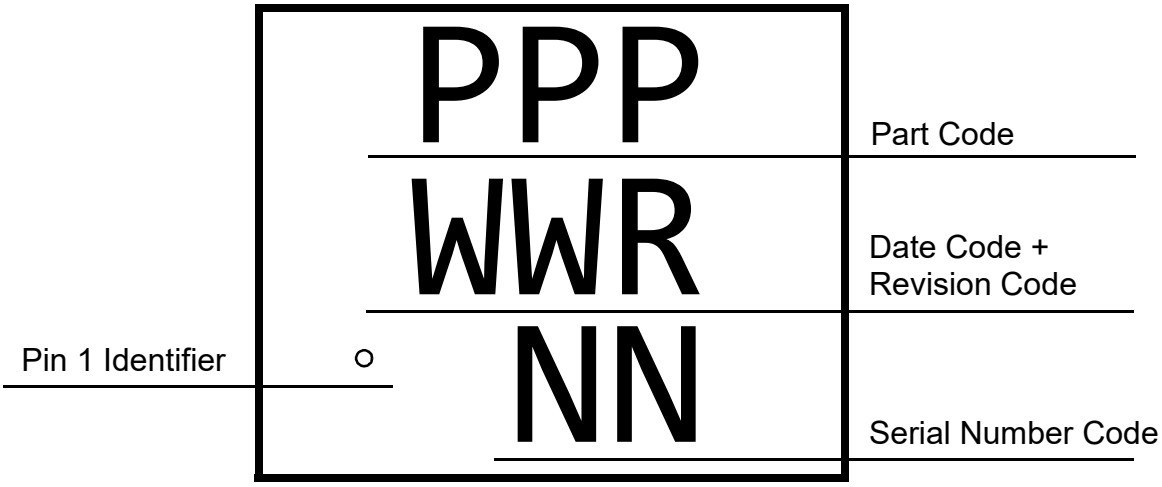
Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
FD	2024	Reserved	
	2025	Reserved	
	2026	Reserved	
	2027	Reserved	
	2028	Reserved	
	2029	Reserved	
	2030	Reserved	
	2031	Reserved	
FE	2032	Reserved	
	2033	Reserved	
	2034	Reserved	
	2035	Reserved	
	2036	Reserved	
	2037	Reserved	
	2038	Reserved	
	2039	Reserved	
FF	2040	Reserved	
	2041	Reserved	
	2042	Reserved	
	2043	Reserved	
	2044	Reserved	
	2045	Reserved	
	2046	Reserved	
	2047	Reserved	

18 Package Top Marking Definitions

18.1 STQFN 12L 1.6 MM X 1.6 MM X 0.55 MM 0.4P FC



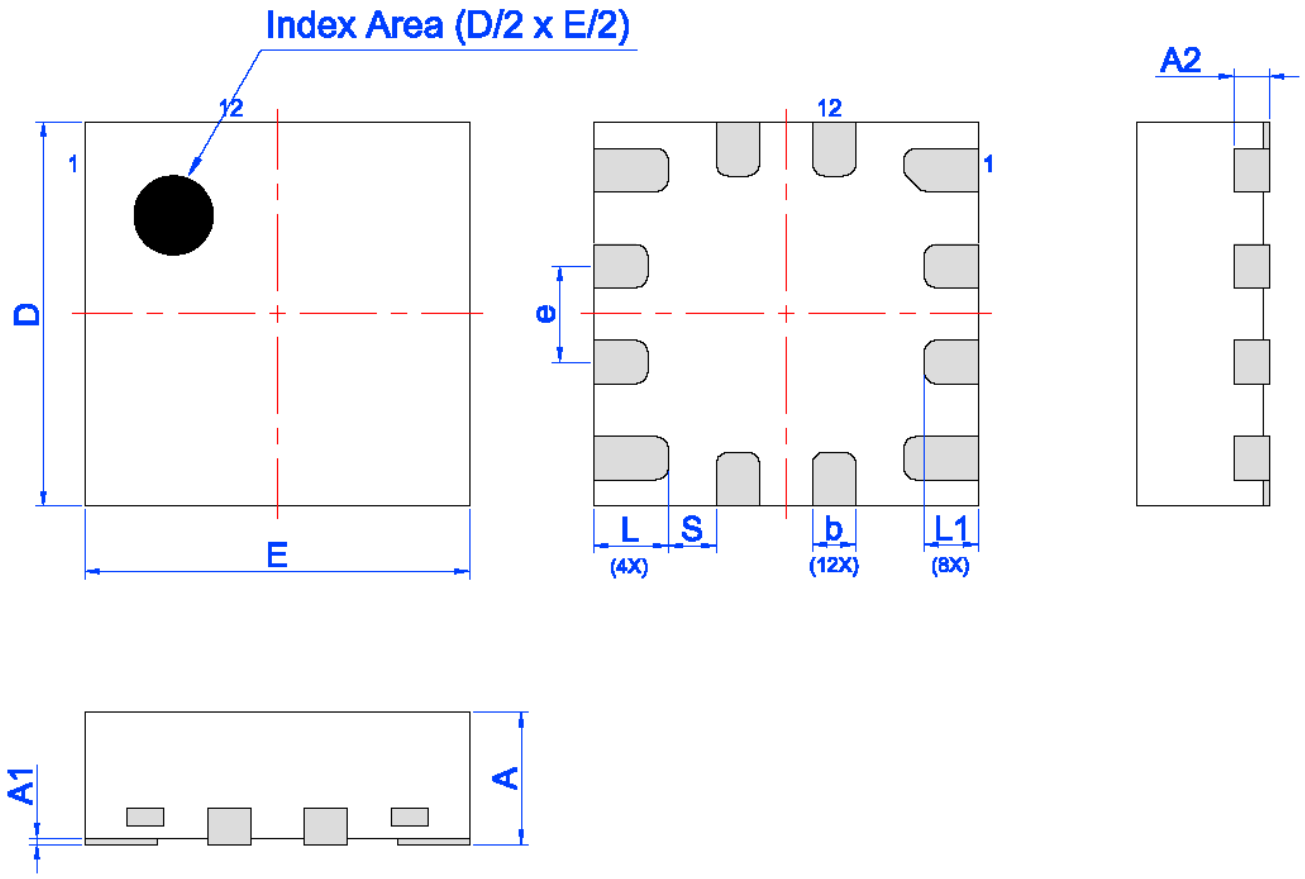
18.2 MSTQFN 16L 1.6 MM X 1.6 MM X 0.55 MM 0.4P



19 Package Information

19.1 PACKAGE OUTLINES FOR STQFN 12L 1.6 MM X 1.6 MM X 0.55 MM 0.4P FC PACKAGE

JEDEC MO-220
IC Net Weight: 0.0035 g

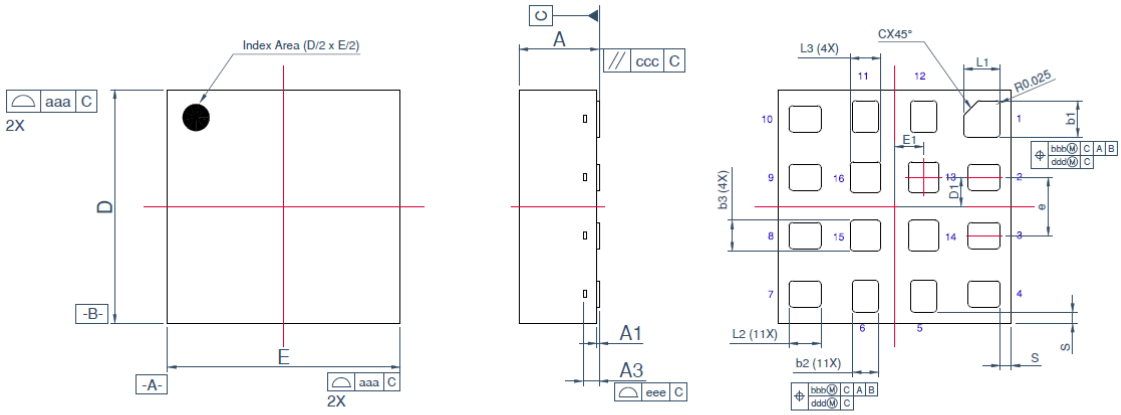


Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

19.2 PACKAGE OUTLINES FOR MSTQFN 16L 1.6 MM X 1.6 MM X 0.55 MM 0.4P PACKAGE

JEDEC MO-220
IC Net Weight: 0.0043 g



Top View **Side View** **Bottom View**

Controlling Dimensions: mm

SYMBOL	MILLIMETER			INCH		
	MIN	NOR	MAX	MIN	NOR	MAX
A	0.500	0.550	0.600	0.020	0.022	0.024
A1	0.00	0.005	0.010	0.0000	0.0002	0.0004
A3		0.11 REF			0.004 REF	
D	1.550	1.600	1.650	0.061	0.063	0.065
E	1.550	1.600	1.650	0.061	0.063	0.065
b1	0.200	0.250	0.300	0.008	0.010	0.012
b2	0.130	0.180	0.230	0.005	0.007	0.009
b3	0.160	0.210	0.260	0.006	0.008	0.010
L1	0.200	0.250	0.300	0.008	0.010	0.012
L2	0.170	0.220	0.270	0.007	0.009	0.011
L3	0.160	0.210	0.260	0.006	0.008	0.010
e		0.400 BSC			0.016 BSC	
C		0.100 REF			0.004 REF	
D1		0.200 BSC			0.008 BSC	
E1		0.200 BSC			0.008 BSC	
S		0.075 REF			0.003 REF	
aaa		0.1			0.004	
bbb		0.07			0.003	
ddd		0.05			0.002	
eee		0.05			0.002	
fff		0.05			0.002	

19.3 MOISTURE SENSITIVITY LEVEL

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 39.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The <PACKAGE_NAME> package is qualified for MSL <n>.

Table 39: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C/60 % RH
MSL 3	168 hours	30 °C/60 % RH
MSL 2A	4 weeks	30 °C/60 % RH
MSL 2	1 year	30 °C/60 % RH
MSL 1	Unlimited	30 °C/60 % RH

19.4 STQFN HANDLING

Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

19.5 SOLDERING INFORMATION

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

20 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Renesas Electronics Corporation's or your local sales representative.

Part Number	Type
SLG47512V	12-pin STQFN
SLG47512VTR	12-pin STQFN - Tape and Reel (3k units)
SLG47513M	16-pin MSTQFN
SLG47513MTR	16-pin MSTQFN - Tape and Reel (3k units)

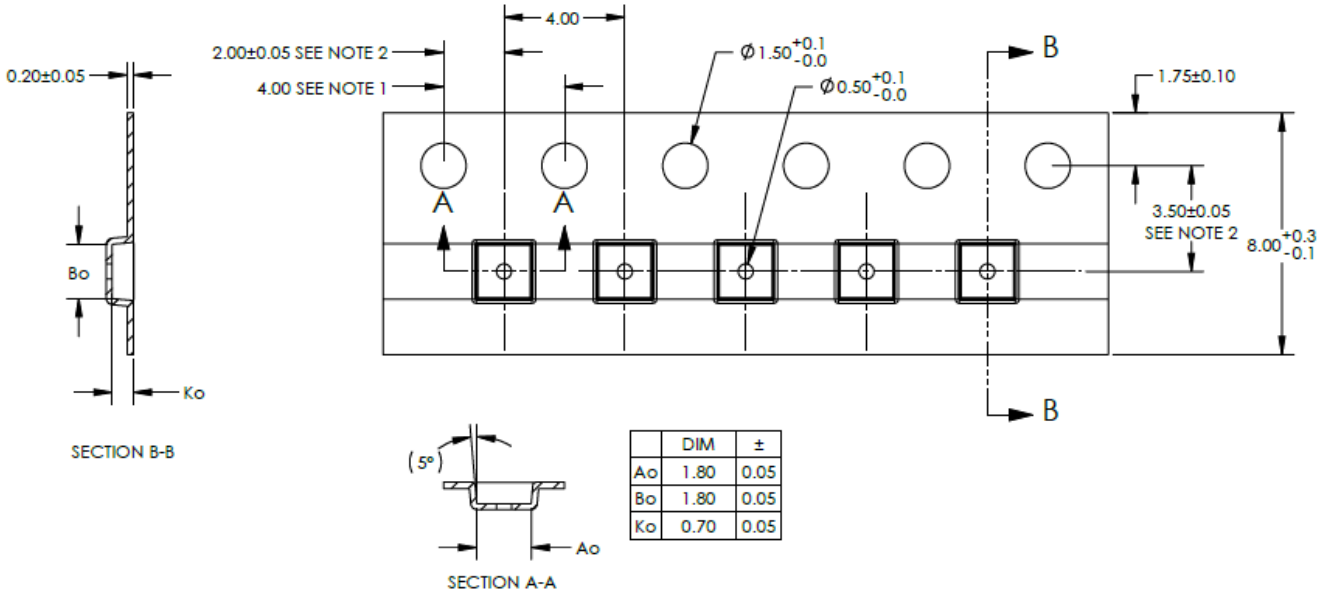
Note 1 Use SLG47512V or SLG47513M to order. Shipments are automatically in Tape and Reel.
Note 2 "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

20.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 12L 1.6 mm x 1.6 mm x 0.55 mm, 0.4P FCA Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4
MSTQFN 16L 1.6 mm x 1.6 mm x 0.55 mm, 0.4P FCA Green	16	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

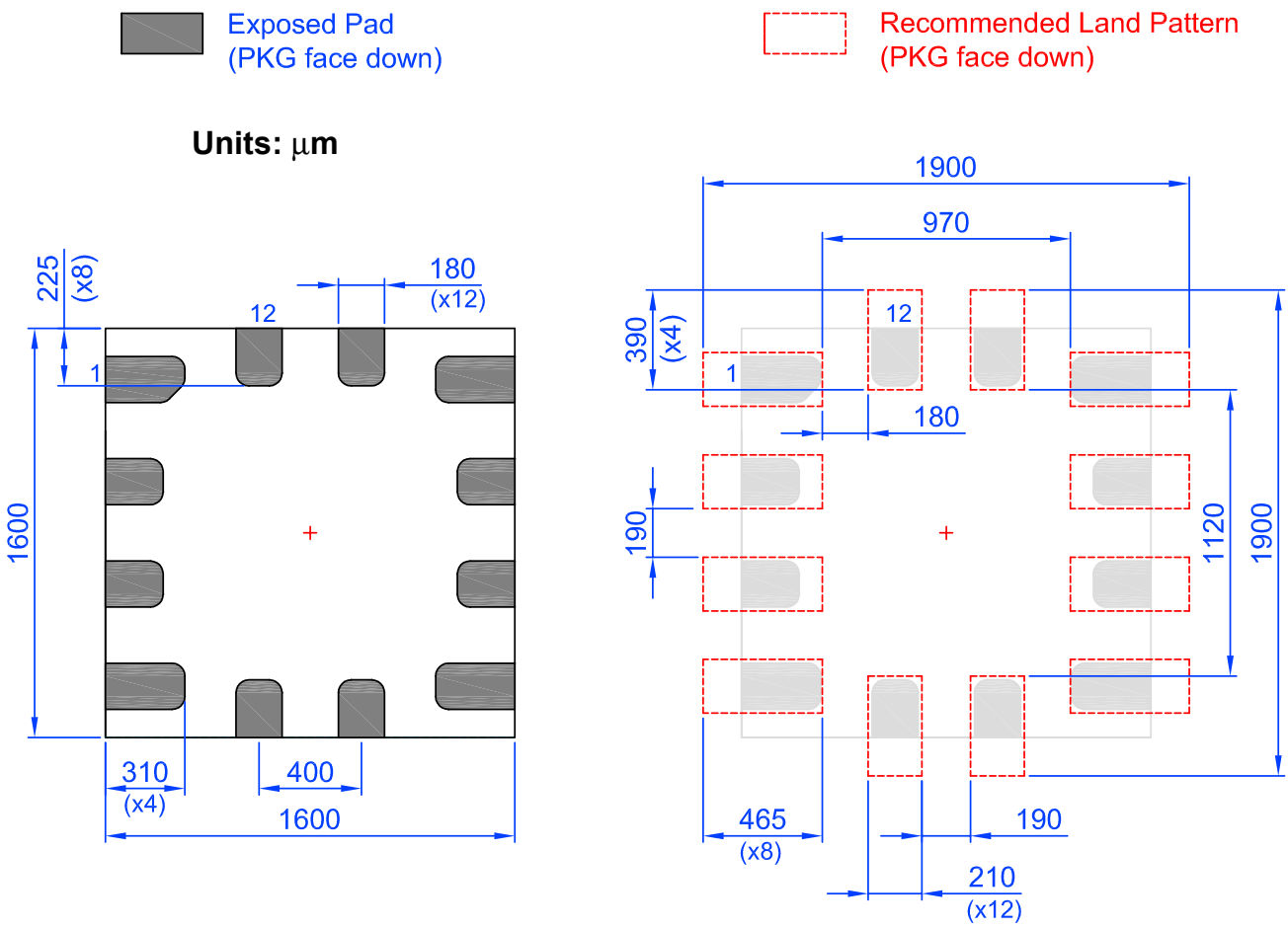
20.2 CARRIER TAPE DRAWING AND DIMENSIONS

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L 1.6 mm x 1.6 mm x 0.55 mm, 0.4P FCA Green	1.80 ±0.05 mm	1.80 ±0.05 mm	0.70 ±0.05 mm	4	4	1.5	1.75	3.5	8
MSTQFN 16L 1.6 mm x 1.6 mm x 0.55 mm, 0.4P FCA Green	1.80 ±0.05 mm	1.80 ±0.05 mm	0.70 ±0.05 mm	4	4	1.5	1.75	3.5	8

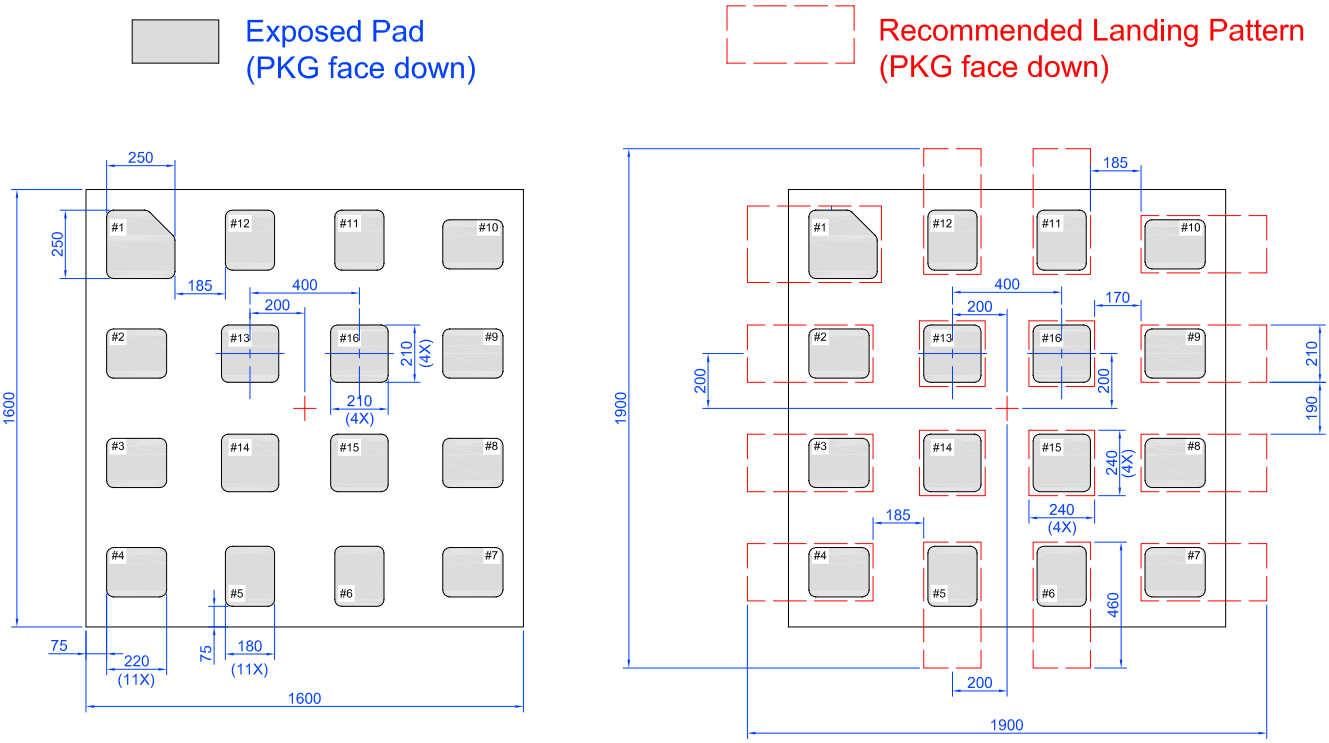


21 Layout Guidelines

21.1 STQFN 12L 1.6 MM X 1.6 MM X 0.55 MM 0.4P FC PACKAGE



21.2 MSTQFN 16L 1.6 MM X 1.6 MM X 0.55 MM 0.4P PACKAGE



Unit: µm

Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High Speed
ACMPL	Analog Comparator Low Power

B

BG	Bandgap

C

CLK	Clock
CMO	Connection matrix output
CNT	Counter

D

DFF	D Flip-Flop
DLY	Delay

E

ESD	Electrostatic discharge
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

L

LPF	Low Pass Filter
LSB	Least Significant Bit
LUT	Look Up Table

LV	Low Voltage

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OD	Open-Drain
OE	Output Enable
OSC	Oscillator
OTP	One Time Programmable
OUT	Output

P

PD	Power-down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-Pull
PWR	Power
P DLY	Programmable Delay

R

R/W	Read/Write

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address
SMT	With Schmitt Trigger
SV	nSET Value

T

TS	Temperature Sensor

V

Vref	Voltage Reference

W

WOSMT	Without Schmitt Trigger
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
2.3	28-Feb-2023	Added notes to section Ordering Information Updated subsection I^2C Serial Communications Device Addressing Updated subsection Byte Write Command Updated section 2-Bit LUT or D Flip-Flop or Shift Register Macrocells Updated section 3-Bit LUT or D Flip-Flop with Set/Reset or Shift Register Macrocells Updated section 4-Bit LUT or D Flip-Flop with Set/Reset or Shift Register Macrocell
2.2	9-Mar-2022	Updated table Typical Counter/Delay Offset Updated R_{PULL} in section Electrical Characteristics Updated table ACMP Specifications Added TS Output vs. Temperature Graph Updated section Analog Temperature Sensor Characteristics Renesas rebranding Added IC Net Weight in Package Information section Updated V_{HYS} in table ACMP Specifications Updated table Oscillators Frequency Limits
2.1	12-Oct-2021	Updated section Electrical Characteristics
2.0	1-Sep-2021	Preliminary version

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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