General Description

Renesas SLG7NT4375 is a low power and small form device. The SoC is housed in a 1.6 x 1.6 mm STQFN package which is optimal for using with small devices.

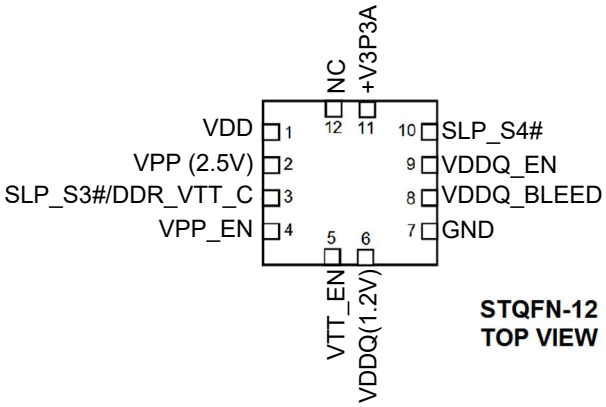
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 12 Package
- MSL “1”

Output Summary

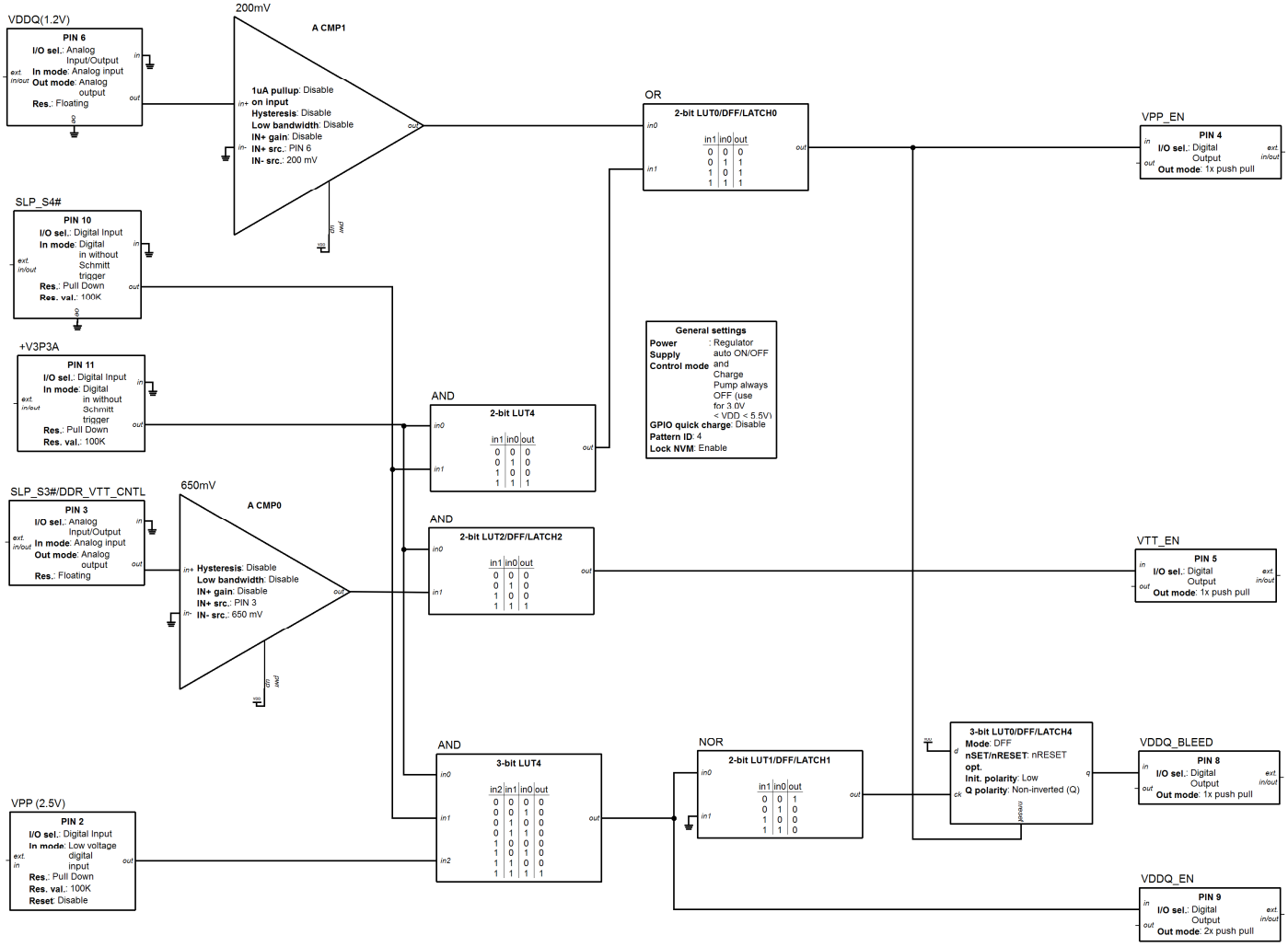
- 3 Outputs — Push Pull 1X
- 1 Output — Open Drain NMOS 1X

Pin Configuration



STQFN-12
TOP VIEW

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	VPP (2.5V)	Digital Input	Low Voltage Digital input
3	SLP_S3#/DDR_VTT_CNTL	Analog Input/Output	Analog Input/Output
4	VPP_EN	Digital Output	Push Pull 1X
5	VTT_EN	Digital Output	Push Pull 1X
6	VDDQ(1.2V)	Analog Input/Output	Analog Input/Output
7	GND	GND	Ground
8	VDDQ_BLEED	Digital Output	Push Pull 1X
9	VDDQ_EN	Digital Output	Push Pull 2X
10	SLP_S4#	Digital Input	Digital Input without Schmitt trigger
11	+V3P3A	Digital Input	Digital Input without Schmitt trigger
12	NC	--	Keep Floating or Connect to GND

Ordering Information

Part Number	Package Type
SLG7NT4375V	V=STQFN-12
SLG7NT4375VTR	STQFN-12 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1000	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	70	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current	Per Each Chip Side	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=3.3V	1.4	--	VDD	V
		Low-Level Logic Input, at VDD=3.3V	0.91	--	VDD	
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=3.3V	--	--	1.65	V
		Low-Level Logic Input, at VDD=3.3V	--	--	0.95	
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push Pull, I_{OH} = 3mA, 1X Driver, at VDD=3.3 V	2.73	3.13	--	V
		Push Pull, I_{OH} = 3mA, 2X Driver, at VDD=3.3 V	2.87	3.22	--	
V_{OL}	LOW-Level Output Voltage	Push Pull, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.15	0.28	V
		Push Pull, I_{OL} = 3mA, 2X Driver, at VDD=3.3 V	--	0.07	0.13	
I_{OH}	HIGH-Level Output Current	Push Pull & PMOS OD, V_{OH} = 2.4 V, 1X Driver, at VDD=3.3 V	6.01	12.07	--	mA
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 2X Driver, at VDD=3.3 V	12.01	24.13	--	
I_{OL}	LOW-Level Output Current	Push Pull, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	4.06	6.92	--	mA
		Push Pull, V_{OL} =0.4V, 2X Driver, at VDD=3.3 V	8.13	13.84	--	

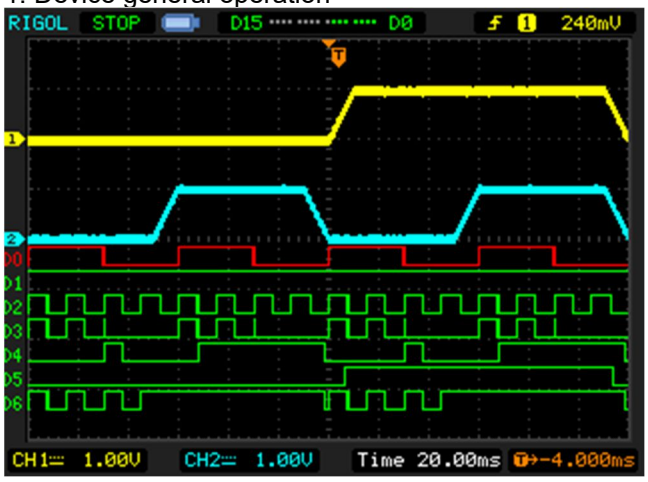
V_{ACMP0}	Analog Comparator Threshold Voltage	ACMP0 threshold including input offset, reference voltage variation and hysteresis.	620	--	677	mV
V_{ACMP1}	Analog Comparator Threshold Voltage	ACMP1 threshold including input offset, reference voltage variation and hysteresis.	186	--	214	mV
T_{SU}	Start up Time	From VDD rising past 1.6V	--	1	--	ms

1. Guaranteed by Design.

Functionality Waveforms

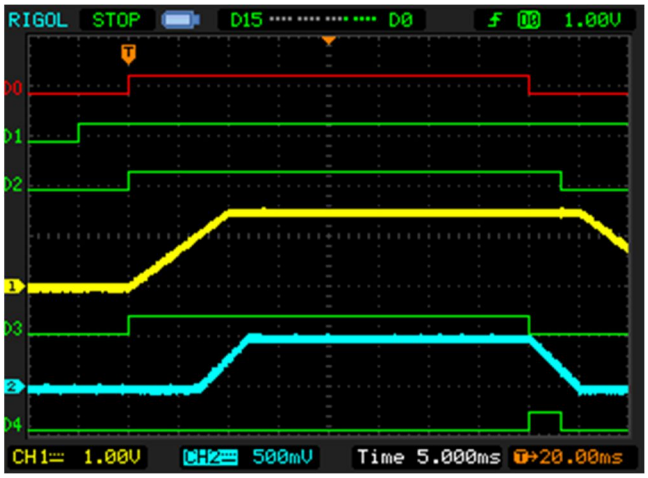
Channel 1 (yellow/top line) – PIN#3 (SLP_S3#/DDR_VTT_CNTL)
Channel 2 (light blue/2nd line) – PIN#6 (VDDQ(1.2V))
D0 – PIN#2 (VPP (2.5V))
D1 – PIN#11 (+V3P3A)
D2 – PIN#10 (SLP_S4#)
D3 – PIN#9 (VDDQ_EN)
D4 – PIN#8 (VDDQ_BLEED)
D5 – PIN#5 (VTT_EN)
D6 – PIN#4 (VPP_EN)

1. Device general operation



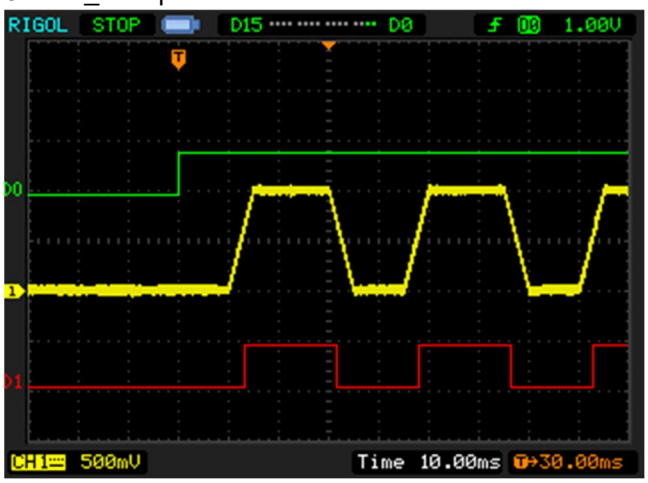
D0 – PIN#10 (SLP_S4#)
D1 – PIN#11 (+V3P3A)
D2 – PIN#4 (VPP_EN)
Channel 1 (yellow/top line) – PIN#3 (SLP_S3#/DDR_VTT_CNTL)
D3 – PIN#9 (VDDQ_EN)
Channel 2 (light blue/2nd line) – PIN#6 (VDDQ(1.2V))
D4 – PIN#8 (VDDQ_BLEED)

2. Enable PIN: SLP_S4#

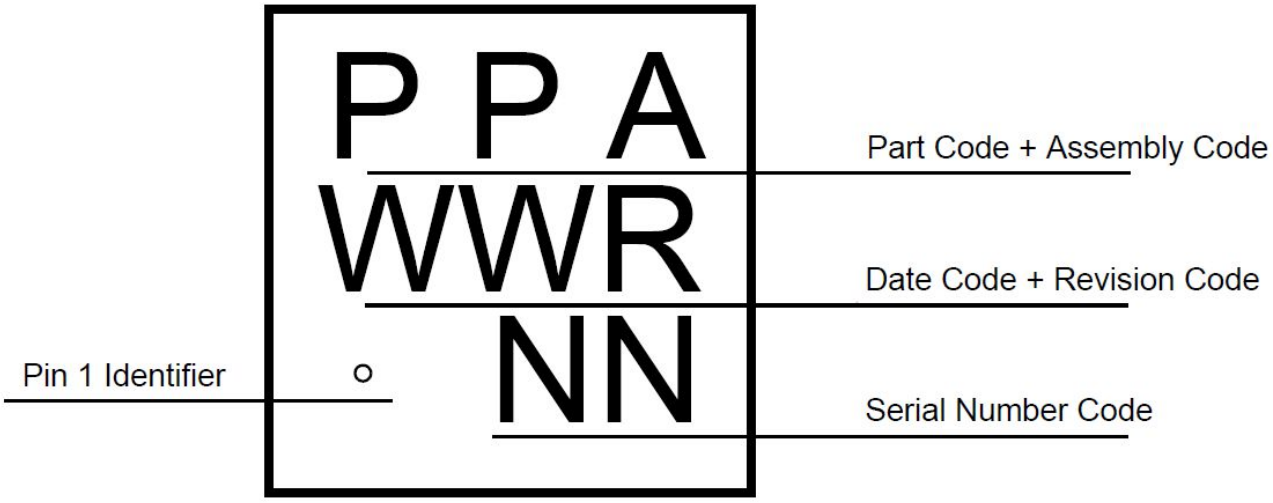


D0 – PIN#11 (+V3P3A)
Channel 1 (yellow/top line) – PIN#3 (SLP_S3#/DDR_VTT_CNTL)
D1 – PIN#5 (VTT_EN)

3. VTT_EN operation



Package Top Marking

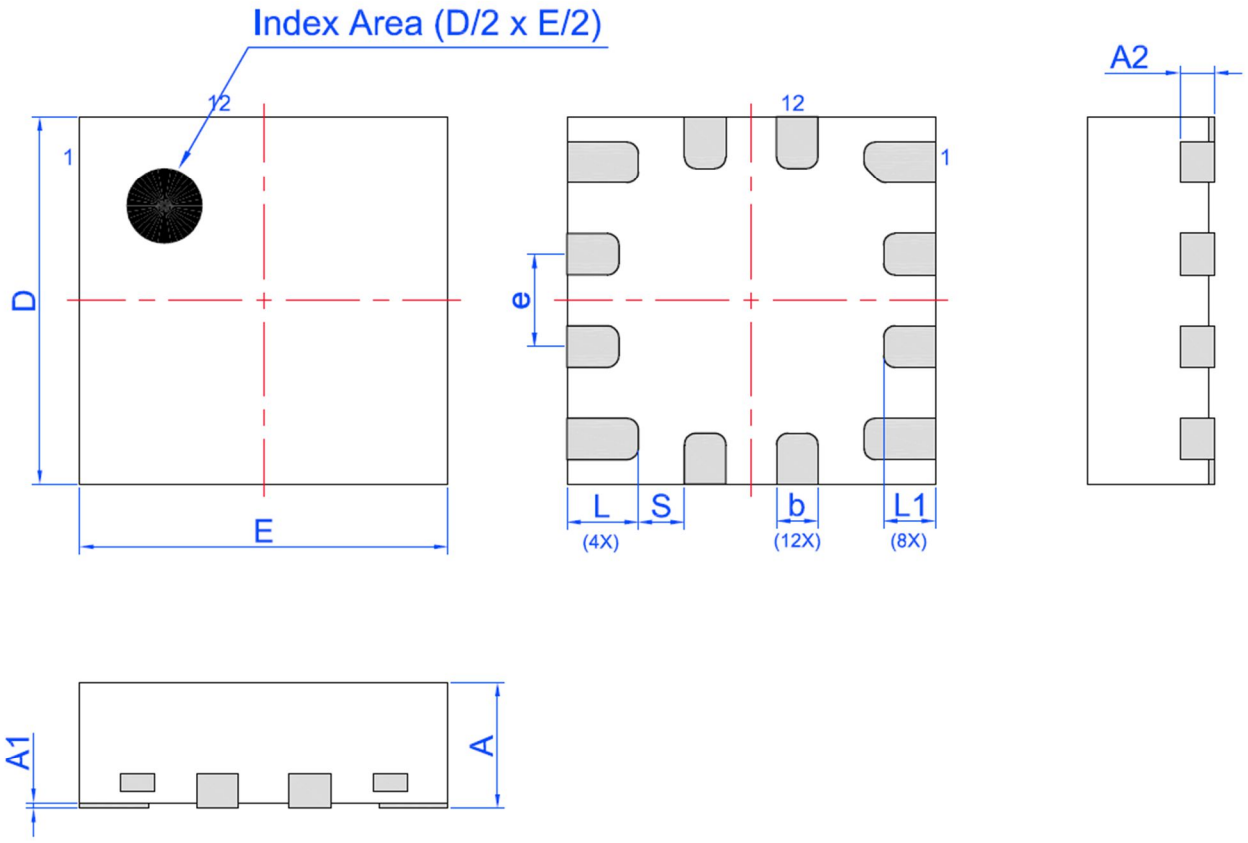


Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.04	004	L	YV	B	02/25/2022

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

12 Lead STQFN FCA Package 1.6 x 1.6 mm



Unit: mm

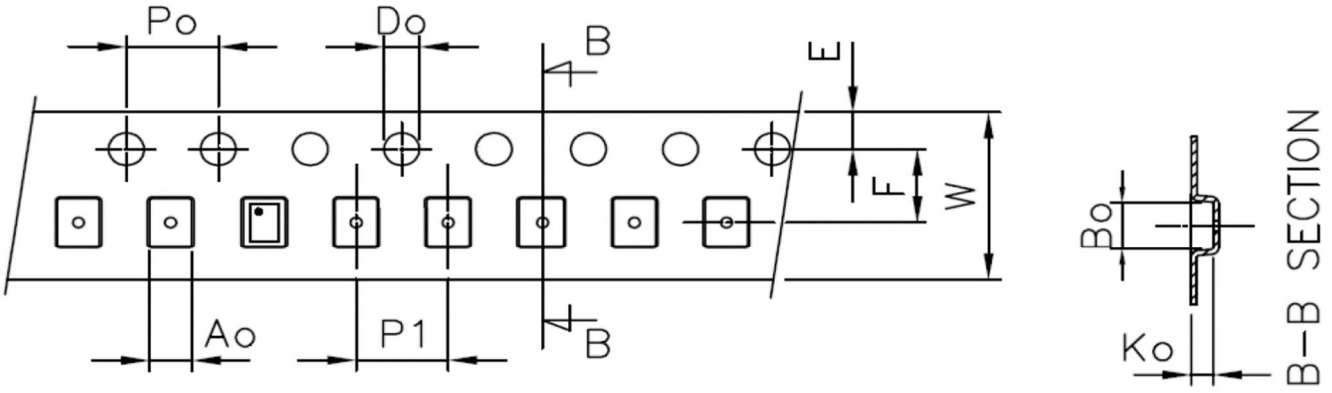
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 12L FCA 0.4P Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

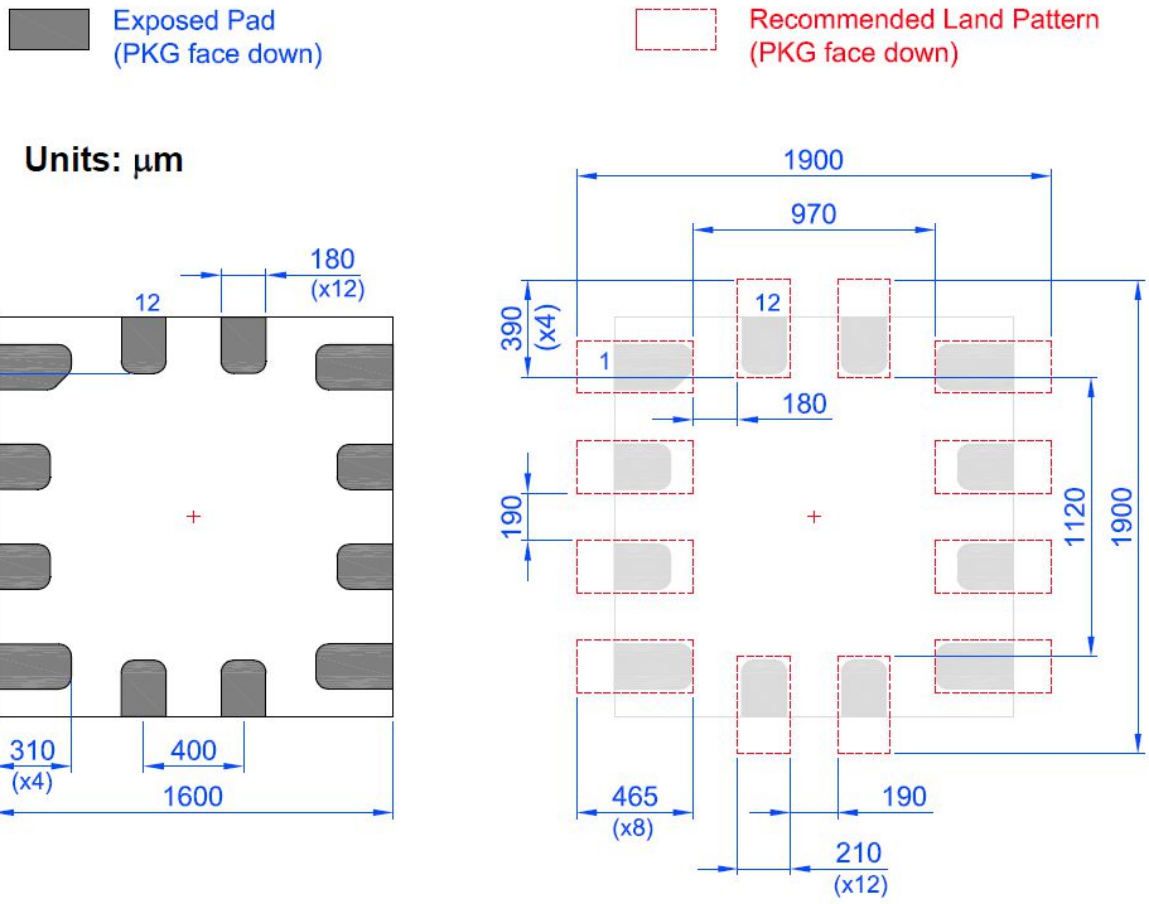
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FCA 0.4P Green	1.9	1.9	0.8	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern



Datasheet Revision History

]Date	Version	Change
03/27/2014	0.10	New designSLG46120
03/28/2014	0.11	Corrected device functionality
04/02/2014	0.12	Change PIN5 name VTT to VTT_EN, correctedElectrical Characteristics
04/24/2014	0.13	Removed LATCH from VPP_EN, ACMP1 Vref changed to 200mV
04/28/2014	0.14	Added one more Functionality Waveform
05/05/2014	0.15	Added additional Functionality Waveforms
05/23/2014	0.16	Version update
07/25/2014	0.17	Updated Device Revision Table
08/25/2014	0.18	Added MSL “1” Renamed Package to FCA package
09/03/2014	0.19	Changed PIN11 name, updated functionality waveforms
09/05/2014	0.20	Removed one functionality waveform
09/25/2014	0.21	Updated Device Revision Table
10/02/2014	0.22	Changed Lock status
10/03/2014	0.23	Updated VIH, VIL logic levels
10/03/2014	0.24	Updated Device Revision Table
11/06/2014	1.00	Production Release
02/23/2015	1.01	Corrected VDDQ_EN output type
11/29/2018	1.02	Updated style and formatting
09/16/2020	1.03	Fixed typos
02/24/2022	1.04	Updated Company name and logo