SLG7NT4505
GreenPAK™
1 Hz Interrupt Generator

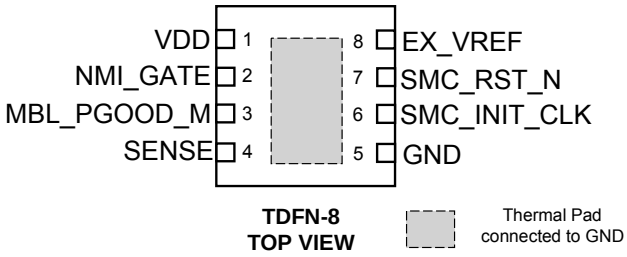
General Description

Silego GreenPAK SLG7NT4505 is a low power and small form device. The SoC is housed in a 2mm x 2mm TDFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- 3.3V Supply
- Pb-Free / RoHS Compliant
- Halogen-Free
- TDFN-8 Package

Pin Configuration



Output Summary

- 2 Outputs — Open Drain NMOS 1X

Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	3.3V Supply Voltage
2	NMI_GATE	Digital Input	Digital Input without Schmitt trigger
3	MBL_PGOOD_MR	Digital Input	Digital Input without Schmitt trigger
4	SENSE	Analog Input/Output	Analog Input/Output
5	GND	GND	Ground
6	SMC_INIT_CLK	Digital Output	Open Drain NMOS 1X
7	SMC_RST_N	Digital Output	Open Drain NMOS 1X
8	EX_VREF	Analog Input/Output	Analog Input/Output
Exposed Bottom Pad	GND	GND	Ground

Ordering Options & Configuration

Part Number	Package Type
SLG7NT4505V	V = TDFN-8
SLG7NT4505VTR	VTR = TDFN-8 – Tape and Reel (3k units)

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_{DD} to GND	-0.3	4.6	V
Voltage at input pins	-0.3	4.6	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C
ESD Human Body Model	2000	--	V
ESD Machine Model	200	--	V

Electrical Characteristics

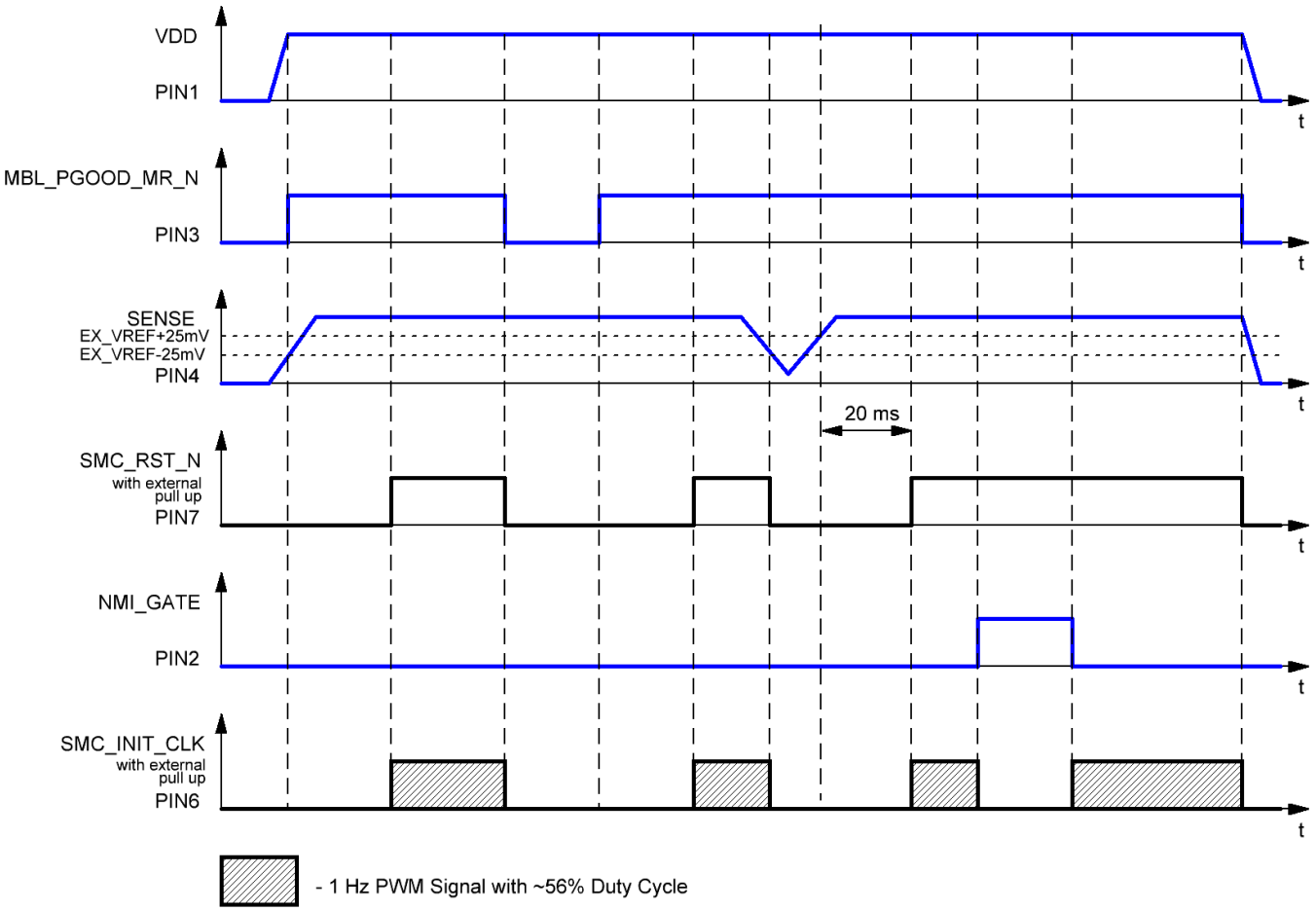
Symbol	Parameter	Condition / Note	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static inputs and outputs	--	30	--	µA
T_A	Operating temperature		-40	25	85	°C
V_{AIR}	Analog Input Voltage Range		0	--	2.2	V
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side	--	--	24	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.6	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.95	V
V_{OL}	LOW-Level Output Voltage (note 1)	Push-Pull , Open Drain Logic Level Outputs	0	--	0.4	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins;V_{IN} = VDD	-100	--	100	nA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN} = 0V	-100	--	100	nA
I_{OL}	LOW-Level Output Current (note 1)	Open Drain, 1X Driver	--	20	--	mA
V_{OFFSET}	Analog Comparator Offset Voltage	Analog Comparator 0	--	±20	--	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (note 1)	ACMP 0	--	50	--	mV
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN3	80	100	120	kΩ
T_{DLY0}	Time Delay0	Delay0	16	20	24	ms
T_{DLY2}	Time Delay2	Delay2	1.6	2.0	2.4	ms
T_{SU}	Start Up Time	After VDD reaches 2.5V	--	7	--	ms

1. Guaranteed by Design.

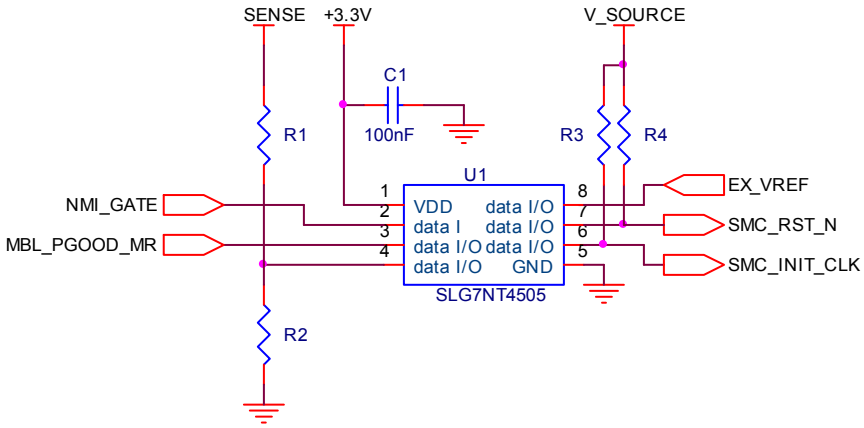
Description

This is a special oscillator with supervisor system. Three inputs are used to control the oscillator. SENSE (PIN4) controls the voltage supply of the chip. If supply voltage decreases down to the threshold set by EX_VREF (PIN8), the chip disables the oscillator and sets SMC_INICK to LOW. When the voltage is bigger than threshold set by EX_VREF is detected on the SENSE pin, SMC_RST_N (PIN7) is set to HIGH with 20 ms delay and enables the oscillator. MBL_PWRGD_MR_N (PIN3) is used for manual reset of SMC_RST_N. Use NMI_GATE (NMI_GATE) to disable the oscillator.

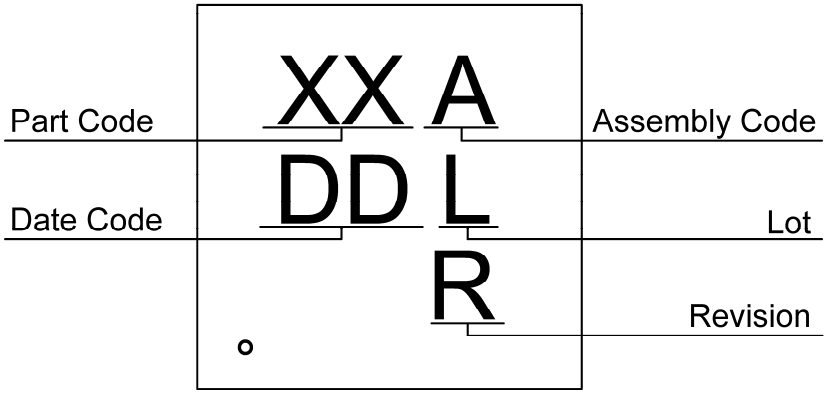
Timing Diagram



Typical Application Circuit



Package Top Marking

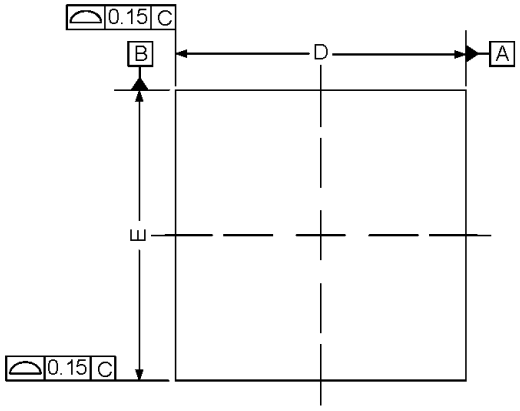


XX – Part Code Field: identifies the specific device configuration
A – Assembly Code Field: Assembly Location of the device.
DD – Date Code Field: Coded date of manufacture
L – Lot Code: Designates Lot #
R – Revision Code: Device Revision

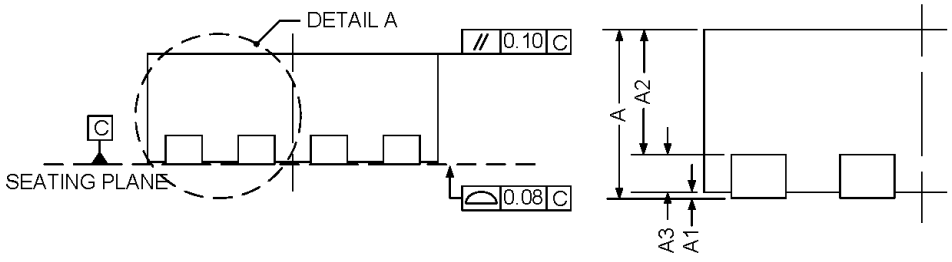
Datasheet Revision	Programming Code Number	Part Code	Revision	Date
1.0	001	YP	A	01/15/2015

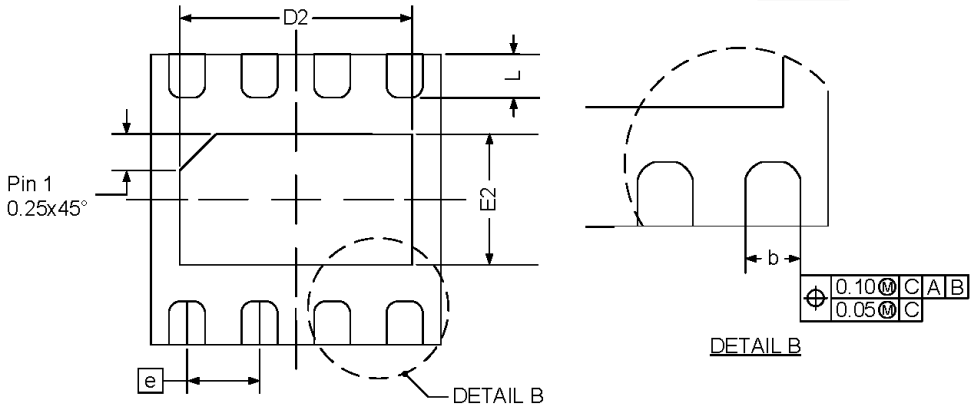
Package Drawing and Dimensions

TDFN-8 Package



Symbol	Min (mm)	NOM (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	--	0.05
A2	--	0.55	--
A3	--	0.20	--
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.50 BSC		
L	0.20	0.30	0.40



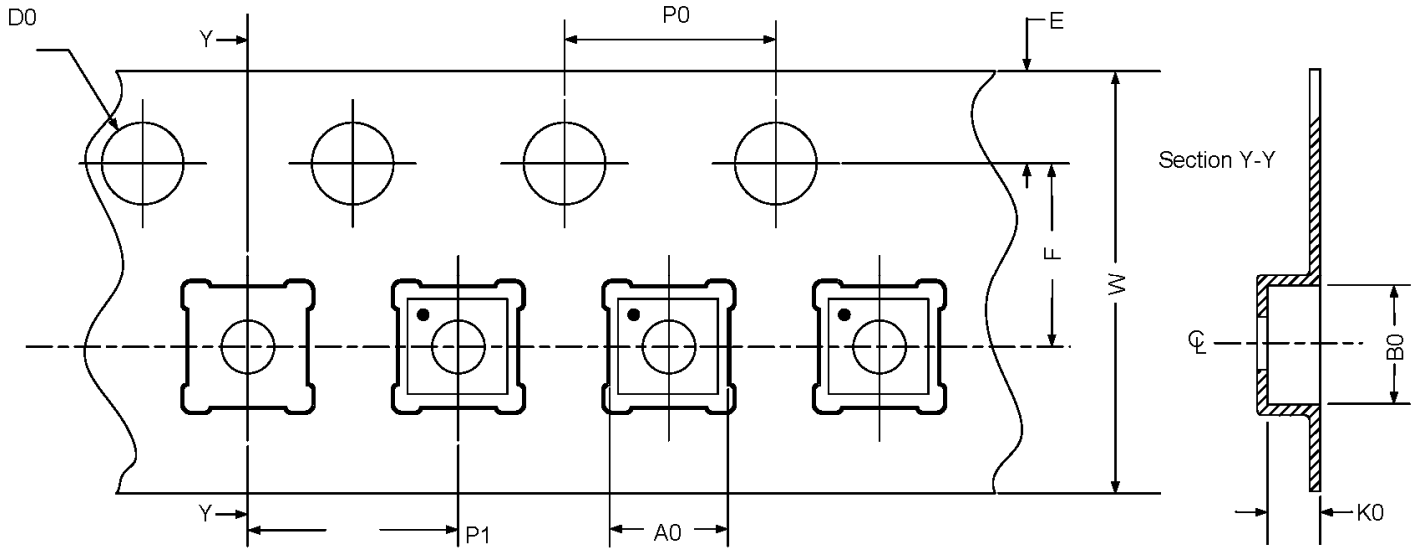


Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TDFN 8L 2x2mm Green	8	2x2x0.75	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L 2x2mm Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm^3 (nominal). More information can be found at www.jedec.org.