SM05 through SM36
TVS Diode Array

PROTECTION PRODUCTS

Description

The SM series of transient voltage suppressors (TVS) are designed to protect components which are connected to data and transmission lines from voltage surges caused by electrostatic discharge **(ESD)**, electrical fast transients **(EFT)**, and **lightning**.

TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The dual-junction common-anode design allows the user to protect one bidirectional data line or two unidirectional lines. The low profile SOT23 package allows flexibility in the design of "crowded" circuit boards.

The SM series will meet the surge requirements of IEC 61000-4-2 (Formerly IEC 801-2), Level 4, "Human Body Model" for air and contact discharge.

Features

- 300 watts peak pulse power (t_p = 8/20µs)
- Transient protection for data & power lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 12A (8/20µs)
- Protects one bidirectional line or two unidirectional lines
- Working Voltages: 5V, 12V, 15V, 24 and 36V
- Low clamping voltage
- Solid-state silicon avalanche technology

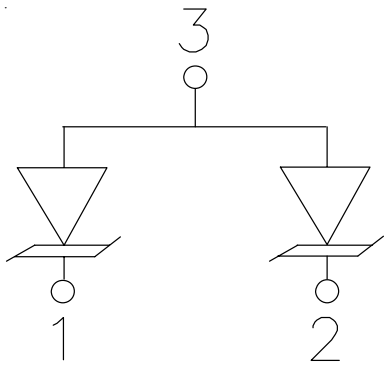
Mechanical Characteristics

- JEDEC SOT23 package
- Molding compound flammability rating: UL 94V-0
- Marking : Marking Code
- Packaging : Tape and Reel per EIA 481

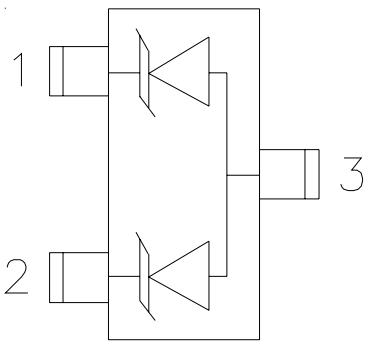
Applications

- Cellular Handsets and Accessories
- Portable Electronics
- Industrial Controls
- Set-Top Box
- Servers, Notebook, and Desktop PC

Circuit Diagram



Schematic & PIN Configuration



SOT23 (Top View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{pk}	300	Watts
Thermal Resistance, Junction to Ambient	θ_{JA}	556	°C/W
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

SM05

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C			20	µA
Clamping Voltage	V_C	I_{PP} = 1A, t_p = 8/20µs			9.8	V
Peak Pulse Current	I_{PP}	t_p = 8/20µs			17	A
Junction Capacitance	C_j	Pin 1 to 2 V_R = 0V, f = 1MHz			350	pF
Junction Capacitance	C_j	Pin 1 to 3 and Pin 2 to 3 V_R = 0V, f = 1MHz			400	pF

SM12

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	13.3			V
Reverse Leakage Current	I_R	V_{RWM} = 12V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, t_p = 8/20µs			19	V
Peak Pulse Current	I_{PP}	t_p = 8/20µs			12	A
Junction Capacitance	C_j	Pin 1 to 2 V_R = 0V, f = 1MHz			120	pF
Junction Capacitance	C_j	Pin 1 to 3 and Pin 2 to 3 V_R = 0V, f = 1MHz			150	pF

Electrical Characteristics *(Continued)*

SM15

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				15	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	16.7			V
Reverse Leakage Current	I_R	V_{RWM} = 15V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, t_p = 8/20µs			24	V
Peak Pulse Current	I_{PP}	t_p = 8/20µs			10	A
Junction Capacitance	C_j	Pin 1 to 2 V_R = 0V, f = 1MHz			75	pF
Junction Capacitance	C_j	Pin 1 to 3 and 2 to 3 V_R = 0V, f = 1MHz			100	pF

SM24

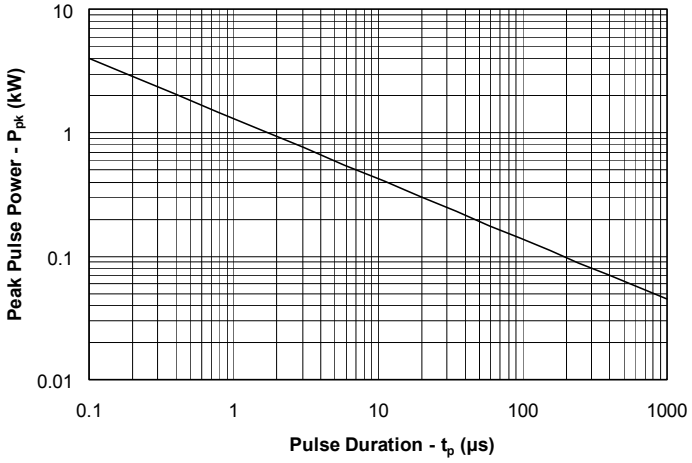
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				24	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	26.7			V
Reverse Leakage Current	I_R	V_{RWM} = 24V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, t_p = 8/20µs			43	V
Peak Pulse Current	I_{PP}	t_p = 8/20µs			5	A
Junction Capacitance	C_j	Pin 1 to 2 V_R = 0V, f = 1MHz			50	pF
Junction Capacitance	C_j	Pin 1 to 3 and 2 to 3 V_R = 0V, f = 1MHz			60	pF

SM36

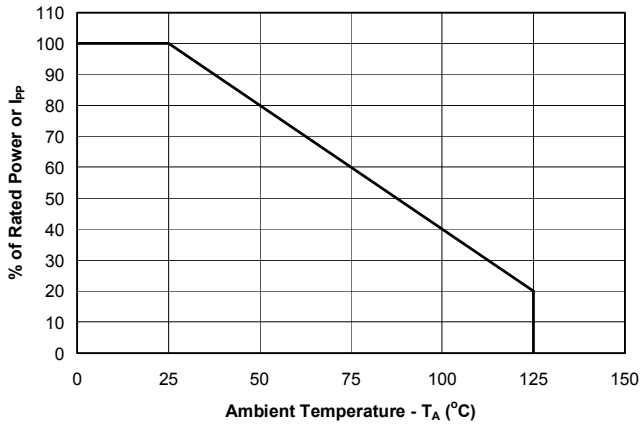
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				36	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	40			V
Reverse Leakage Current	I_R	V_{RWM} = 36V, T=25°C			1	µA
Clamping Voltage	V_C	I_{PP} = 1A, t_p = 8/20µs			60	V
Peak Pulse Current	I_{PP}	t_p = 8/20µs			4	A
Junction Capacitance	C_j	Pin 1 to 2 V_R = 0V, f = 1MHz			40	pF
Junction Capacitance	C_j	Pin 1 to 3 and 2 to 3 V_R = 0V, f = 1MHz			45	pF

Typical Characteristics

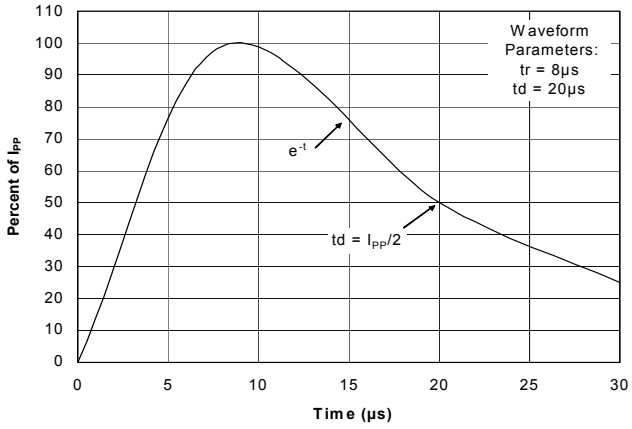
Non-Repetitive Peak Pulse Power vs. Pulse Time



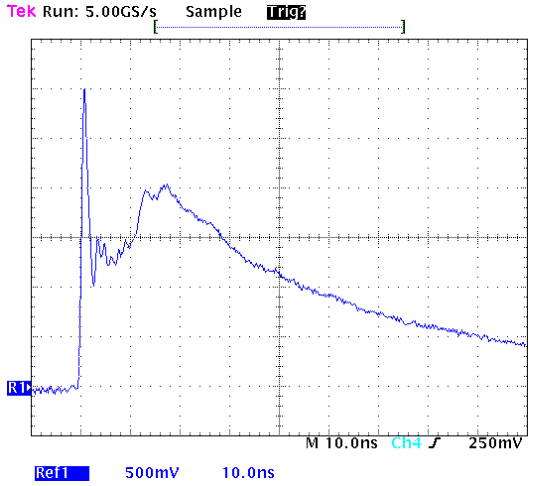
Power Derating Curve



Pulse Waveform



ESD Pulse Waveform (Per IEC 61000-4-2)



IEC 61000-4-2 Discharge Parameters

Level	First Peak Current (A)	Peak Current at 30 ns (A)	Peak Current at 60 ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

Applications Information

Device Connection Options

The SM series is designed to protect one bidirectional or two unidirectional data or I/O lines operating at 5 to 36 volts. Connection options are as follows:

- **Bidirectional:** Pin 1 is connected to the data line and pin 2 is connected to ground (Since the device is symmetrical, these connections may be reversed). The ground connection should be made directly to a ground plane. The path length should be kept as short as possible to minimize parasitic inductance. Pin 3 is not connected.
- **Unidirectional:** Data lines are connected to pin 1 and pin 2. Pin 3 is connected to ground. For best results, this pin should be connected directly to a ground plane on the board. The path length should be kept as short as possible to minimize parasitic inductance.

Circuit Board Layout Recommendations for Suppression of ESD.

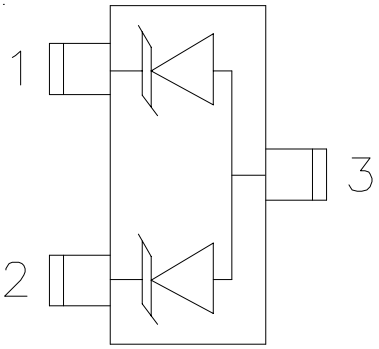
Good circuit board layout is critical for the suppression of fast rise-time transients such as ESD. The following guidelines are recommended (Refer to application note SI99-01 for more detailed information):

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

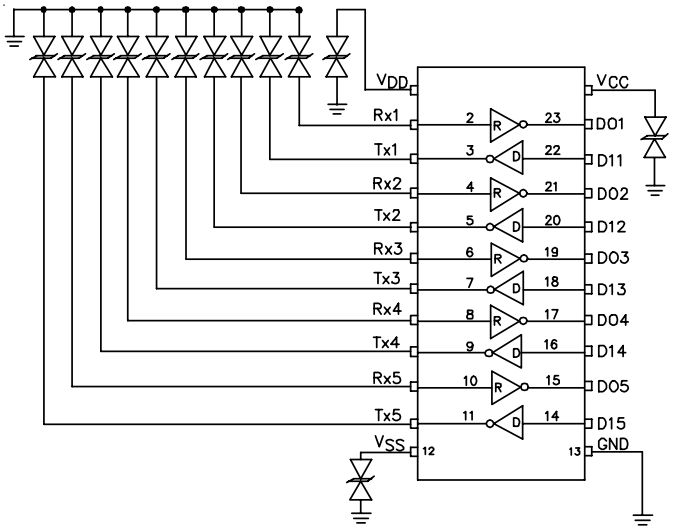
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

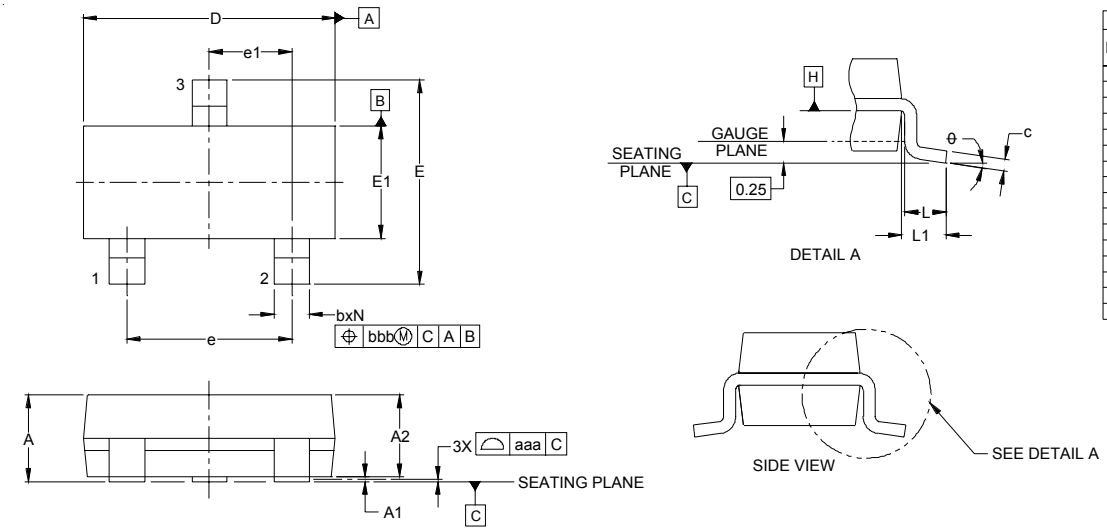
Device Schematic & Pin Configuration



RS-232 Transceiver Protection Example



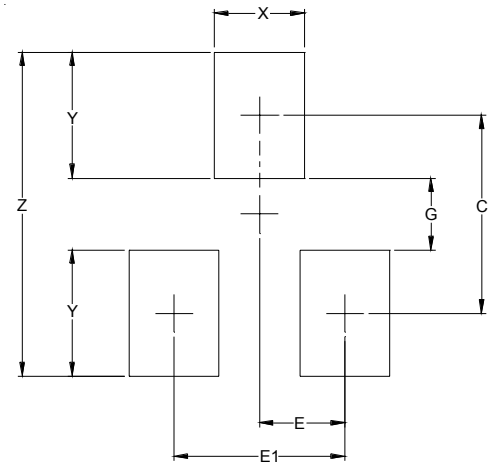
Outline Drawing - SOT23



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.035	-	.044	0.89	-	1.12
A1	.000	-	.004	0.01	-	0.10
A2	.035	.037	.040	0.88	0.95	1.02
b	.012	-	.020	0.30	-	0.51
c	.003	-	.007	0.08	-	0.18
D	.110	.114	.120	2.80	2.90	3.04
E	.082	.093	.104	2.10	2.37	2.64
E1	.047	.051	.055	1.20	1.30	1.40
e	.075			1.90 BSC		
e1	.037			0.95 BSC		
L	.015	.020	.024	0.40	0.50	0.60
L1	.022			(0.55)		
N	3			3		
θ	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.008			0.20		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SOT23



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.087)	(2.20)
E	.037	0.95
E1	.075	1.90
G	.031	0.80
X	.039	1.00
Y	.055	1.40
Z	.141	3.60

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A.