

PROTECTION PRODUCTS

Description

The SMDAxxC-5 series of transient voltage suppressors are designed to protect components which are connected to data and transmission lines from voltage surges caused by electrostatic discharge (ESD), electrical fast transients (EFT), and lightning.

TVS diodes are characterized by their high surge capability, low operating and clamping voltages, and fast response time. This makes them ideal for use as board level protection of sensitive semiconductor components. The SMDAxxC-5 is designed to provide transient suppression on multiple data lines and I/O ports. The low profile SO-8 design allows the user to protect up to five data and I/O lines with one package.

The SMDAxxC-5 TVS diode array will meet the surge requirements of IEC 61000-4-2 (Formerly IEC 801-2), Level 4, "Human Body Model" for air and contact discharge.

Features

- ◆ Transient protection for data lines to **IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)**
IEC 61000-4-4 (EFT) 40A (5/50ns)
IEC 61000-4-5 (Lightning) 12A (8/20 μs)
- ◆ Small SO-8 surface mount package
- ◆ Protects five I/O lines
- ◆ Working voltages: 5V, 12V, 15V and 24V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages
- ◆ Solid-state silicon avalanche technology

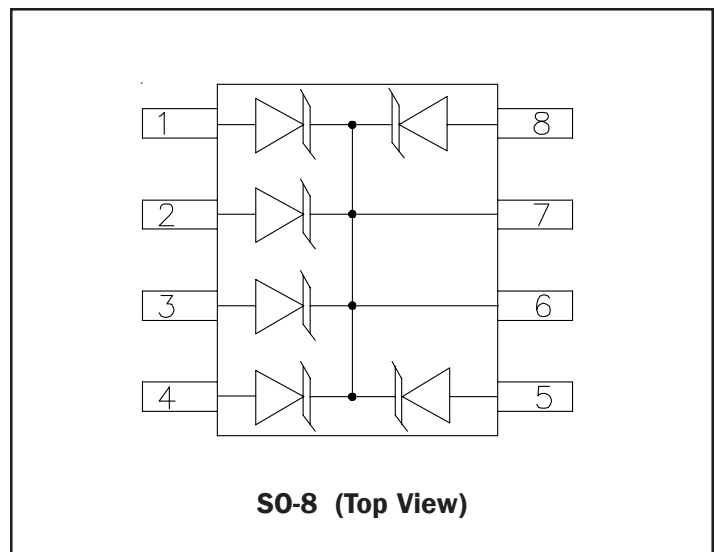
Mechanical Characteristics

- ◆ JEDEC SO-8 package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Part number, date code, logo
- ◆ Packaging : Tube or Tape and Reel per EIA 481

Applications

- ◆ RS-232 and RS-422 Data Lines
- ◆ Microprocessor Based Equipment
- ◆ LAN/WAN Equipment
- ◆ Notebooks, Desktops, and Servers
- ◆ Instrumentation
- ◆ Peripherals
- ◆ Set Top Box
- ◆ Serial and Parallel Ports

Schematic and PIN Configuration



PROTECTION PRODUCTS
Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P _{pk}	300	Watts
Lead Soldering Temperature	T _L	260 (10 sec.)	°C
Operating Temperature	T _J	-55 to +125	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics

SMDA05C-5						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V _{RWM}				5	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA	6			V
Reverse Leakage Current	I _R	V _{RWM} = 5V, T=25°C			20	μA
Clamping Voltage	V _C	I _{pp} = 1A, tp = 8/20μs			9.8	V
Maximum Peak Pulse Current	I _{pp}	tp = 8/20μs			17	A
Junction Capacitance	C _J	Between I/O Pins and Ground V _R = 0V, f = 1MHz			350	pF

SMDA12C-5						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V _{RWM}				12	V
Reverse Breakdown Voltage	V _{BR}	I _t = 1mA	16.7			V
Reverse Leakage Current	I _R	V _{RWM} = 12V, T=25°C			1	μA
Clamping Voltage	V _C	I _{pp} = 1A, tp = 8/20μs			19	V
Maximum Peak Pulse Current	I _{pp}	tp = 8/20μs			12	A
Junction Capacitance	C _J	Between I/O Pins and Ground V _R = 0V, f = 1MHz			120	pF

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Electrical Characteristics

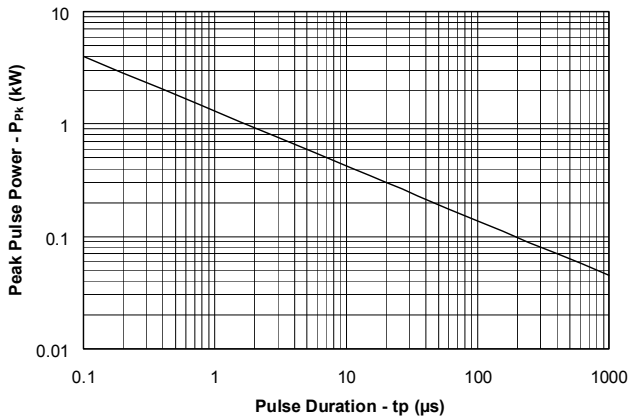
SMDA15C-5						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				15	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	16.7			V
Reverse Leakage Current	I_R	$V_{RWM} = 15V, T=25^{\circ}C$			1	μA
Clamping Voltage	V_C	$I_{PP} = 1A, t_p = 8/20\mu s$			24	V
Maximum Peak Pulse Current	I_{PP}	$t_p = 8/20\mu s$			10	A
Junction Capacitance	C_J	Between I/O Pins and Ground $V_R = 0V, f = 1MHz$			75	pF

SMDA24C-5						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				24	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	26.7			V
Reverse Leakage Current	I_R	$V_{RWM} = 24V, T=25^{\circ}C$			1	μA
Clamping Voltage	V_C	$I_{PP} = 1A, t_p = 8/20\mu s$			43	V
Maximum Peak Pulse Current	I_{PP}	$t_p = 8/20\mu s$			5	A
Junction Capacitance	C_J	Between I/O Pins and Ground $V_R = 0V, f = 1MHz$			50	pF

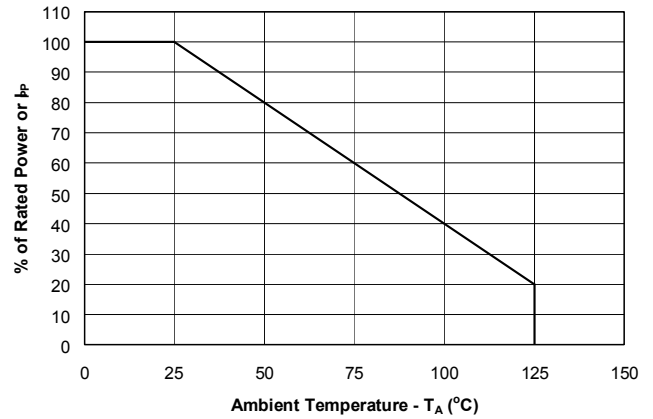
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Typical Characteristics

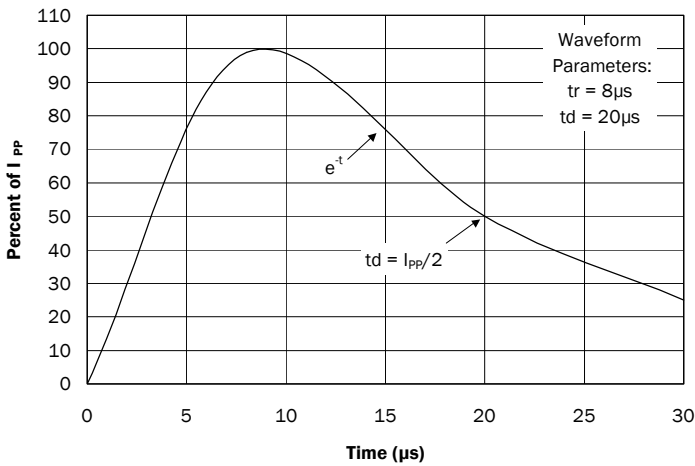
Non-Repetitive Peak Pulse Power vs. Pulse Time



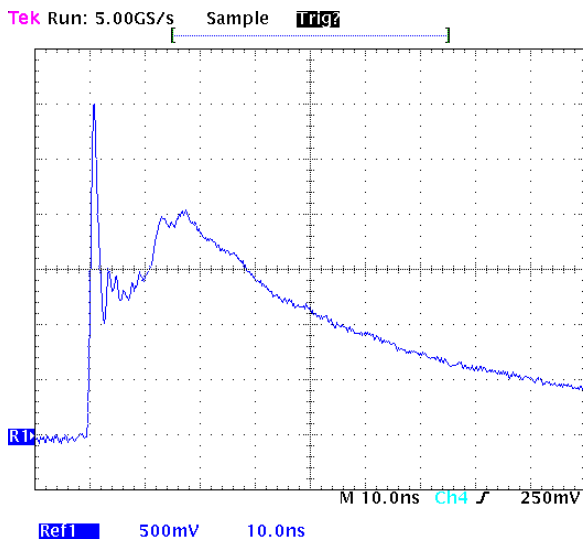
Power Derating Curve



Pulse Waveform



ESD Pulse Waveform (Per IEC 61000-4-2)



IEC 61000-4-2 Discharge Parameters

Level	First Peak Current (A)	Peak Current at 30 ns (A)	Peak Current at 60 ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

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Applications Information

Device Connection for Protection of Five Data Lines

The SMDAxxC-5 is designed to protect up to 5 data or I/O lines. They are bidirectional devices and may be used on lines where the signal polarities are above and below ground.

The SMDAxxC-5 TVS arrays employ a monolithic structure. Therefore, the working voltage (V_{RWM}) and breakdown voltage (V_{BR}) specifications apply to the differential voltage between any two data line pins. For example, the SMDA24C-5 is designed for a maximum voltage excursion of $\pm 12V$ between any two data lines. The device is connected as follows:

- Pins 1, 2, 3, 4, and 5 are connected to the lines that are to be protected. Pin 8 is connected to ground. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces. Pins 6 and 7 are not connected.

Circuit Board Layout Recommendations for Suppression of ESD.

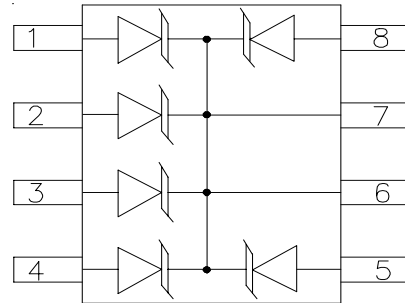
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

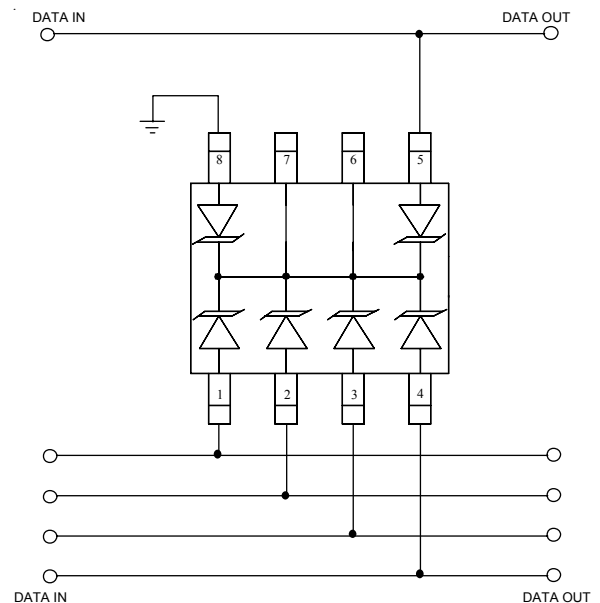
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both

Circuit Diagram



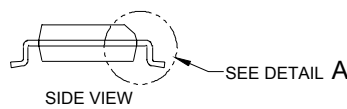
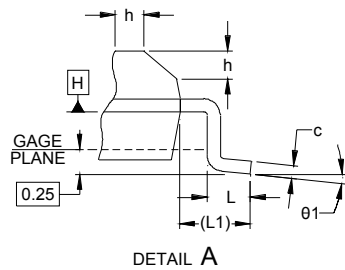
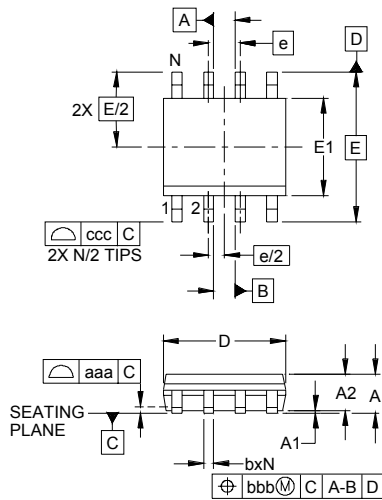
Connection Diagram



lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

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Outline Drawing - S0-8

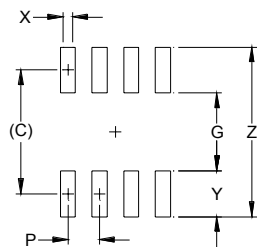


DIM	INCHES		MILLIMETERS			
	MIN	NOM	MIN	MAX		
A	.053	-.069	1.35	- 1.75		
A1	.004	-.010	0.10	- 0.25		
A2	.049	-.065	1.25	- 1.65		
b	.012	-.020	0.31	- 0.51		
c	.007	-.010	0.17	- 0.25		
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC		6.00 BSC			
e	.050 BSC		1.27 BSC			
h	.010	-.020	0.25	- 0.50		
L	.016	.028	.041	0.40	0.72	1.04
L1	(0.041)		(1.04)			
N	8		8			
theta 1	0°	- 8°	0°	- 8°		
aaa	.004		0.10			
bbb	.010		0.25			
ccc	.008		0.20			

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **+H-**.
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - S0-8



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.