IFN112 N-Channel JFET

Features

- InterFET N0132H Geometry
- Low Noise: 1.5 nV/√Hz Typical
- High Gain: 12mS Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

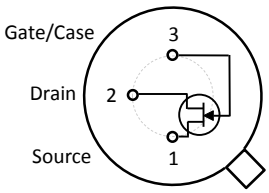
Applications

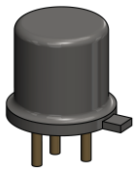
- Low-Noise, High Gain
- Replacement for Japanese 2SK112

Description

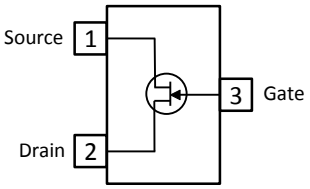
The -50V InterFET IFN112 is a low noise high gain replacement for the Japanese 2SK112 JFET. Gate leakages are typically less than 50pA at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications.

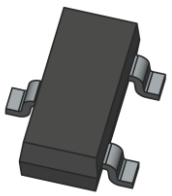
TO-18 Bottom View



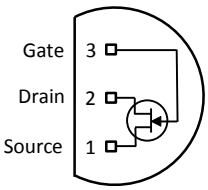


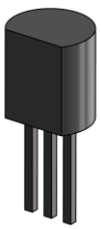
SOT23 Top View





TO-92 Bottom View





Product Summary

Parameters		IFN112 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-50	V
I_{DSS}	Drain to Source Saturation Current	1.2	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.25	V
G_{FS}	Forward Transconductance	7	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN112	Through-Hole	TO-18	Bulk
PN112	Through-Hole	TO-92	Bulk
SMP112	Surface Mount	SOT23	Bulk
SMP112TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
IFN112COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFN112CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-50	V
I_{FG}	Continuous Forward Gate Current	10	mA
P_D	Continuous Device Power Dissipation	360	mW
P	Power Derating	2.88	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

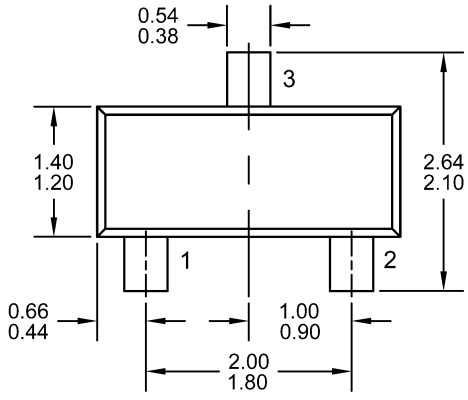
Parameters		Conditions	IFN112		Unit
			Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-50		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -30V, V_{DS} = 0V		-0.1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 15V, I_D = 100nA	-0.25	-1.2	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 15V (Pulsed)	1.2	9	mA

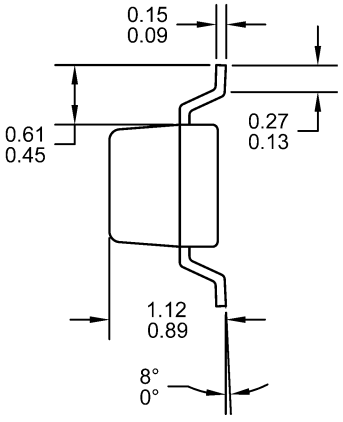
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

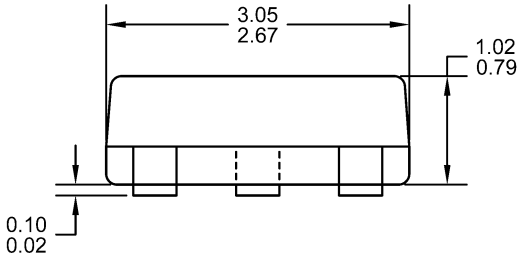
Parameters		Conditions	IFN112		Unit
			Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = 15V, V_{GS} = 0V, f = 1kHz	7	34	mS
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	12 (typ)		pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	3 (typ)		pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 10V, I_D = 5mA, f = 1kHz	1.5 (typ)		nV/√Hz

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

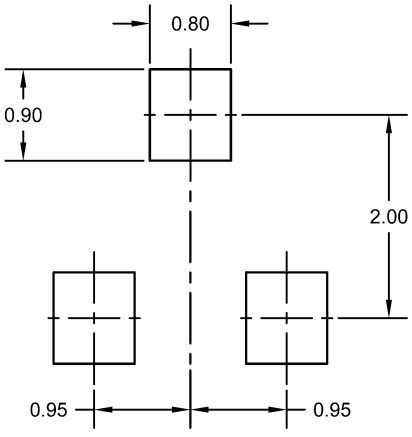






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

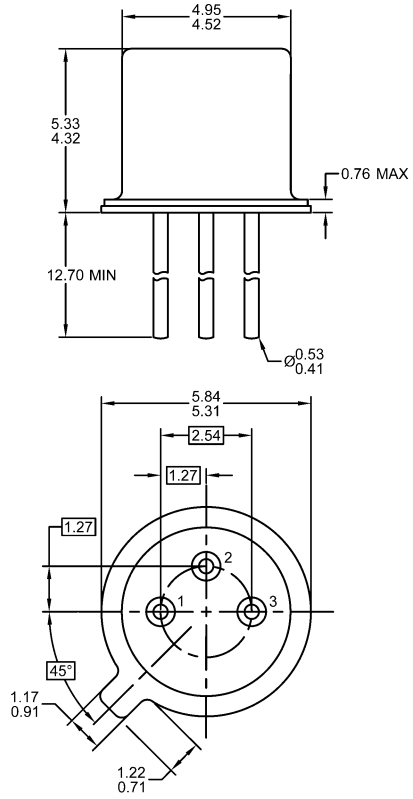
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

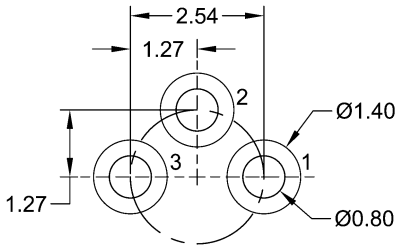
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.