

DATA SHEET

SMP1331-087LF: 45 W Surface Mount Series Connected PIN Diode

Applications

- Low-loss, high-power switches
- Low-distortion attenuators

Features

- High RF power handling: 45 W
- Low thermal resistance: 26 °C/W
- Low series resistance: 0.50 Ω typical @ 100 mA
- Low total capacitance: 0.35 pF maximum @ 30 V
- Small QFN (2 × 2 mm) package (MSL1, 260 °C per JEDEC J-STD-020)



Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

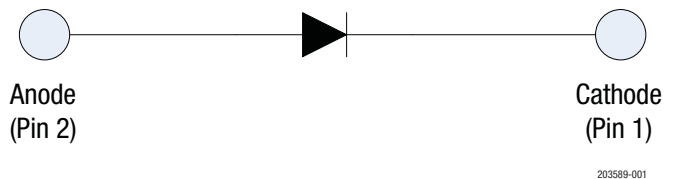


Figure 1. SMP1331-087LF Block Diagram

Description

The SMP1331-087LF is a surface mountable, low-capacitance silicon PIN diode designed as a series connected PIN diode for high-power, high-volume switch and attenuator applications from 10 MHz to beyond 6 GHz.

Typical resistance at 100 mA is 0.50 Ω and maximum capacitance at 30 V is 0.35 pF. The combination of low capacitance, low parasitic inductance, and nominal 30 μm I-region width, makes the SMP1331-087LF useful in large signal switches and attenuator applications.

The device has a 0.75 W dissipation power rating, which makes it capable of handling up to 45 W @ 85 °C Continuous Wave (CW) in a series-connected transmit/receive (T/R) switch.

Design information for high-power switches may be found in the Skyworks Application Note, *Design With PIN Diodes* (document number 200312).

A block diagram of the SMP1331-087LF is shown in Figure 1.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SMP1331-087LF are provided in Table 1. Electrical specifications are provided in Table 2. Typical DC performance characteristics of the SMP1331-087LF are illustrated in Figures 2, 3, and 4.

The SMP1331-087LF Evaluation Board is used to test the performance of the SMP1331-087LF PIN Diode. Figure 5 shows a

bias schematic, and Table 3 lists the Evaluation Board Bill of Materials. Typical RF performance of the SMP1331-087LF using the schematic shown in Figure 5 is summarized in Table 4 and illustrated in Figures 6, 7, and 8.

An assembly drawing for the Evaluation Board is shown in Figure 9. The layer detail physical characteristics are provided in Figure 10.

Table 1. SMP1331-087LF Absolute Maximum Ratings¹

Parameter	Symbol	Minimum	Maximum	Units
Forward current	I _F		200	mA
Reverse voltage	V _R		200	V
Dissipated power @ 85 °C	P _D		0.75	W
Peak pulse power dissipation @ 85 °C (10% duty cycle)			7.5	W
Operating temperature	T _A	-55	+85	°C
Storage temperature	T _{STG}	-55	+200	°C
Junction temperature	T _J	-55	+175	°C
Electrostatic discharge:	ESD			
Charged-Device Model (CDM), Class 4			1100	V
Human Body Model (HBM), Class 3A			5000	V
Machine Model (MM), Class C			400	V

¹ Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD HANDLING: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 2. SMP1331-087LF Electrical Specifications¹
(T_A = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Forward voltage	V _F	I _F = 10 mA		0.80		V
Reverse leakage current	I _R	V _R = 200 V			10	μA
Series resistance	R _{S1}	I _F = 1 mA, f = 100 MHz		9.0	14.5	Ω
	R _{S10}	I _F = 10 mA, f = 100 MHz		1.7		Ω
	R _{S100}	I _F = 100 mA, f = 100 MHz		0.50		Ω
Total capacitance	C _{T30}	V _R = 30 V, f = 1 MHz		0.26	0.35	pF
Series inductance	L _S			0.37		nH
Minority carrier lifetime	t _L	I _F = 10 mA		600		ns
I region width	W			30		μm
Thermal resistance (Note 2)	θ _{JC}	Junction-to-case		26		°C/W
Peak thermal resistance	θ _P	Single, 1 μs pulse width, junction-to-case (10% duty cycle)		2.6		°C/W

¹ Performance is guaranteed only under the conditions listed in this table.

² Assume a thermal resistance of 90 °C/W for the junction-to-bottom of the circuit board.

Typical DC Performance Characteristics
 (T_A = 25 °C, Unless Otherwise Noted)

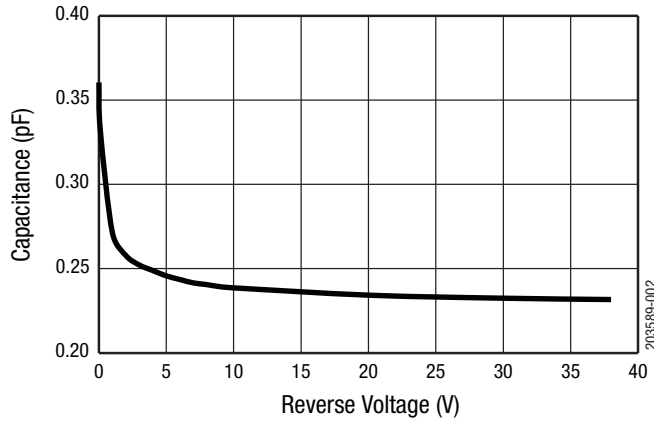


Figure 2. Capacitance vs Reverse Voltage

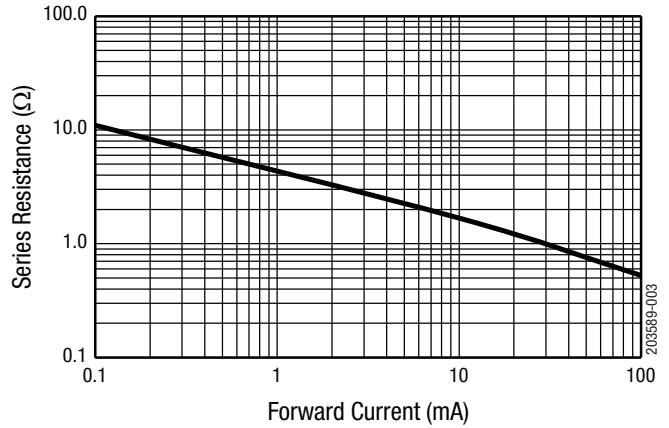


Figure 3. Series Resistance vs Forward Current

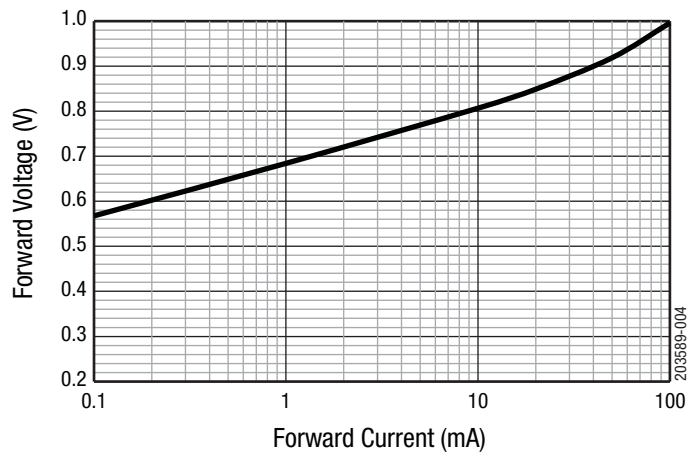


Figure 4. Forward Voltage vs Forward Current

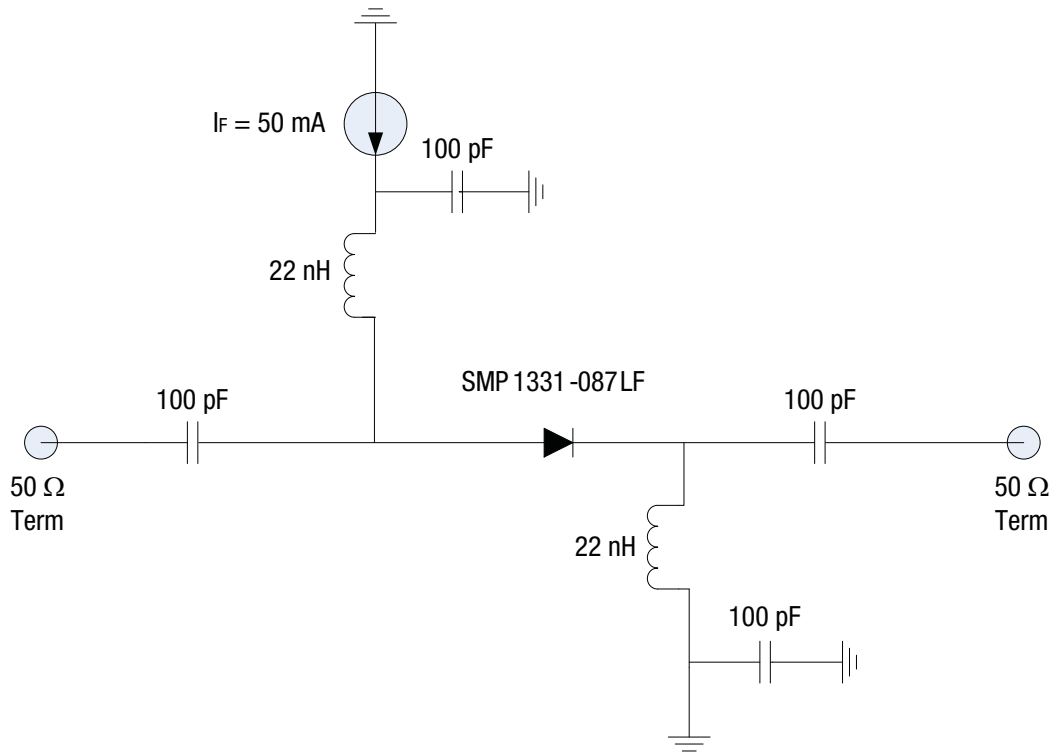


Figure 5. SMP1331-087LF Bias Schematic

Table 3. Evaluation Board Bill of Materials for EN33-D515-01_V3

Component	Value	Size	QTY	Manufacturer	Mfg. Part Number	Characteristics
C	100 pF	0402	4	Murata	GRM1555C1H101JZ01	5% COG 50 V
L	22 nH	0402	2	Murata	HK100522NJ-T	5%

Table 4. Typical RF Performance @ 25 °C, f = 2.6 GHz, If = 50 mA

Parameter	Typical	Units
Insertion loss	0.35	dB
Return loss	16	dB
Isolation	12.2	dB
Max power (If = 100 mA)	+47	dBm

Typical RF Performance Characteristics

(TOP = +25 °C, Characteristic Impedance [Z₀] = 50 Ω, EVB Optimized with Bias Circuit, Unless Otherwise Noted)

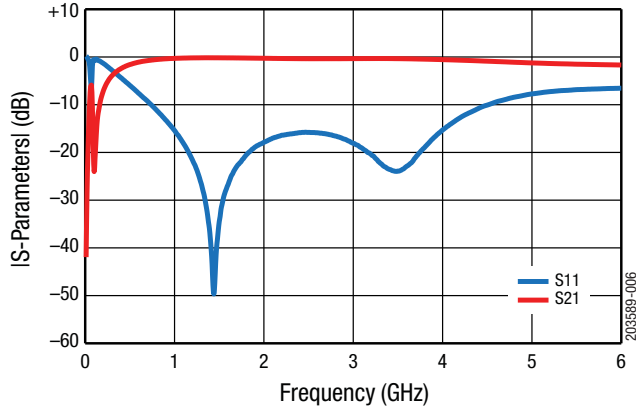


Figure 6. S-Parameter Magnitude vs Frequency (I_F = 50 mA)

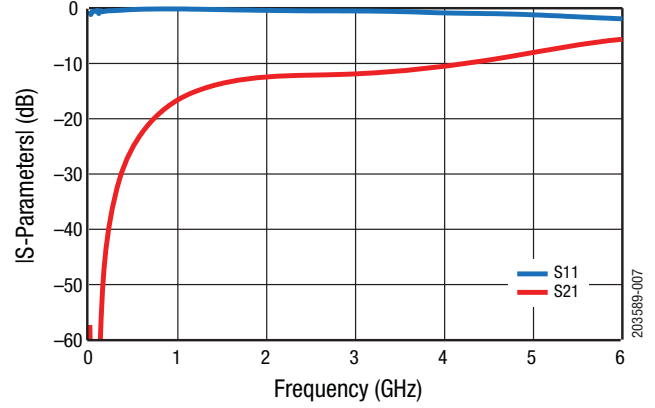


Figure 7. S-Parameter Magnitude vs Frequency (V_{REV} = -30 V)

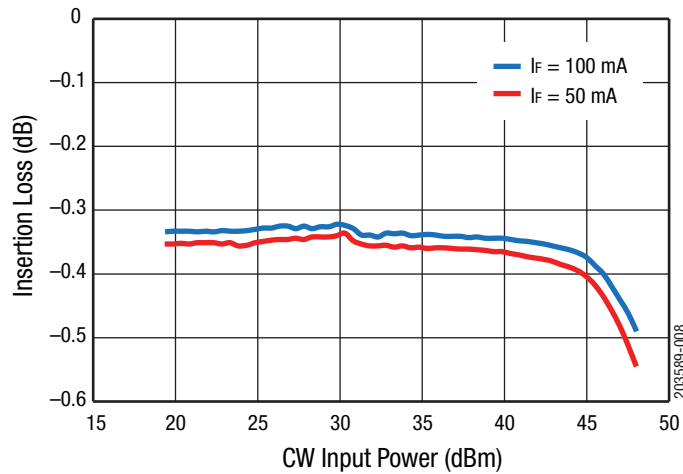


Figure 8. Insertion Loss vs CW Input Power (f = 2.6 GHz)

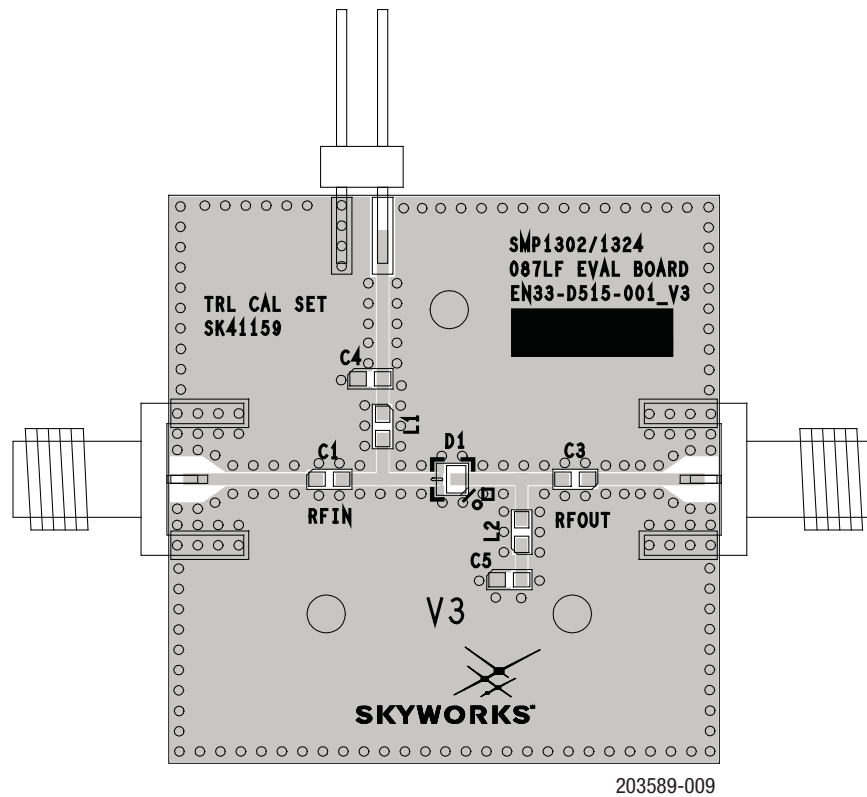


Figure 9. SMP1331-087LF Evaluation Board

Cross Section	Name	Thickness (in)	Material
	Top Solder Mask		
	L1	(0.0028)	Cu foil
	Laminate	0.012 ± 0.0006	Rogers R04003C Core
	L2	(0.0014)	Cu foil
	Laminate	(Note 1)	FR4 Prepreg
	L3	(0.0014)	Cu foil
	Laminate	0.010 ± 0.0006	FR4 Core
	L4	(0.0028)	Cu foil
	Bottom Solder Mask		

Note 1: Adjust this thickness to meet total thickness goal of 0.062 ± 0.005 inch.

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Figure 10. Board Layer Detail Physical Characteristics

Package Dimensions

The PCB layout footprint for the SMP1331-087LF is provided in Figure 11. Typical part markings are shown in Figure 12. Package dimensions for the SMP1331-087LF are provided in Figure 13, and tape and reel dimensions are provided in Figure 14.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SMP1331-087LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

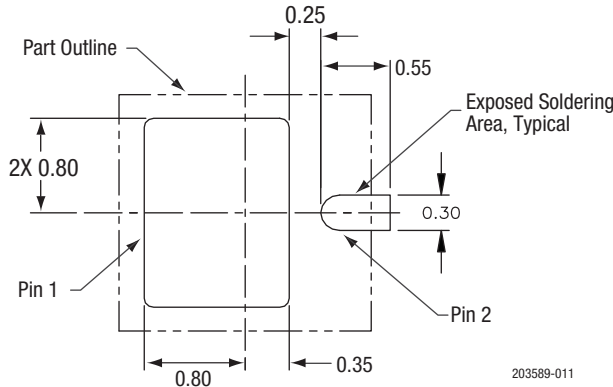


Figure 11. SMP1331-087LF PCB Layout Footprint (Top View)

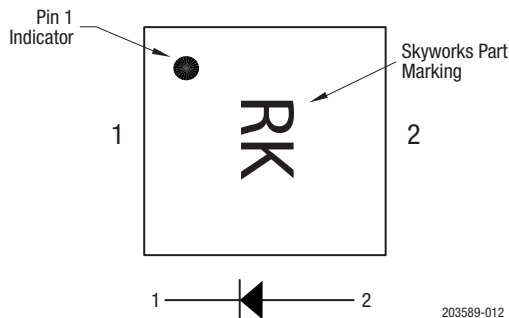
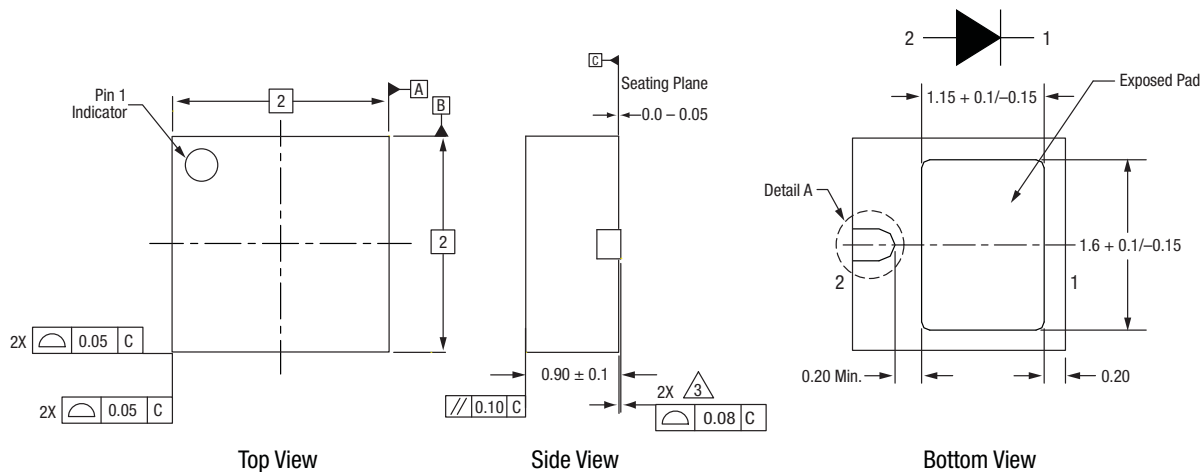
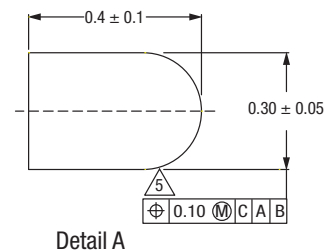


Figure 12. Typical Part Markings (Top View)



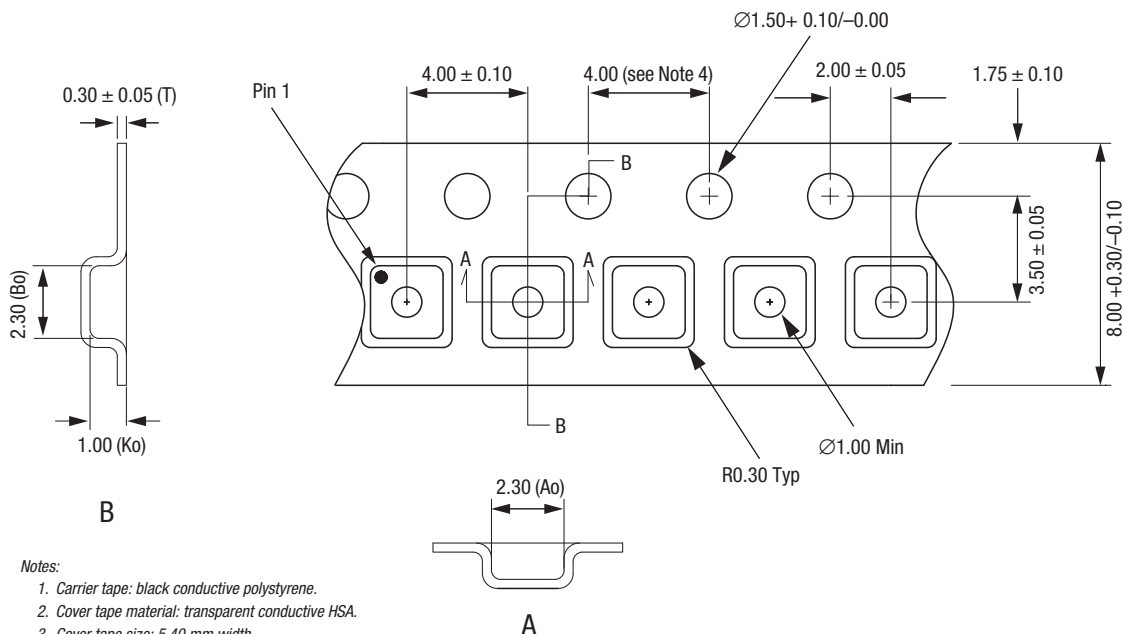
Notes:

1. All measurements are in millimeters.
2. Dimensions and tolerances according to ASME Y14.5M-1994.
3. Coplanarity applies to the exposed heat sink slug as well as the terminals..
4. Dimension applies to metalized terminal and is measured between 0.10 mm and 0.30 mm from terminal tip.



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Figure 13. SMP1331-087LF Package Dimensions



Notes:

1. Carrier tape: black conductive polystyrene.
2. Cover tape material: transparent conductive HSA.
3. Cover tape size: 5.40 mm width.
4. Ten sprocket hole pitch cumulative tolerance = ±0.20 mm.
5. ESD surface resistivity is $\leq 1 \times 10^8$ Ohms/square per EIA, JEDEC tape and reel specification.
6. Ao and Bo measurement point to be 0.30 mm from bottom pocket.
7. All measurements are in millimeters.

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Figure 14. SMP1331-087LF Tape and Reel Dimensions