IFN152 N-Channel JFET

Features

- InterFET N0132L Geometry
- Low Noise: 1.0 nV/√Hz Typical
- High Gain: 30mS Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

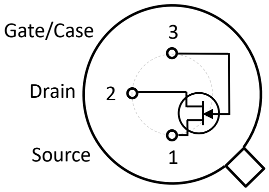
Applications

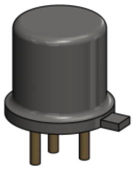
- Low-Noise, High Gain
- Replacement for Japanese 2SK152

Description

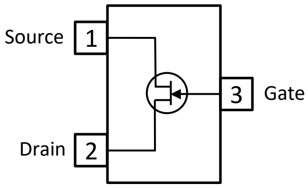
The -20V InterFET IFN152 is a low noise high gain replacement for the Japanese 2SK152 JFET. Gate leakages are typically less than 50pA at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications.

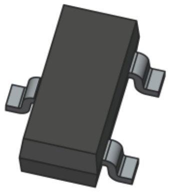
TO-18 Bottom View



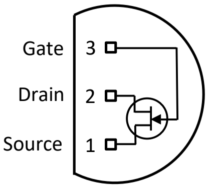


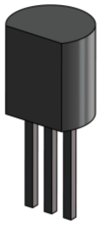
SOT23 Top View





TO-92 Bottom View





Product Summary

Parameters		IFN152 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-20	V
I_{DSS}	Drain to Source Saturation Current	5	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.5	V
G_{FS}	Forward Transconductance	30 (typ)	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFN152	Through-Hole	TO-18	Bulk
PN152	Through-Hole	TO-92	Bulk
SMP152	Surface Mount	SOT23	Bulk
SMP152TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
IFN152COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFN152CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG}	Continuous Forward Gate Current	10	mA
P_D	Continuous Device Power Dissipation	300	mW
P	Power Derating	2.8	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

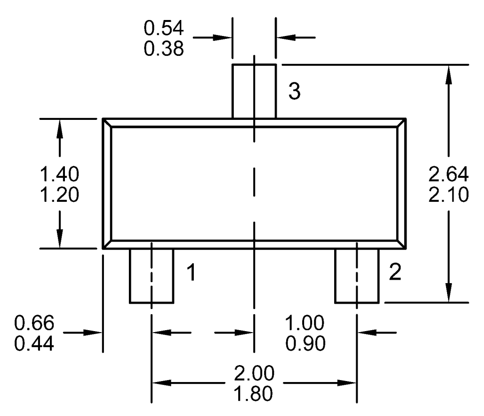
Parameters		Conditions	IFN152		Unit
			Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-20		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -10V, V_{DS} = 0V		1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = -10V, I_D = 100nA	-0.5	-2	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = -10V (Pulsed)	5	20	mA

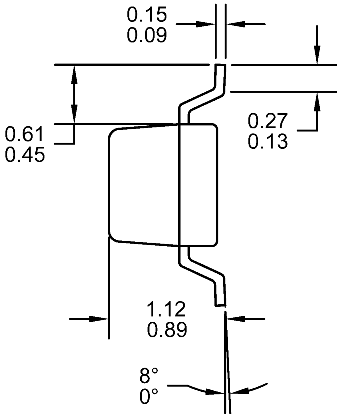
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

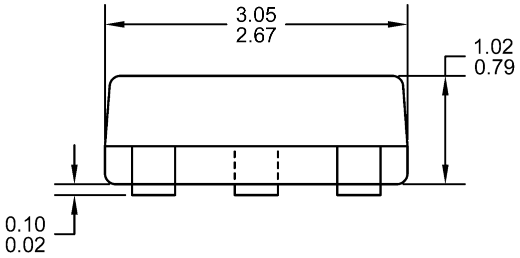
Parameters		Conditions	IFN152	Unit
			Typ	
G_{FS}	Forward Transconductance	V_{DS} = -10V, V_{GS} = 0V, f = 1kHz	30	mS
C_{iss}	Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz	15	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 10V, I_D = 0A, f = 1MHz	4	pF

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

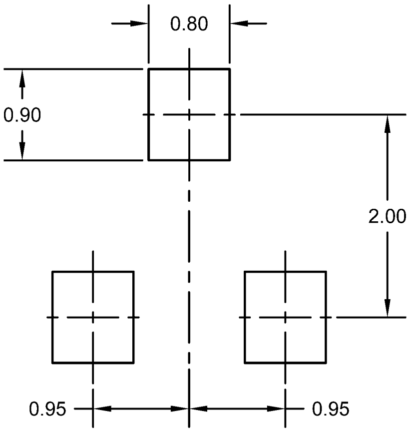






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

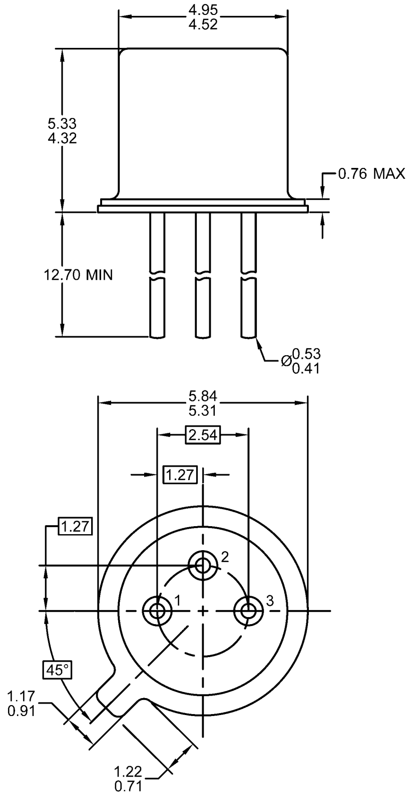
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

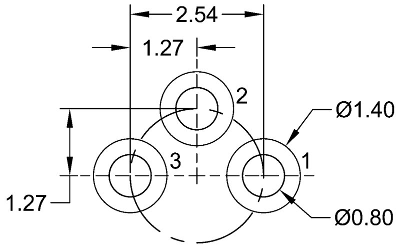
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.