2N3330, 2N3331 P-Channel JFET

Features

- InterFET P0032F Geometry
- Typical Noise: 10 nV/√Hz
- Low Ciss: 3.2pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

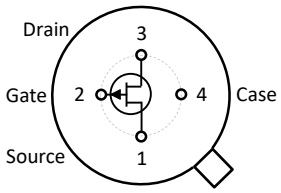
Applications

- Choppers
- Data Switches
- Commutators

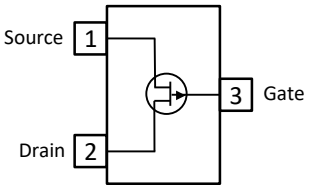
Description

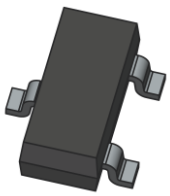
The 20V InterFET 2N3330 and 2N3331 are targeted for data switches and chopper designs. Gate leakages are typically less than 1nA at room temperatures. The TO-72 package is hermetically sealed and suitable for military applications.

TO-72 Bottom View

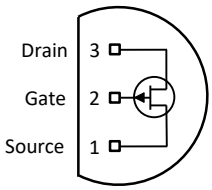


SOT23 Top View





TO-92 Bottom View



Product Summary

Parameters		2N3330 Min	2N3331 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	20	20	V
I_{DSS}	Drain to Source Saturation Current	-2	-5	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	0.3	0.3	V
G_{FS}	Forward Transconductance	1500	2000	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N3330; 2N3331	Through-Hole	TO-72	Bulk
PN3330; PN3331	Through-Hole	TO-92	Bulk
SMP3330; SMP3331	Surface Mount	SOT23	Bulk
SMP3330TR; SMP3331TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N3330COT; 2N3331COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N3330CFT; 2N3331CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	20	V
I_{FG}	Continuous Forward Gate Current	10	mA
P_D	Continuous Device Power Dissipation	300	mW
P	Power Derating	2	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

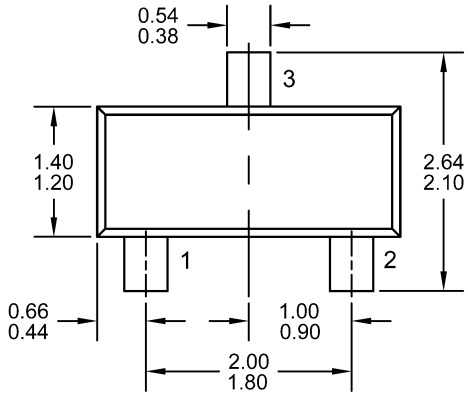
Parameters		Conditions	2N3330		2N3331		Unit
			Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = 10µA	20		20		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = 10V, V_{DS} = 0V		10		10	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = -15V, I_D = -10nA	0.3	6	0.3	8	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = -10V (Pulsed)	-2	-6	-5	-15	mA

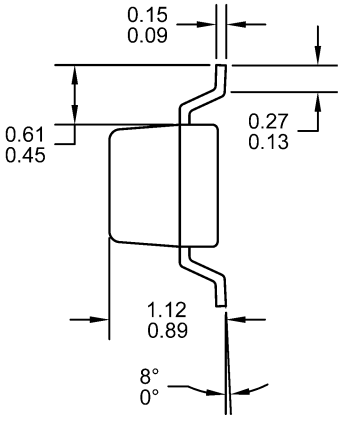
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

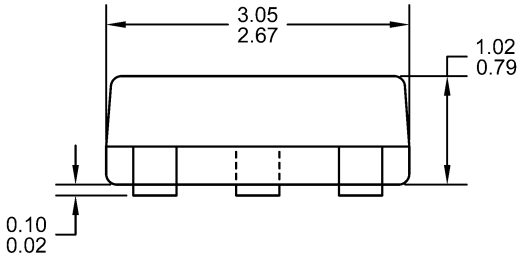
Parameters		Conditions	2N3330		2N3331		Unit
			Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = -10V, V_{GS} = 0V, f = 1kHz	1500	3000	2000	4000	µS
C_{iss}	Input Capacitance	V_{DS} = -10V, V_{GS} = 1V, f = 1MHz		20		20	pF
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{GS} = 0V, I_D = 0mA, f = 1MHz		800		600	Ω

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

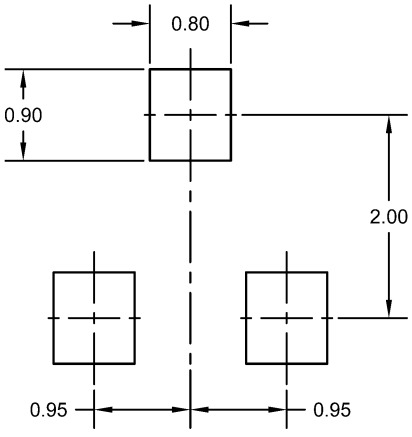






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

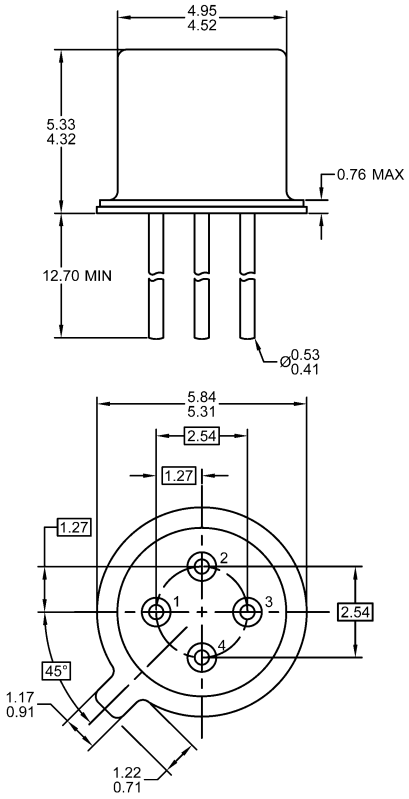
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

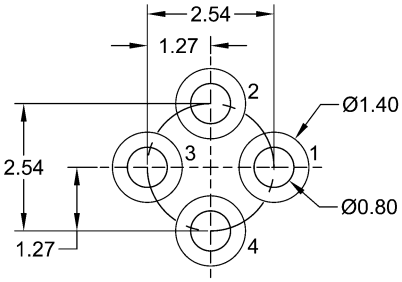
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.