2N3970, 2N3971, 2N3972 N-Channel JFET

Features

- InterFET N0132S Geometry
- Low Noise: 1.2 nV/√Hz Typical
- Fast Switching
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

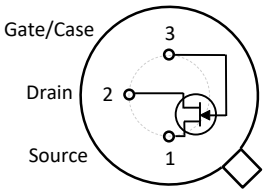
Applications

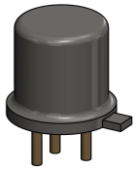
- Low $R_{DS(ON)}$
- Low Leakage
- Fast Switching

Description

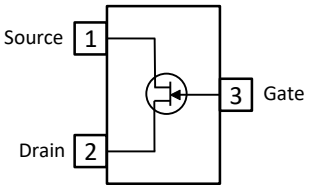
The -40V InterFET 2N3970, 2N3971, and 2N3972 JFET's are targeted for very low noise switching applications for mid to high frequency designs. Gate leakages are typically 50pA at room temperatures. The 2N3972 has a cutoff voltage of less than 3.0V ideal for low-level power supplies. The TO-18 package is hermetically sealed and suitable for military applications.

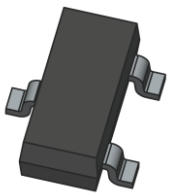
TO-18 Bottom View



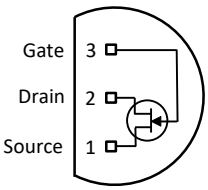


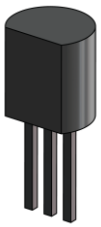
SOT23 Top View





TO-92 Bottom View





Product Summary

Parameters		2N3970 Min	2N3971 Min	2N3972 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-40	-40	-40	V
I_{DSS}	Drain to Source Saturation Current	50	25	5	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-4	-2	-0.5	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N3970; 2N3971; 2N3972	Through-Hole	TO-18	Bulk
PN3970; PN3971; PN3972	Through-Hole	TO-92	Bulk
SMP3970; SMP3971; SMP3972	Surface Mount	SOT23	Bulk
SMP3970TR; SMP3971TR; SMP3972TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N3970COT; 2N3971COT; 2N3972COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N3970CFT; 2N3971CFT; 2N3972CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	300	mW
P	Power Derating	1.7	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

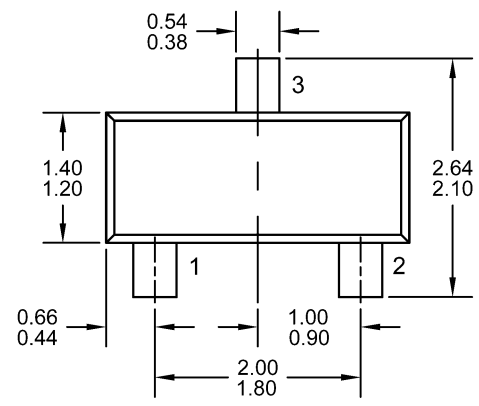
Parameters		Conditions	2N3970		2N3971		2N3972		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA,V_{DS} = 0V	-40		-40		-40		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V		-1		-1		-1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA	-4	-10	-2	-5	-0.5	-3	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 20V, V_{GS} = 0V (Pulsed)	50	150	25	75	5	30	mA
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = 20V, V_{GS} = -12V, T_A = 25°C V_{DS} = 20V, V_{GS} = -12V, T_A = 150°C		250 500		250 500		250 500	pA nA
I_{DG}	Drain Reverse Current	V_{DG} = 20V, I_S = 0A, T_A = 25°C V_{DG} = 20V, I_S = 0A, T_A = 150°C		250 500		250 500		250 500	pA nA
$V_{DS(ON)}$	Drain to Source ON Voltage	V_{GS} = 0V, I_D = ( )		1 (20)		1.5 (10)		2 (5)	V mA

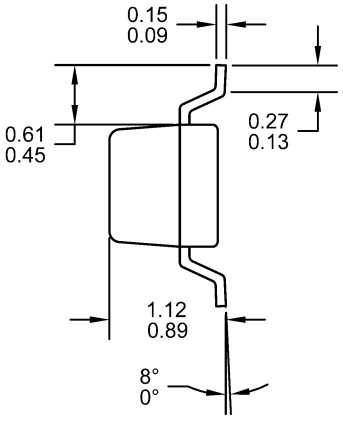
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

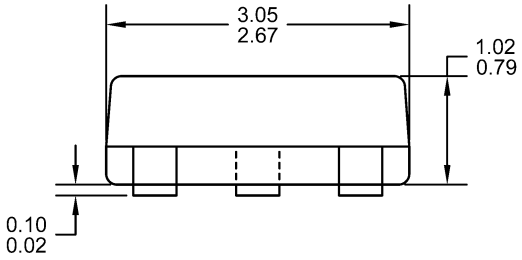
Parameters		Conditions	2N3970		2N3971		2N3972		Unit
			Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{GS} = 0V, I_D = 0A, f = 1kHz		30		60		100	Ω
C_{iss}	Input Capacitance	V_{DS} = -20V, V_{GS} = 0V, f = 1MHz		25		25		25	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 0V, V_{GS} = -12V, f = 1MHz		6		6		6	pF
t_d	Turn-On Delay Time	V_{DD} = 10V, $V_{GS(ON)}$ = 0V		10		15		40	nS
t_r	Rise Time	V_{DD} = 10V, $V_{GS(ON)}$ = 0V		10		15		40	nS
t_{off}	Turn-Off Time	V_{DD} = 10V,$V_{GS(ON)}$ = 0V		30		60		100	nS

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

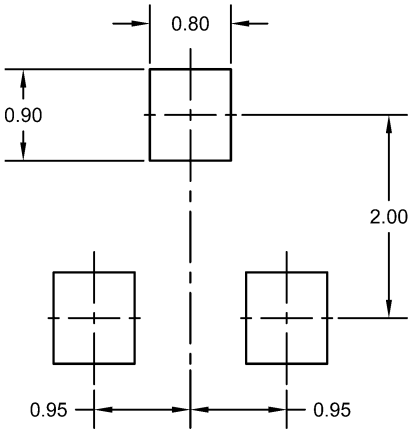






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

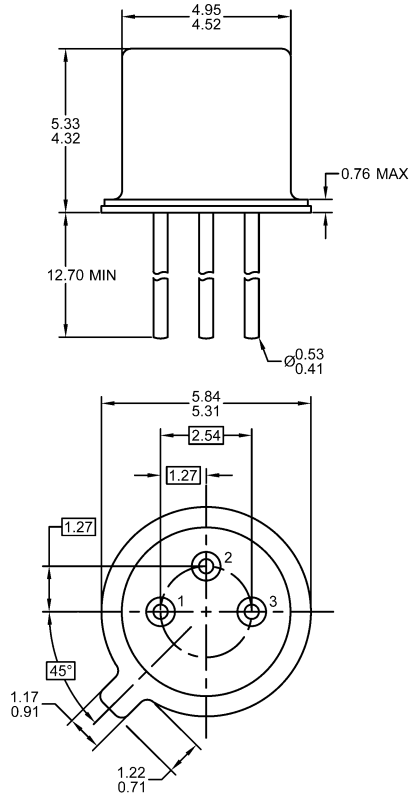
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

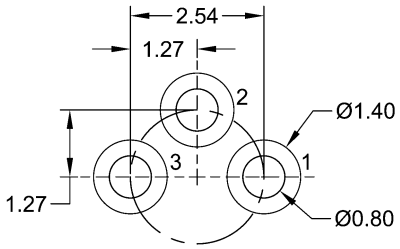
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.