2N4091, 2N4092, 2N4093 N-Channel JFET

Features

- InterFET N0132S Geometry
- Low Noise: 1.2 nV/√Hz Typical
- Fast Switching
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

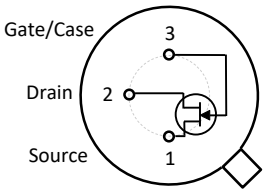
Applications

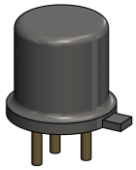
- Low $R_{DS(ON)}$
- Low Leakage
- Fast Switching

Description

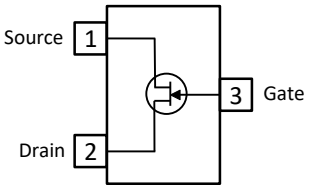
The -40V InterFET 2N4091, 2N4092, and 2N4093 JFET's are targeted for very low noise switching applications for mid to high frequency designs. Gate leakages are typically 50pA at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications.

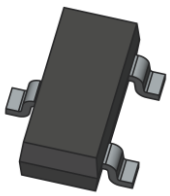
TO-18 Bottom View



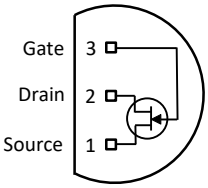


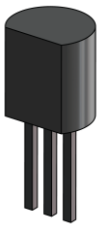
SOT23 Top View





TO-92 Bottom View





Product Summary

Parameters		2N4091 Min	2N4092 Min	2N4093 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-40	-40	-40	V
I_{DSS}	Drain to Source Saturation Current	30	15	8	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-5	-2	-1	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N4091; 2N4092; 2N4093	Through-Hole	TO-18	Bulk
PN4091; PN4092; PN4093	Through-Hole	TO-92	Bulk
SMP4091; SMP4092; SMP4093	Surface Mount	SOT23	Bulk
SMP4091TR; SMP4092TR SMP4093TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N4091COT; 2N4092COT 2N4093COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N4091CFT; 2N4092CFT 2N4093CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	1800	mW
P	Power Derating	12	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

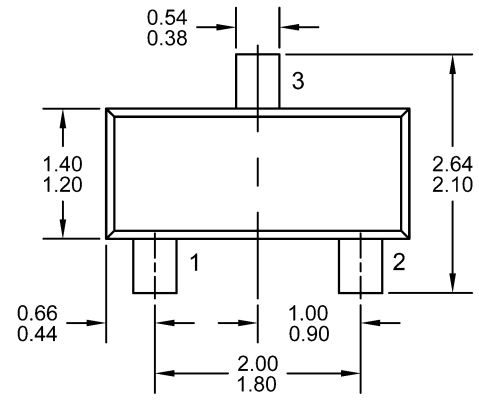
Parameters		Conditions	2N4091		2N4092		2N4093		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-40		-40		-40		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V		-1		-1		-1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 20V, I_D = 1nA	-5	-10	-2	-7	-1	-5	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 20V (Pulsed)	30		15		8		mA

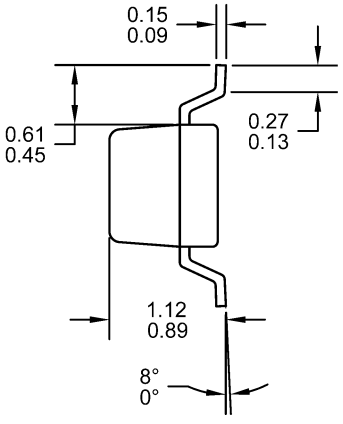
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

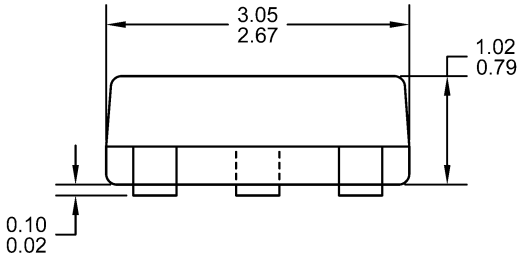
Parameters		Conditions	2N4091		2N4092		2N4093		Unit
			Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{GS} = 0V, I_D = 0A, f = 1kHz		30		50		80	Ω
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		16		16		16	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 0V, V_{GS} = -20V, f = 1MHz		5		5		5	pF
t_d	Turn-On Delay Time	V_{DD} = 3V, $V_{GS(ON)}$ = 0V		10		15		20	ns
t_r	Rise Time	V_{DD} = 3V, $V_{GS(ON)}$ = 0V		10		20		40	ns
t_{off}	Turn-Off Time	V_{DD} = 3V,$V_{GS(ON)}$ = 0V		40		60		80	ns

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

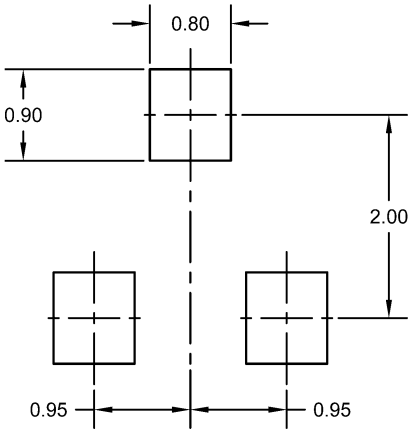






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

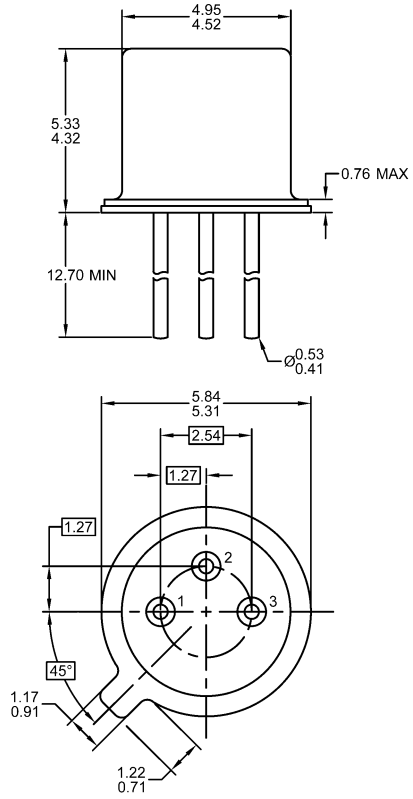
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

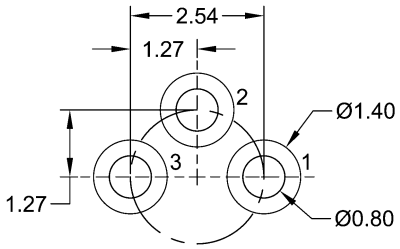
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.