2N4867/A, 2N4868/A, 2N4869/A N-Channel JFET

Features

- InterFET N0016H Geometry
- Typical Noise: 5 nV/√Hz
- Typical Ciss: 3.5pF
- Low Cutoff Voltage: 2N4867 < 2.0V
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

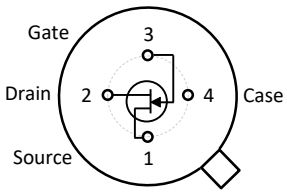
Applications

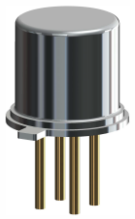
- Audio Amplifiers
- Small Signal Amplifier
- Ultrahigh Impedance Pre-Amplifier

Description

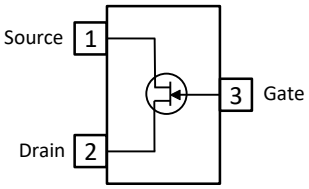
The -50V InterFET 2N4867/A, 2N4868/A, and 2N4869/A are targeted for Audio and sensitive amplifier stages for mid-frequencies designs. Gate leakages are typically less than 10pA at room temperatures. The 2N4867/A has a cutoff voltage of less than 2.0V ideal for low-level power supplies. The TO-72 package is hermetically sealed and suitable for military applications.

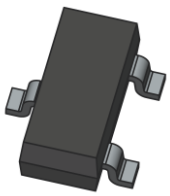
TO-72 Bottom View



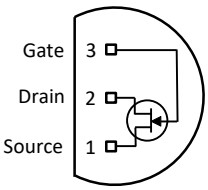


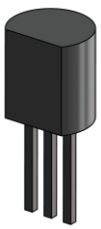
SOT23 Top View





TO-92 Bottom View





Product Summary

Parameters		2N4867/A Min	2N4868/A Min	2N4869/A Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-40	-40	-40	V
I_{DSS}	Drain to Source Saturation Current	0.4	1	2.5	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.7	-1	-1.8	V
G_{FS}	Forward Transconductance	700	1000	1300	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N4867; 2N4868; 2N4869 2N4867A; 2N4868A; 2N4869A	Through-Hole	TO-72	Bulk
PN4867; PN4868; PN4869 PN4867A; PN4868A; PN4869A	Through-Hole	TO-92	Bulk
SMP4867; SMP4868; SMP4869 SMP4867A; SMP4868A; SMP4869A	Surface Mount	SOT23	Bulk
SMP4867TR; SMP4868TR; SMP4869TR SMP4867ATR; SMP4868ATR; SMP4869ATR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N4867COT; 2N4868COT; 2N4869COT 2N4867ACOT; 2N4868ACOT; 2N4869ACOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N4867CFT; 2N4868CFT; 2N4869CFT 2N4867ACFT; 2N4868ACFT; 2N4869ACFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	300	mW
P	Power Derating	1.7	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

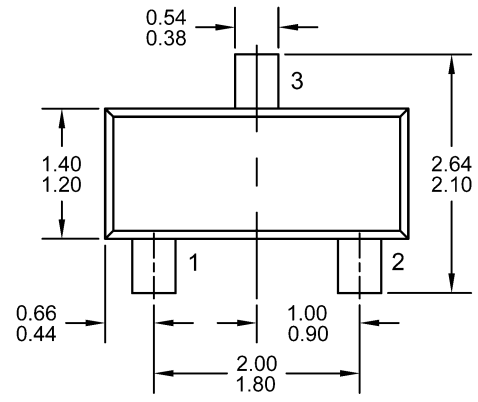
Parameters		Conditions	2N4867/A		2N4868/A		2N4869/A		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-40		-40		-40		V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -30V, V_{DS} = 0V, T_A = 25°C		-0.25		-0.25		-0.25	nA
		V_{GS} = -30V, V_{DS} = 0V, T_A = 150°C		-0.25		-0.25		-0.25	µA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 20V, I_D = 1µA	-0.7	-2	-1	-3	-1.8	-5	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 20V, V_{GS} = 0V (Pulsed)	0.4	1.2	1	3	2.5	7.5	mA

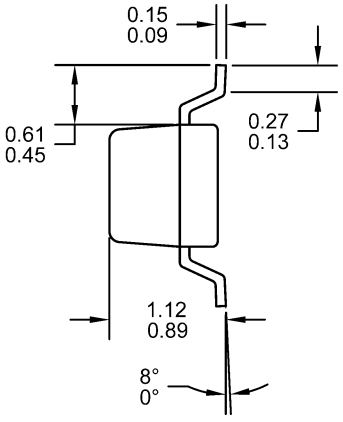
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

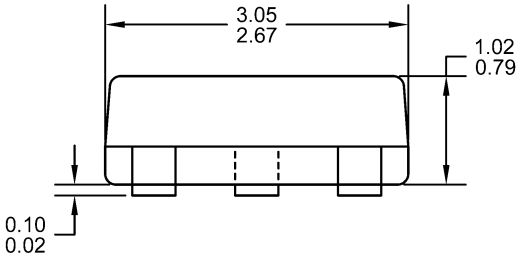
Parameters		Conditions	2N4867/A		2N4868/A		2N4869/A		Unit
			Min	Max	Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = 20V, V_{GS} = 0V, f = 1kHz	700	2000	1000	3000	1300	4000	µS
G_{OS}	Output Conductance	V_{DS} = 20V, V_{GS} = 0V, f = 1kHz		1.5		4		10	µS
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		25		25		25	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		5		5		5	pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 10V, V_{GS} = 0V, f = 10Hz		20		20		20	nV/√Hz
		V_{DS} = 10V, V_{GS} = 0V, f = 1kHz		10		10		10	
NF	Noise Figure	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz R_G = 20 kΩ, A variant R_G = 5 kΩ		1		1		1	dB

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

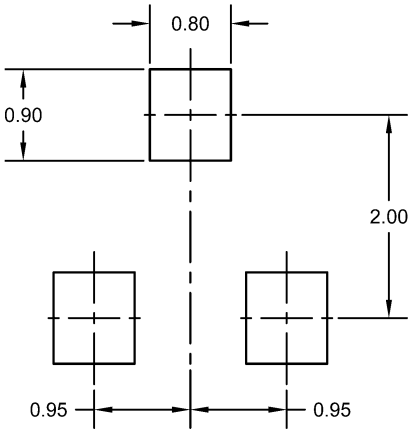






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

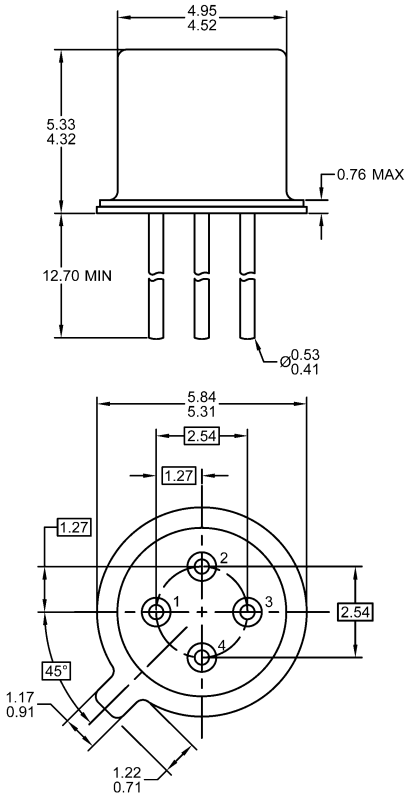
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

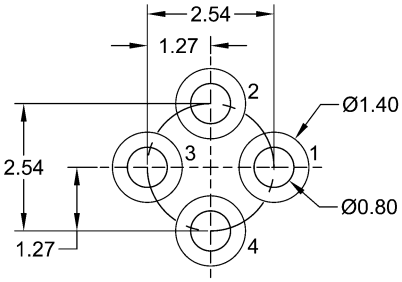
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.