2N5114, 2N5115, 2N5116 P-Channel JFET

Features

- InterFET P0099F Geometry
- Typical Noise: 8 nV/√Hz
- Low Rds(on)
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

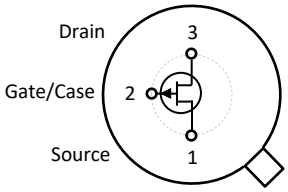
Applications

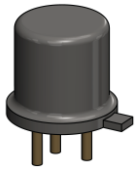
- Analog Switches
- Choppers

Description

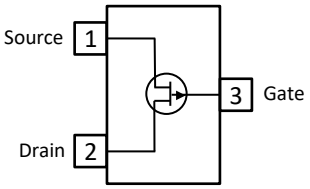
The 30V InterFET 2N5114, 2N5115, and 2N5116 are targeted for choppers and analog switch designs. The on resistance is typically less than 100 Ohms at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications.

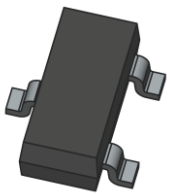
TO-18 Bottom View



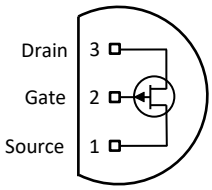


SOT23 Top View





TO-92 Bottom View



Product Summary

Parameters		2N5114 Min	2N5115 Min	2N5116 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	30	30	30	V
I_{DSS}	Drain to Source Saturation Current	-30	-15	-5	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	5	3	1	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N5114; 2N5115; 2N5116	Through-Hole	TO-18	Bulk
PN5114; PN5115; PN5116	Through-Hole	TO-92	Bulk
SMP5114; SMP5115; SMP5116	Surface Mount	SOT23	Bulk
SMP5114TR; SMP5115TR SMP5116TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N5114COT; 2N5115COT 2N5116COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N5114CFT; 2N5115CFT 2N5116CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	30	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	500	mW
P	Power Derating	4	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

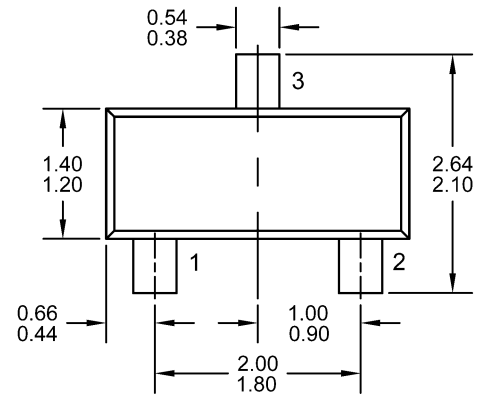
Parameters		Conditions	2N5114		2N5115		2N5116		Unit
			Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1mA	30		30		30		V
I_{GSS}	Gate to Source Reverse Current	V_{DS} = 20V, V_{GS} = 0V, T_A = 25°C V_{DS} = 20V, V_{GS} = 0V, T_A = 150°C		2 10		2 10		2 10	nA µA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = -15V, I_D = -1nA	5	10	3	6	1	4	V
$V_{GS(F)}$	Gate to Source Forward Voltage	V_{DS} = 0V, I_G = -1mA		-1		-1		-1	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 18V, V_{DS} = -15V V_{GS} = 15V, V_{DS} = -15V (Pulsed)	-30	-90	-15	-60	-5	-25	mA
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = -15V, V_{GS} = 12V, T_A = 25°C V_{DS} = -15V, V_{GS} = 7V, T_A = 150°C		-2 -10		-2 -10		-2 -10	nA µA
$V_{DS(ON)}$	Drain to Source ON Voltage	V_{GS} = 0V, I_D = -15mA		-1.3					V
		V_{GS} = 0V, I_D = -7mA				-0.8			
		V_{GS} = 0V, I_D = -3mA						-0.6	
$R_{DS(ON)}$	Static Drain to Source ON Resistance	V_{GS} = 0V, I_D = -1mA		75		100		150	Ω

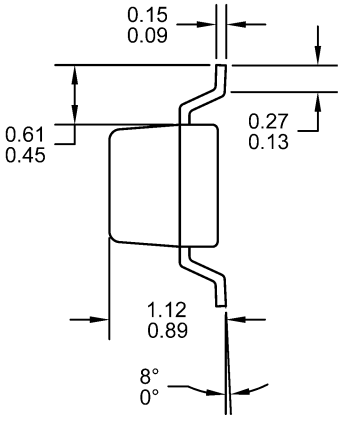
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

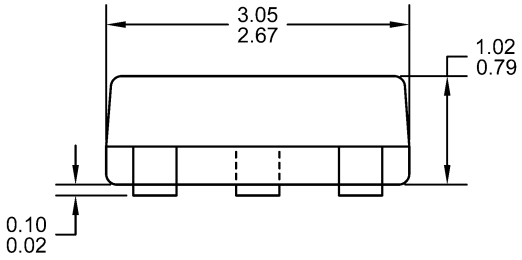
Parameters		Conditions	2N5114		2N5115		2N5116		Unit
			Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$	Drain to Source ON Resistance	V_{GS} = 0V, I_D = 0A, f = 1kHz		75		100		150	Ω
C_{iss}	Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1MHz		25		25		27	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = -10V, V_{GS} = 12V, f = 1MHz		7					pF
		V_{DS} = -10V, V_{GS} = 7V, f = 1MHz				7			
		V_{DS} = -10V, V_{GS} = 5V, f = 1MHz						7	
$t_{d(ON)}$	Turn-On Delay Time	V_{DD} = V		6		10		25	ns
t_r	Rise Time	V_{DD} = V		10		20		35	ns
$t_{d(OFF)}$	Turn-Off Delay Time	V_{DD} = V		6		8		20	ns
t_f	Fall Time	V_{DD} = V		15		30		60	ns

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

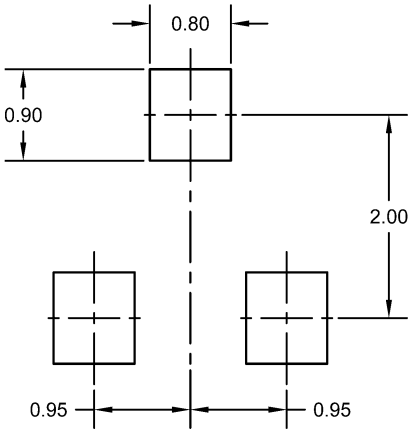






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

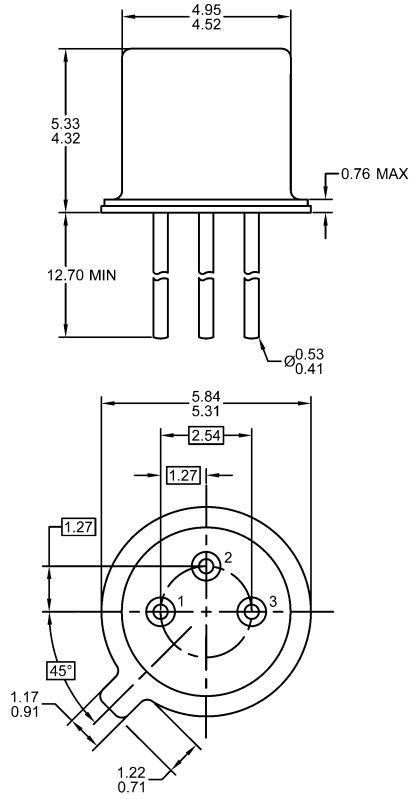
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

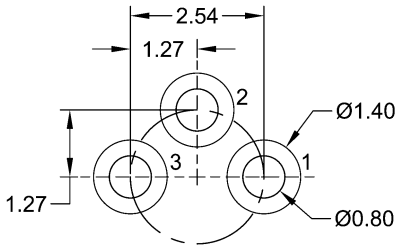
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.