

## 2N6550 N-Channel JFET

### Features

- InterFET [N0450L Geometry](#)
- Low Noise: 0.9 nV/√Hz Typical
- High Gain: 25mS Minimum
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

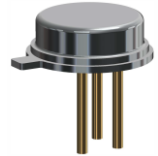
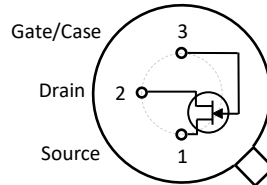
### Applications

- Low-Noise, High Gain Amplifiers

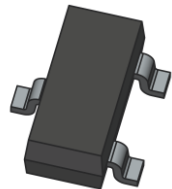
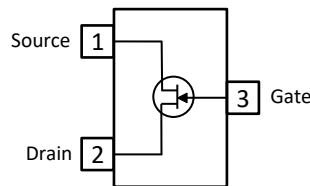
### Description

The -20V InterFET 2N6550 is targeted for sensitive amplifier stages for mid-frequencies designs. The 2N6550 has a cutoff voltage of less than 3.0V ideal for low-level power supplies. The TO-46 package is hermetically sealed and suitable for military applications.

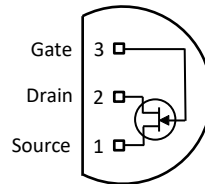
**TO-46 Bottom View**



**SOT23 Top View**



**TO-92 Bottom View**



### Product Summary

Parameters		2N6550 Min	Unit
$BV_{GSS}$	Gate to Source Breakdown Voltage	-20	V
$I_{DSS}$	Drain to Source Saturation Current	10	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.3	V
$G_{FS}$	Forward Transconductance	25	mS

### Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
2N6550	Through-Hole	TO-46	Bulk
PN6550	Through-Hole	TO-92	Bulk
SMP6550	Surface Mount	SOT23	Bulk
SMP6550TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
2N6550COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
2N6550CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



**Disclaimer:** It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

## Electrical Characteristics

### Maximum Ratings (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Value	Unit
$V_{RGS}$ Reverse Gate Source and Gate Drain Voltage	-20	V
$I_{FG}$ Continuous Forward Gate Current	50	mA
$P_D$ Continuous Device Power Dissipation	400	mW
$P$ Power Derating	2.3	mW/ $^\circ\text{C}$
$T_J$ Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
$T_{STG}$ Storage Temperature	-65 to 200	$^\circ\text{C}$

### Static Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Conditions	2N6550			Unit
		Min	Typ	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = 10\mu\text{A}$	-20			V
$I_{GSS}$ Gate to Source Reverse Current	$V_{GS} = -10V, V_{DS} = 0V, T_A = 25^\circ\text{C}$			-3	nA
	$V_{GS} = -10V, V_{DS} = 0V, T_A = 85^\circ\text{C}$			-0.1	$\mu\text{A}$
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10V, I_D = 0.1\text{mA}$	-0.3		-3	V
$I_{DSS}$ Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 10V$ (Pulsed)	10	100	250	mA

### Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Conditions	2N6550			Unit
		Min	Typ	Max	
$G_{FS}$ Forward Transconductance	$V_{DS} = 10V, I_D = 10\text{mA}, f = 1\text{kHz}$	25		150	mS
$G_{OS}$ Output Conductance	$V_{DS} = 10V, I_D = 10\text{mA}, f = 1\text{kHz}$			150	$\mu\text{S}$
$C_{iss}$ Input Capacitance	$V_{DS} = 10V, I_D = 10\text{mA}, f = 140\text{kHz}$		30	35	pF
$C_{rss}$ Reverse Transfer Capacitance	$V_{DS} = 10V, f = 140\text{kHz}$		10	20	pF
$e_n$ Equivalent Input Noise Voltage	$V_{DS} = 5V, I_D = 10\text{mA}, f = 10\text{Hz}$		1.4	2	nV/ $\sqrt{\text{Hz}}$
	$V_{DS} = 5V, I_D = 10\text{mA}, f = 1\text{kHz}$		6	10	
$e_{n\text{ Total}}$ Equivalent Total Input Noise Voltage	$V_{DS} = 5V, I_D = 10\text{mA}, f = 10\text{kHz to } 20\text{kHz}$		0.4	0.6	$\mu\text{Vrms}$
$i_n$ Equivalent Input Noise Current	$R_S < 100\text{ k}\Omega, f = 1\text{kHz}$		0.1		pA/ $\sqrt{\text{Hz}}$

## SOT23 (TO-236AB) Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

### Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

