

IFBF510, IFBF511 N-Channel JFET

Features

- InterFET [N0026 Geometry](#)
- Low Noise: 3 nV/√Hz Typical
- Low Ciss: 5.0pF Maximum
- Low Leakage: 10pA Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

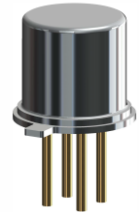
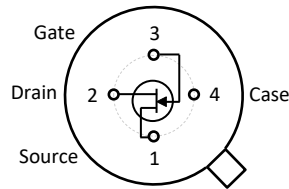
Applications

- Low Noise High Gain
- Replacement for BF510 and BF511
- Mixers
- Oscillators
- VHF Amplifiers

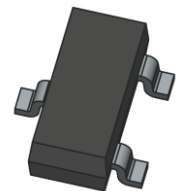
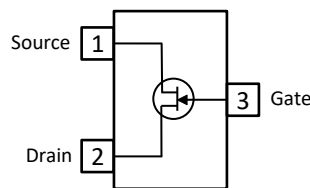
Description

The -20V InterFET IFBF510 and IFBF511 are targeted for low noise amplifier stages as well as mixer and oscillator designs. Gate leakages are typically less than 10pA at room temperatures. The TO-72 package is hermetically sealed and suitable for military applications.

TO-72 Bottom View

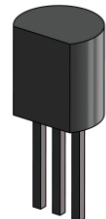
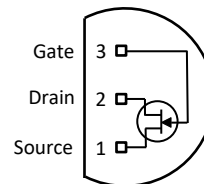


SOT23 Top View



Note: The SOT23 package is pinned out differently than the BF51x part to optimize thermal performance. Package and pinout variations are available through InterFET custom ordering.

TO-92 Bottom View



Product Summary

Parameters		IFBF510 Min	IFBF511 Min	Unit
BV _{GSS}	Gate to Source Breakdown Voltage	-20	-20	V
I _{DSS}	Drain to Source Saturation Current	0.7	2.5	mA
V _{GS(off)}	Gate to Source Cutoff Voltage	-0.8 (typ)	-1.5 (typ)	V
G _{FS}	Forward Transconductance	2.5	4	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFBF510; IFBF511	Through-Hole	TO-72	Bulk
PNBF510; PNB511	Through-Hole	TO-92	Bulk
SMPBF510; SMPBF511	Surface Mount	SOT23	Bulk
SMPBF510TR; SMPBF511TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
IFBF510COT; IFBF511COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFBF510CFT; IFBF511CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG} Continuous Forward Gate Current	10	mA
P_D Continuous Device Power Dissipation	300	mW
P Power Derating	1.7	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 150	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IFBF510		IFBF511		Unit
		Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu\text{A}$	-20		-20		V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -15V, V_{DS} = 0V, T_A = 25^\circ\text{C}$		-10		-10	nA
$V_{GS(F)}$ Gate to Source Forward Voltage	$V_{DS} = 0V, I_G = 1\text{mA}$		1		1	V
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10V, I_D = 1\text{nA}$	-0.5		-0.8		V
I_{DSS} Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 10V$ (Pulsed)	0.7	3.0	2.5	7.0	mA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IFBF510		IFBF511		Unit
		Min	Max	Min	Max	
G_{FS} Forward Transconductance	$V_{DS} = 10V, V_{GS} = 0V, f = 1\text{kHz}$	2.5		4		mS
G_{OS} Output Conductance	$V_{DS} = 10V, V_{GS} = 0V, f = 1\text{MHz}$		60		80	μS
C_{ISS} Input Capacitance	$V_{DS} = 10V, V_{GS} = 0V, f = 1\text{MHz}$		5		5	pF
C_{RSS} Reverse Transfer Capacitance	$V_{DS} = 10V, V_{GS} = 0V, f = 1\text{MHz}$		1.5		1.5	pF

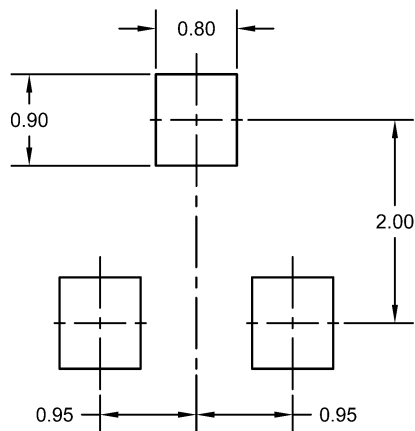
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

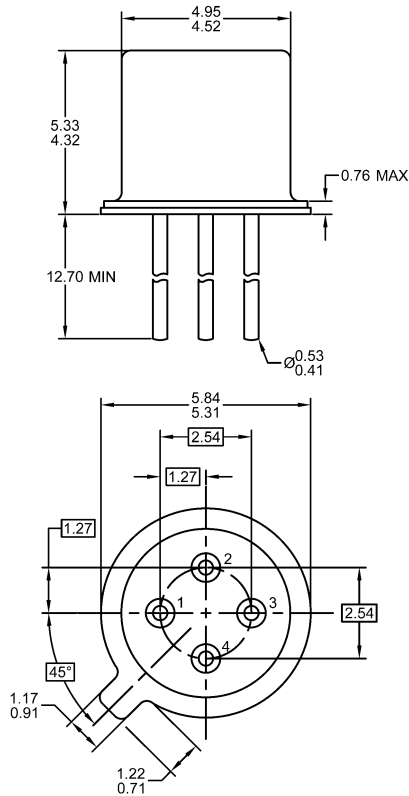
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

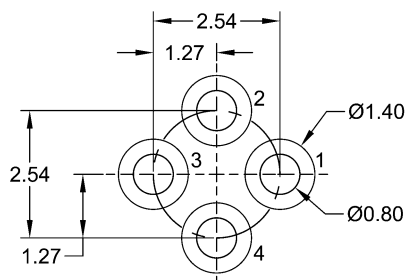
TO-72 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Four leaded device. Not all leads are shown in drawing views.
3. Package weight approximately 0.31 grams
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.