

## J111/A, J112/A, J113/A N-Channel JFET

### Features

- InterFET [N0132S Geometry](#)
- Low Noise: 1.2 nV/√Hz Typical
- High Gain: 15mS Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

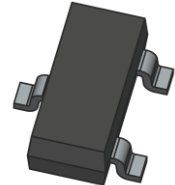
### Applications

- Choppers
- Commutators
- Analog Switches

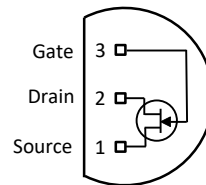
### Description

The -25V InterFET J111/A, J112/A, and J113/A JFET's are targeted for high gain low noise switching, commutator, and chopper applications.

SOT23 Top View



TO-92 Bottom View



### Product Summary

Parameters	J111/A Min	J112/A Min	J113/A Min	Unit
$BV_{GSS}$ Gate to Source Breakdown Voltage	-40	-40	-40	V
$I_{DSS}$ Drain to Source Saturation Current	-2	-2	-2	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-5	-2	-1	V

### Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J111; J112; J113 J111A; J112A; J113A	Through-Hole	TO-92	Bulk
SMPJ111; SMPJ112; SMPJ113 SMPJ111A; SMPJ112A; SMPJ113A	Surface Mount	SOT23	Bulk
SMPJ111TR; SMPJ112TR; SMPJ113TR SMPJ111ATR; SMPJ112ATR; SMPJ113ATR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
J111COT; J112COT; J113COT J111ACOT; J112ACOT; J113ACOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
J111CFT; J112CFT; J113CFT J111ACFT; J112ACFT; J113ACFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



**Disclaimer:** It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

## Electrical Characteristics

### Maximum Ratings (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Parameters	Value	Unit
$V_{RGS}$ Reverse Gate Source and Gate Drain Voltage	-40	V
$I_{FG}$ Continuous Forward Gate Current	50	mA
$P_D$ Continuous Device Power Dissipation	360	mW
P Power Derating	3.3	mW/ $^\circ\text{C}$
$T_J$ Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
$T_{STG}$ Storage Temperature	-65 to 150	$^\circ\text{C}$

### Static Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified, Highlighted values = A variant)

Parameters	Conditions	J111/A		J112/A		J113/A		Unit
		Min	Max	Min	Max	Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$V_{DS} = 0V, I_G = -1\mu\text{A}$	-35		-35		-35		V
		-40		-40		-40		
$I_{GSS}$ Gate to Source Reverse Current	$V_{GS} = -15V, V_{DS} = 0V$		-1		-1		-1	nA
			-2		-2		-2	
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 5V, I_D = 1\mu\text{A}$	-3	-10	-1	-5		-3	V
		-5	-10	-2	-7	-1	-5	
$I_{DSS}$ Drain to Source Saturation Current	$V_{GS} = 0V, V_{DS} = 15V$ (Pulsed)	20		5		2		mA
		30		15		8		
$I_{D(OFF)}$ Drain Cutoff Current	$V_{DS} = 15V, V_{GS} = -10V$		-1		-1		-1	nA
			-1		-1		-1	

### Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$ , Unless otherwise specified, Highlighted values = A variant)

Parameters	Conditions	J111/A		J112/A		J113/A		Unit
		Min	Max	Min	Max	Min	Max	
$R_{DS(ON)}$ Drain to Source ON Resistance	$V_{DS} = 0.1V, V_{GS} = 0V,$ $f = 1\text{kHz}$		30		50		100	$\Omega$
			30		50		80	
$C_{gd}$ Drain Gate Capacitance	$V_{DS} = 0V, V_{GS} = -10V,$ $f = 1\text{MHz}$		5		5		5	pF
$C_{gs}$ Input Capacitance	$V_{DS} = 0V, V_{GS} = -10V,$ $f = 1\text{MHz}$		5		5		5	pF
$C_{gd} + C_{gs}$ Drain + Source Gate Capacitance	$V_{DS} = V_{GS} = 0V, f = 1\text{MHz}$		28		28		28	pF
$t_{d(ON)}$ Turn ON Delay Time	$V_{DD} = 10V$ J111/A: $V_{GS(OFF)} = -12V,$ $R_L = 800\Omega$ J112/A: $V_{GS(OFF)} = -7V,$ $R_L = 1600\Omega$ J113/A: $V_{GS(OFF)} = -5V,$ $R_L = 3200\Omega$	7 (typ)		7 (typ)		7 (typ)		ns
$t_r$ Rise Time		6 (typ)		6 (typ)		2 (typ)		ns
$t_{d(OFF)}$ Turn OFF Delay Time		20 (typ)		20 (typ)		20 (typ)		ns
$t_f$ Fall Time		15 (typ)		15 (typ)		15 (typ)		ns

## SOT23 (TO-236AB) Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

### Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.